http://researchspace.auckland.ac.nz

ResearchSpace@Auckland

Copyright Statement

The digital copy of this thesis is protected by the Copyright Act 1994 (New Zealand).

This thesis may be consulted by you, provided you comply with the provisions of the Act and the following conditions of use:

- Any use you make of these documents or images must be for research or private study purposes only, and you may not make them available to any other person.
- Authors control the copyright of their thesis. You will recognise the author’s right to be identified as the author of this thesis, and due acknowledgement will be made to the author where appropriate.
- You will obtain the author's permission before publishing any material from their thesis.

To request permissions please use the Feedback form on our webpage. http://researchspace.auckland.ac.nz/feedback

General copyright and disclaimer

In addition to the above conditions, authors give their consent for the digital copy of their work to be used subject to the conditions specified on the Library Thesis Consent Form and Deposit Licence.

Note : Masters Theses

The digital copy of a masters thesis is as submitted for examination and contains no corrections. The print copy, usually available in the University Library, may contain corrections made by hand, which have been requested by the supervisor.
Bit-Stream Control of Doubly Fed Induction Generators

Student: Jonathan Bernard Bradshaw

Supervisors: Associate Professor Udaya Madawala
Dr. Nitish Patel

7 March 2012

Abstract

In recent years rising energy costs and concerns about global climate change have led to the widespread development of renewable electricity generation technology, especially wind generation. The Doubly Fed Induction Generator (DFIG) is commonly used for wind generation applications as it allows for efficient operation of the wind turbine by varying the speed of the generator without resorting to the use of large power converters. A typical DFIG system employs a wound rotor induction generator, with a stator that is directly connected to an external AC grid. The rotor winding is connected to the AC grid via a pair of back-to-back power converters: the Rotor Side Converter (RSC) and Grid Side Converter (GSC).

The RSC and GSC require separate vector control systems. Traditionally, these control systems are implemented using microcontrollers, which perform the required control functions sequentially. As the complexity of control algorithms increases to achieve improved functionality and the time available to complete the calculations reduces to keep pace with ever-faster power electronic devices, microprocessor based solutions cannot execute the control program within the available time limit.

A potential solution to this performance limitation is the use of hardware based control systems, which can execute control algorithms extremely quickly because many operations are processed in parallel. This is attractive for use in control systems, but implementing hardware control systems is difficult. The designer must either manually translate the control algorithm into individual operations, which are then usually encoded using a Hardware Description Language (HDL), or employ an automated code generation tool. The code is then synthesised and used to program a Field Programmable Gate Array (FPGA).

An alternative method for implementing digital control systems is the Bit-Stream control technique. In contrast to the usual methods of implementing digital controllers, Bit-Stream control systems are developed using standard schematic editors provided by FPGA manufacturers. Provided that the desired control functions are available in the Bit-Stream library, the designer need not use HDL to develop the control system.

A Bit-Stream based control system for a 2.6 kW DFIG is proposed in this thesis. As previously published research on Bit-Stream control systems focused on scalar control systems only, new Bit-Stream blocks are developed for use in vector control systems. The new vector control blocks include: coordinate transformation units, a Phase Locked Loop (PLL) and a family of modulators which convert Bit-Stream reference signals to gate drive commands for three-phase inverters. A Bit-Stream control system for a 2 kW GSC is developed, simulated and tested experimentally. Elements of this control system are adapted and re-used to develop a Bit-Stream based control system for the RSC of a 2.6 kW DFIG system. These are the first Bit-Stream based vector control systems to be reported in the literature. Supervisory control systems are added to the GSC and RSC to provide closed-loop speed control of the generator speed, soft synchronisation of the generator to the AC grid and operation with unity power factor at the stator terminals of the generator. Control of the DFIG is demonstrated by simulation and experimental testing of a 2.6 kW DFIG system.
Acknowledgments

Although a PhD thesis is allegedly a one-person exercise, the actual process of researching for and writing a PhD thesis is most definitely a team sport.

Firstly, I must thank my supervisor Dr. Udaya Madawala who has been enthusiastic about the project since I first contacted him about returning to study. I went in thinking to study for a Masters of Engineering and he convinced me that since I was there I might as well go for the PhD instead. He has been a constant source of ideas and motivation for the research, the papers and the thesis, as well as arranging excellent opportunities for my studies: two months studying in Aalborg University, Denmark, and numerous meeting with professors, lecturers and students from other universities. I owe him special thanks for the many hours he has put in helping me edit conference papers, journal papers and chapters of this thesis.

Dr. Nitish Patel has also had a massive impact upon this thesis; as the original developer of the Bit-Stream method he has been an information source, sounding board and troubleshooter.

In addition to my supervisors, a number of other students and staff have played vital roles in my studies: Dr. Duleepa Thrimawithana has provided a number of helpful hints, opinions on papers, suggestions for development and, when all else failed, some much-needed proof reading; Dr. Tobias Geyer has been a valuable sounding board for the operation and modelling of inverters and generators; and Victor Church has provided some of that information about the real world operation of machines that just isn’t in the textbook. I also want to thank my fellow postgraduate students; there are too many of them to list here, but I appreciate their support. Thanks also go to my parents Rosemary and David Bradshaw for their support and proof reading efforts.

Finally, I must thank and my wonderful wife Mira Bradshaw for encouraging me to return to university, her patience and support during the PhD and her help with the thesis planning, editing and proofing. Without her I might never have begun this PhD, and I certainly wouldn’t have finished it.

Jonathan Bradshaw

7 March 2012
# Contents

**Abstract** v

**Acknowledgments** vii

**List of Figures** xv

**List of Tables** xxi

**List of Abbreviations** xxiii

**List of Symbols** xxv

1 **Introduction** 1

1.1 Background ................................................. 1

1.2 Motivation .................................................. 2

1.3 Research Objectives ........................................ 3

1.4 Thesis Organisation ........................................ 3

2 **Control of Doubly Fed Induction Generators** 5

2.1 The Bit-Stream Control Technique .......................... 5

2.1.1 Representation of Bit-Stream Signals ................... 5

2.1.2 Bit-Stream Control Elements .......................... 7

2.2 Overview of Doubly Fed Induction Generators .............. 8

2.3 Operating Principles of Induction Machines ................. 10

2.4 A Survey of DFIG Control Methods ........................ 12

2.4.1 Historical Background ................................ 12

2.4.2 Vector Control of DFIGs ............................... 13

2.4.3 Sensorless operation ................................ 14

2.4.4 Operation Within Unbalanced AC Networks ............. 14

2.4.5 Fault Ride Through ................................ 14
## Contents

2.4.6 Stand-Alone Operation .............................................. 15
2.5 Principles of Vector Control .......................................... 16
2.5.1 Vector Control of the Grid Side Converter ....................... 17
2.5.2 Vector Control of Wound Rotor Induction Machines ............. 18
2.6 Proposed DFIG Control Method ....................................... 20
2.7 Summary ................................................................. 21

3 Bit-Stream Based Phase Locked Loop ................................ 23
3.1 Structure of the Phase Locked Loop .................................. 24
3.1.1 Phase Detector ...................................................... 24
3.1.2 Loop Filter ........................................................ 25
3.1.3 Controlled Oscillator .............................................. 25
3.1.4 Small Signal Equivalent Model .................................. 25
3.2 Bit-Stream Implementation of PLL .................................... 26
3.2.1 Phase Detector ...................................................... 26
3.2.2 PI Controller ........................................................ 28
3.2.3 Numerically Controlled Oscillator (NCO) ....................... 28
3.3 Simulation Results .................................................... 30
3.4 Experimental Results .................................................. 31
3.5 Summary ................................................................. 32

4 Bit-Stream Modulators for Single Phase Power Electronics Applications 35
4.1 Two Level Bit-Stream Modulators .................................... 36
4.1.1 Fixed Frequency Pulse Width Modulators ....................... 36
4.1.2 Standard Down-sampled Bit-Stream Modulators ............... 39
4.1.3 Hysteretically Down-sampled Bit-Stream Modulators .......... 40
4.1.4 Dead Time Compensated HDBS Modulator ..................... 42
4.2 Three Level Bit-Stream Modulators .................................. 44
4.2.1 Three Level HDBS Modulator ................................... 44
4.2.2 Dead Time Compensated Three-Level HDBS Modulator ...... 48
4.2.3 Comparison with Fixed Frequency Three Level PWM .......... 50
4.3 Summary ................................................................. 51

5 Bit-Stream Modulators for Three Phase Power Electronics Applications 53
5.1 Proposed Three-Phase Modulation Method ........................ 55
5.1.1 Error Integrators ..................................................... 55
## 7 Bit-Stream Control of Rotor Side Converter

7.1 Rotor Side Converter Specifications ............................................. 94
7.2 Control System for RSC ................................................................. 95
   7.2.1 Measurement System ................................................................. 96
   7.2.2 Rotor Current Controllers ......................................................... 98
   7.2.3 Modulator ........................................................................ 98
7.3 Bit-Stream Implementation of Control System for the RSC . .............. 98
   7.3.1 Measurement System ................................................................. 99
   7.3.2 Rotor Current Controllers ......................................................... 103
   7.3.3 Modulator ........................................................................ 103
   7.3.4 Under and Over Speed Protection .............................................. 103
7.4 Simulation Results ....................................................................... 104
7.5 Experimental Results .................................................................... 106
   7.5.1 Rotor Current Control Response .............................................. 107
   7.5.2 Over- and Under-speed Protection Systems .................................. 108
   7.5.3 FPGA Resource Consumption .................................................... 109
7.6 Summary ..................................................................................... 109

## 8 Bit-Stream Control of Doubly Fed Induction Generator

8.1 DFIG Specifications ............................................................... 112
8.2 Control System for DFIG .......................................................... 112
   8.2.1 Supervisory System ................................................................. 112
   8.2.2 DC Link Soft Start ................................................................. 114
   8.2.3 Excitation Control System ....................................................... 114
   8.2.4 Speed Control System ............................................................. 117
8.3 Bit-Stream Control of DFIG System ............................................ 118
   8.3.1 Supervisory System ................................................................. 119
   8.3.2 DC Link Soft Start ................................................................. 119
   8.3.3 Excitation Control System ....................................................... 119
   8.3.4 Speed Control System ............................................................. 119
8.4 Simulation Results ....................................................................... 120
   8.4.1 DC Link Soft Start ................................................................. 121
   8.4.2 Excitation Control System ....................................................... 122
List of Figures

2.1 Decomposition of Bit-Stream signal $S$ into positive and negative quanta. ........... 6
2.2 Structure of a Bit-Stream integrator block. ..................................................... 7
2.3 A typical DFIG system used in a wind energy application. .............................. 8
2.4 Power flow through the DFIG. ........................................................................ 10
2.5 Wound rotor induction machine. ....................................................................... 11
2.6 Photograph of the WRIM used for the experimental work of this thesis. ............ 12
2.7 Graphical representation of the Clarke Transformation. .................................... 16
2.8 Graphical representation of Park’s Transformation. .......................................... 17
2.9 Single phase equivalent circuit of the GSC. ......................................................... 18
2.10 Alignment of the $DQ$ reference frame to the stator flux vector and measurement of rotor current components on this reference frame. ........... 19
2.11 Block diagram of proposed Bit-Stream control system for DFIG applications. 20
3.1 Block diagram of the basic PLL system. ............................................................. 24
3.2 Small signal behaviour of the PLL system. ......................................................... 25
3.3 Bit-Stream PLL implementation. ........................................................................ 26
3.4 Two-input Bit-Stream vector scaling block. ......................................................... 27
3.5 Bit-Stream blocks for (a) Clarke Transformation, (b) Park’s Transformation. .... 28
3.6 Bit-Stream based numerically controlled oscillator ............................................ 29
3.7 Simulated PLL lock-in. ................................................................................. 30
3.8 Experimental PLL lock-in. ................................................................................ 32
4.1 Test system for proposed two-level Bit-Stream modulators. ............................. 36
4.2 Bit-Stream based two-level pulse width modulator ............................................ 36
4.3 Simulated behaviour of two-level VSI under PWM control. ............................ 37
4.4 Experimental apparatus used for single phase inverter testing. ......................... 38
4.5 Experimental behaviour of two-level VSI under PWM control. ....................... 38
4.6 Standard Down-sampled Bit-Stream modulator. ............................................... 40
<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.7</td>
<td>Hysteretic Down-sampling Bit-Stream modulator</td>
</tr>
<tr>
<td>4.8</td>
<td>Experimental behaviour of two-level VSI under HDBS control</td>
</tr>
<tr>
<td>4.9</td>
<td>Hysteretic Down-sampling Bit-Stream modulator with dead time compensation</td>
</tr>
<tr>
<td>4.10</td>
<td>Experimental behaviour of two-level VSI under HDBS control with DTC</td>
</tr>
<tr>
<td>4.11</td>
<td>Test system for proposed three-level Bit-Stream modulators</td>
</tr>
<tr>
<td>4.12</td>
<td>Three level HDBS modulator</td>
</tr>
<tr>
<td>4.13</td>
<td>Simulation results for full-bridge VSI with HDBS modulator</td>
</tr>
<tr>
<td>4.14</td>
<td>State machine for full-bridge VSI with balanced switching losses</td>
</tr>
<tr>
<td>4.15</td>
<td>Approximate error trajectory of the full-bridge HDBS modulator</td>
</tr>
<tr>
<td>4.16</td>
<td>Simulation results for full-bridge VSI with improved 3L HDBS modulator</td>
</tr>
<tr>
<td>4.17</td>
<td>Experimental results for full-bridge VSI with improved 3L HDBS modulator</td>
</tr>
<tr>
<td>4.18</td>
<td>Three-level VSI with dead-time-compensated HDBS modulator</td>
</tr>
<tr>
<td>4.19</td>
<td>Experimental behaviour of full-bridge PWM-controlled inverter</td>
</tr>
<tr>
<td>5.1</td>
<td>The proposed Bit-Stream space vector modulator</td>
</tr>
<tr>
<td>5.2</td>
<td>State machine for the square-box Bit-Stream SVM unit</td>
</tr>
<tr>
<td>5.3</td>
<td>Operating waveforms of the square box Bit-Stream SVM unit</td>
</tr>
<tr>
<td>5.4</td>
<td>Influence of the error box on the state machine</td>
</tr>
<tr>
<td>5.5</td>
<td>Operating waveforms of the hexagonal box Bit-Stream SVM unit</td>
</tr>
<tr>
<td>5.6</td>
<td>Operating waveforms of the sector-aware hexagonal box Bit-Stream SVM unit</td>
</tr>
<tr>
<td>5.7</td>
<td>Schematic of the proposed Bit-Stream SVM with DTC</td>
</tr>
<tr>
<td>5.8</td>
<td>Operating waveforms of the hexagonal box Bit-Stream SVM with DTC</td>
</tr>
<tr>
<td>5.9</td>
<td>Operating waveforms of the SVPWM-controlled inverter</td>
</tr>
<tr>
<td>6.1</td>
<td>Circuit diagram of the GSC</td>
</tr>
<tr>
<td>6.2</td>
<td>Block diagram of proposed control system for the GSC</td>
</tr>
<tr>
<td>6.3</td>
<td>Orientation of grid voltage and GSC current vectors on the $\alpha\beta$ and $DQ$ reference frames</td>
</tr>
<tr>
<td>6.4</td>
<td>Single phase equivalent circuit of GSC</td>
</tr>
<tr>
<td>6.5</td>
<td>Response of the GSC to a step change of Q axis current reference</td>
</tr>
<tr>
<td>6.6</td>
<td>Simplified model of the Q-axis current controller</td>
</tr>
<tr>
<td>6.7</td>
<td>Simplified model of the DC link voltage control loop</td>
</tr>
<tr>
<td>6.8</td>
<td>Simulated response of the simplified DC link control system to a step change in DC load current</td>
</tr>
<tr>
<td>6.9</td>
<td>Grid side line filter</td>
</tr>
<tr>
<td>6.10</td>
<td>Bit-Stream implementation of the grid measurement system</td>
</tr>
<tr>
<td>Figure</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>6.11</td>
<td>Bit-Stream implementation of the grid current control system.</td>
</tr>
<tr>
<td>6.12</td>
<td>Bit-Stream implementation of the modulator for the GSC.</td>
</tr>
<tr>
<td>6.13</td>
<td>Bit-Stream implementation of the DC link voltage control system.</td>
</tr>
<tr>
<td>6.14</td>
<td>Simulated response of current control loops to step changes in Q axis current reference.</td>
</tr>
<tr>
<td>6.15</td>
<td>Simulated response of current control loops to step changes in DC load.</td>
</tr>
<tr>
<td>6.16</td>
<td>GSC and control system apparatus</td>
</tr>
<tr>
<td>6.17</td>
<td>Experimental response of the GSC to step changes in reactive current reference.</td>
</tr>
<tr>
<td>6.18</td>
<td>Experimental response of the GSC to step changes in DC load.</td>
</tr>
<tr>
<td>6.19</td>
<td>Line currents of the GSC when operating in rectifying mode with 2 kW DC load and no reactive current.</td>
</tr>
<tr>
<td>6.20</td>
<td>Line currents of the GSC when operating in inverting mode with 2 kW DC source and no reactive current.</td>
</tr>
<tr>
<td>7.1</td>
<td>Circuit diagram of the WRIM and RSC.</td>
</tr>
<tr>
<td>7.2</td>
<td>Block diagram of proposed control system for the RSC.</td>
</tr>
<tr>
<td>7.3</td>
<td>Rotor current reference frame orientation, (a) physical orientation of stator flux and rotor current vectors, (b) slip angle diagram for a two pole generator.</td>
</tr>
<tr>
<td>7.4</td>
<td>Block diagram of the stator flux estimator.</td>
</tr>
<tr>
<td>7.5</td>
<td>Implementation of Bit-Stream based generator measurement system.</td>
</tr>
<tr>
<td>7.6</td>
<td>Bit-Stream implementation of stator flux estimator.</td>
</tr>
<tr>
<td>7.7</td>
<td>Rotary encoder output signals when rotating (a) forwards and (b) backwards.</td>
</tr>
<tr>
<td>7.8</td>
<td>Bit-Stream angle reference system</td>
</tr>
<tr>
<td>7.9</td>
<td>Illustration of the effects of clumping on the speed measurement signals $\omega_X$ and $\omega_R$.</td>
</tr>
<tr>
<td>7.10</td>
<td>Bit-Stream implementation of the rotor current control system.</td>
</tr>
<tr>
<td>7.11</td>
<td>Bit-Stream implementation of the modulator for the RSC.</td>
</tr>
<tr>
<td>7.12</td>
<td>Over- and under-speed detection systems.</td>
</tr>
<tr>
<td>7.13</td>
<td>Simulated response of rotor current control loops to step changes in Q axis current reference.</td>
</tr>
<tr>
<td>7.14</td>
<td>Simulated rotor currents during a speed sweep from 750 RPM to 1250 RPM.</td>
</tr>
<tr>
<td>7.15</td>
<td>The experimental apparatus used to test the RSC and generator.</td>
</tr>
<tr>
<td>7.16</td>
<td>Experimental response of D and Q axis rotor currents to a step change in the Q axis current reference.</td>
</tr>
<tr>
<td>7.17</td>
<td>Response of rotor phase currents during a speed sweep from 750 RPM to 1250 RPM.</td>
</tr>
<tr>
<td>8.1</td>
<td>Circuit diagram of the DFIG system.</td>
</tr>
<tr>
<td>8.2</td>
<td>Block diagram of the proposed control architecuture for the DFIG system.</td>
</tr>
</tbody>
</table>
8.3 Supervisory state machine .................................................. 115
8.4 Single phase equivalent circuit of the WRIM .......................... 116
8.5 Bit-Stream based DFIG excitation control system .................. 117
8.6 Simplified model of the Bit-Stream based speed control loop .... 117
8.7 Response of simplified speed control loop ............................ 118
8.8 Bit-Stream Implementation of the DC link soft start mechanism .. 119
8.9 Bit-Stream implementation of the speed controller .................. 120
8.10 Simulated DC link soft charge procedure ............................ 121
8.11 Simulated synchronisation of the DFIG to the AC grid ............ 122
8.12 Simulated response of the generator to a speed reference step .... 123
8.13 Simulated response of the generator to a turbine torque step ...... 124
8.14 Experimental test results of the DC link soft charge procedure .... 125
8.15 Experimental synchronisation test ................................. 126
8.16 Experimental response of the generator to a speed reference step 127
8.17 Experimental response of the generator to a turbine torque step 128
A.1 Additional vector transformation units ................................. 135
B.1 Isolated voltage and current to Bit-Stream converters ............ 139
B.2 Current-loop-based isolated supply concept .......................... 139
C.1 Trajectory of error signal during operation .......................... 141
C.2 Switching frequency curve for two-level HDBS modulator ....... 142
C.3 Switching frequency curve for three-level HDBS modulator ....... 144
F.1 Clock sources and supervisory control system ........................ 149
F.2 DC link control system .................................................. 150
F.3 Measurement system for GSC ................................. 151
F.4 Current control system for GSC ........................................ 152
F.5 Modulator for GSC .................................................... 153
F.6 Stator voltage and current measurements ............................ 154
F.7 Slip angle calculation system ........................................... 155
F.8 Rotor current measurements ............................................. 156
F.9 Rotor current control system ............................................ 157
F.10 Modulator for RSC ..................................................... 157
F.11 Excitation control system .............................................. 157
F.12 Speed control system: .................................................. 158
List of Tables

2.1 Decomposition of a Bit-Stream Signal into Quanta. ........................................ 6

3.1 Resource Utilisation of Bit-Stream PLL Components ......................................... 31

4.1 Estimation of half bridge output voltage. .......................................................... 42
4.2 Output voltage states and state names of full bridge inverter ............................. 45
4.3 Estimation of full bridge output voltage. ............................................................ 49
4.4 Simulated comparison of SDBS, HDBS and PWM Modulators Driving Half- and Full-Bridge Inverters .......................................................... 51
4.5 Experimental comparison of HDBS and PWM Modulators Driving Half- and Full-Bridge Inverters .......................................................... 51

5.1 Inverter states, output voltages and feedback values ......................................... 56
5.2 Allowable modulator states with respect to operating sector. ............................. 63
5.3 Simulated output current THD levels, average switching frequencies, device temperatures and switching losses of three phase inverter using various Bit-Stream SVM units. .......................................................... 69
5.4 Experimental output current THD levels and average switching frequencies of three phase inverter using various Bit-Stream SVM units. .......................................................... 69
5.5 IEEE1547-2003 Harmonic Current Limits ............................................................ 70

6.1 Grid Side Converter Specifications ................................................................. 74
6.2 Harmonic current measurements, as measured by PA4000 power analyser. .......... 91
6.3 Power loss and efficiency measurements of the GSC at various operating points. .... 91
6.4 Logic consumption of the proposed GSC control system .................................... 92

7.1 Wound Rotor Induction Machine Parameters ..................................................... 94
7.2 Rotor side converter specifications ................................................................. 94
7.3 Logic resource consumption of the proposed control system for the RSC. ............ 109

8.1 Summary of DFIG Parameters ................................................................. 113
<table>
<thead>
<tr>
<th>Section</th>
<th>Table Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.2</td>
<td>DFIG Protection Signals</td>
<td>114</td>
</tr>
<tr>
<td>8.3</td>
<td>Measured Power Factor of Stator Winding</td>
<td>126</td>
</tr>
<tr>
<td>8.4</td>
<td>Logic consumption of the proposed control system for the DFIG.</td>
<td>128</td>
</tr>
<tr>
<td>B.1</td>
<td>Commercially Available $\Sigma - \Delta$ ADCs</td>
<td>138</td>
</tr>
<tr>
<td>B.2</td>
<td>DFIG Measurement Cards - construction and performance.</td>
<td>139</td>
</tr>
<tr>
<td>D.1</td>
<td>Grid side converter parameters</td>
<td>145</td>
</tr>
<tr>
<td>D.2</td>
<td>Bit-Stream parameters for GSC control system</td>
<td>146</td>
</tr>
<tr>
<td>D.3</td>
<td>Phase locked loop parameters for GSC control system</td>
<td>146</td>
</tr>
<tr>
<td>D.4</td>
<td>Controller parameters for GSC control system</td>
<td>146</td>
</tr>
<tr>
<td>E.1</td>
<td>Rotor side converter parameters</td>
<td>147</td>
</tr>
<tr>
<td>E.2</td>
<td>Bit-Stream parameters for the RSC’s control system</td>
<td>147</td>
</tr>
<tr>
<td>E.3</td>
<td>Stator flux estimator parameters</td>
<td>147</td>
</tr>
<tr>
<td>E.4</td>
<td>Slip Angle Calculation Parameters</td>
<td>148</td>
</tr>
<tr>
<td>E.5</td>
<td>Controller parameters for RSC</td>
<td>148</td>
</tr>
</tbody>
</table>
# List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2L</td>
<td>Two-Level</td>
</tr>
<tr>
<td>3L</td>
<td>Three-Level</td>
</tr>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>ADC</td>
<td>Analogue to Digital Converter</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
</tr>
<tr>
<td>CORDIC</td>
<td>COordinate Rotation DIgital Computer</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DDS</td>
<td>Direct Digital Synthesis</td>
</tr>
<tr>
<td>DFIG</td>
<td>Doubly Fed Induction Generator</td>
</tr>
<tr>
<td>DPC</td>
<td>Direct Power Control</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processor</td>
</tr>
<tr>
<td>DTC</td>
<td>Dead Time Compensation</td>
</tr>
<tr>
<td>EMF</td>
<td>Electro-Motive Force</td>
</tr>
<tr>
<td>FOC</td>
<td>Field Oriented Control</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>GaN</td>
<td>Gallium Nitride</td>
</tr>
<tr>
<td>GSC</td>
<td>Grid Side Converter</td>
</tr>
<tr>
<td>HDBS</td>
<td>Hysteretically Down-sampled Bit-Stream</td>
</tr>
<tr>
<td>HDL</td>
<td>Hardware Description Language</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>LCI</td>
<td>Line Commutated Inverter</td>
</tr>
<tr>
<td>L-L</td>
<td>Line to Line</td>
</tr>
<tr>
<td>L-N</td>
<td>Line to Neutral</td>
</tr>
<tr>
<td>LUT</td>
<td>LookUp Table</td>
</tr>
<tr>
<td>LVVRT</td>
<td>Low Voltage Ride Through</td>
</tr>
<tr>
<td>MIMO</td>
<td>Multiple-Input Multiple-Output</td>
</tr>
<tr>
<td>MPPT</td>
<td>Maximum Power Point Tracking</td>
</tr>
<tr>
<td>MRAS</td>
<td>Model Reference Adaptive Subsystem</td>
</tr>
<tr>
<td>NCO</td>
<td>Numerically Controlled Oscillator</td>
</tr>
<tr>
<td>PI</td>
<td>Proportional-Integral</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>PR</td>
<td>Proportional-Resonant</td>
</tr>
<tr>
<td>PSoC</td>
<td>Programmable System on Chip</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>Q</td>
<td>Bit-Stream Quanta</td>
</tr>
<tr>
<td>RMS</td>
<td>Root-Mean-Square</td>
</tr>
<tr>
<td>RPM</td>
<td>Revolutions Per Minute</td>
</tr>
<tr>
<td>RRF</td>
<td>Rotating Reference Frame</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Full Form</td>
</tr>
<tr>
<td>--------------</td>
<td>-----------</td>
</tr>
<tr>
<td>RSC</td>
<td>Rotor Side Converter</td>
</tr>
<tr>
<td>RTOS</td>
<td>Real Time Operating System</td>
</tr>
<tr>
<td>SDBS</td>
<td>Standard Down-sampled Bit-Stream</td>
</tr>
<tr>
<td>SiC</td>
<td>Silicon Carbide</td>
</tr>
<tr>
<td>SISO</td>
<td>Single-Input Single-Output</td>
</tr>
<tr>
<td>SRF</td>
<td>Synchronous Reference Frame</td>
</tr>
<tr>
<td>SVM</td>
<td>Space Vector Modulation</td>
</tr>
<tr>
<td>SVPWM</td>
<td>Space Vector Pulse Width Modulation</td>
</tr>
<tr>
<td>TDD</td>
<td>Total Demand Distortion</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
<tr>
<td>VA</td>
<td>Volt-Amp</td>
</tr>
<tr>
<td>VAr</td>
<td>Volt-Amp reactive</td>
</tr>
<tr>
<td>VHDL</td>
<td>Very high speed integrated circuit Hardware Description Language</td>
</tr>
<tr>
<td>VSCF</td>
<td>Variable Speed Constant Frequency</td>
</tr>
<tr>
<td>VSD</td>
<td>Variable Speed Drive</td>
</tr>
<tr>
<td>VSI</td>
<td>Voltage Sourced Inverter</td>
</tr>
<tr>
<td>WRIM</td>
<td>Wound Rotor Induction Machine</td>
</tr>
</tbody>
</table>
List of Symbols

Symbols for Bit-Stream Systems:

\[ R \] Resolution of Bit-Stream system
\[ N \] Frame length of Bit-Stream system
\[ S \] Generic Bit-Stream signal or complex power
\[ z \] Zero Bit-Stream signal
\[ V_{min}, V_{max} \] Minimum and maximum possible Bit-Stream signal
\[ F_B \] Sampling rate of Bit-Stream signal
\[ F_{MAX} \] Maximum closed loop frequency of Bit-Stream system
\[ S_i \] Input Bit-Stream signal
\[ S_1, S_2 \text{ etc.} \] Input Bit-Stream signal 1, 2 etc.
\[ S_o \] Output Bit-Stream signal
\[ k \] Bit-Stream gain numerator
\[ m \] Bit-Stream gain denominator
\[ K_{Pup}, K_{Pdown} \] Bit stream proportional gain pair
\[ K_{Iup}, K_{Idown} \] Bit stream integral gain pair
\[ K'_I \] Inherent gain of Bit-Stream integrator

Symbols for Generator:

\[ P_M, P_S, P_R \] Mechanical, stator and rotor powers
\[ \tau_M, \tau_E \] Mechanical and electrical torque
\[ \omega_R \] Rotor speed
\[ \omega_{synch} \] Synchronous speed
\[ \omega_S \] Angular speed of stator flux vector
\[ \omega_{slip} \] Slip speed
\[ s \] Slip ratio
\[ P_P \] Number of pole pairs
\[ J \] Generator inertia
\[ V_S \] Stator voltage vector
\[ V_{SA}, V_{SB}, V_{SC} \] Stator phase voltages
\[ V_{S\alpha}, V_{S\beta} \] \( \alpha \) and \( \beta \) axis stator voltages
\[ V_{SD}, V_{SQ} \] D and Q axis stator voltages
\[ I_S \] Stator current vector
\[ I_{SA}, I_{SB}, I_{SC} \] Stator phase currents
\[ I_{S\alpha}, I_{S\beta} \] \( \alpha \) and \( \beta \) axis rotor voltages
\[ I_{SD}, I_{SQ} \] D and Q axis stator currents
\[ R_S \] Stator resistance
\[ L_{LS} \] Stator leakage inductance
List of Symbols

\( e_S \)  
Stator EMF vector

\( \lambda_S \)  
Stator flux vector

\( \lambda_{SD}, \lambda_{SQ} \)  
D and Q axis stator fluxes

\( L_M \)  
Magnetising inductance

\( I_M \)  
Magnetising current vector

\( I_{MD}, I_{MQ} \)  
D and Q axis magnetising currents

\( \lambda_M \)  
Air gap flux vector

\( V_R \)  
Rotor voltage vector

\( I_R \)  
Rotor current vector

\( I_{RA}, I_{RB}, I_{RC} \)  
Rotor phase currents

\( I_{RD}, I_{RQ} \)  
D and Q axis rotor currents

\( I_{RD}, I_{RQ}^* \)  
D and Q axis rotor current references

\( R_R \)  
Rotor resistance

\( L_{LR} \)  
Rotor leakage inductance

\( \lambda_R \)  
Rotor flux vector

\( N_{RS} \)  
Rotor to stator turns ratio

**Generic Symbols:**

\( V \)  
Voltage vector

\( V_A, V_B, V_C \)  
Phase voltages

\( v_\alpha, v_\beta \)  
\( \alpha \) and \( \beta \) axis voltages

\( v_D, v_Q \)  
D and Q axis voltages

\( \theta \)  
Reference angle

\( K_P \)  
Proportional gain

\( K_I \)  
Integral gain

**Symbols for PLL**

\( u_D \)  
Phase detector output

\( u_F \)  
Loop filter output

\( K_D \)  
Phase detector gain

\( K_0 \)  
Oscillator gain

\( \omega_0 \)  
Oscillator center frequency

\( \omega_{osc} \)  
Oscillator frequency

\( \theta_{osc} \)  
Oscillator phase

\( \omega_n \)  
Natural frequency of loop filter

\( \zeta \)  
Damping factor of loop filter

\( \tau_1, \tau_2 \)  
PLL loop filter time constants

\( \Delta F \)  
NCO frequency resolution

\( P_{width} \)  
Width of the NCO phase accumulator

\( F_{out} \)  
Output frequency of NCO

\( F_{word} \)  
NCO frequency word

\( F_{min}, F_{max} \)  
Minimum and maximum NCO frequencies

**Symbols for Bit-Stream Modulators**

\( V_{DC} \)  
DC bus voltage

\( L \)  
Filter inductance
$R_L$  Load resistance  
$I_1$  Fundamental current component  
$I_n$  $n$th harmonic current component  
$F_S$  Average switching frequency  
$v_L$  Voltage across inductor  
$i_L$  Inductor current  
$H$  Modulator threshold parameter  
$h$  Modulator threshold value  
$Lift$  Modulator threshold adjustment parameter  
$e, E$  Modulator error signal  
$v_S$  Output voltage of inverter  
$v_A, v_B, v_C$  Voltage of A, B and C legs of inverter  
$v_\alpha, v_\beta$  $\alpha$ and $\beta$ axis voltages  
$top, bottom, left, right$  Collision signals for single phase or square error boxes  
$i, ii, iii, iv, vi$  Collision signals for hexagonal error box  
$ZL, N, P, ZH, LZL, LN, LP, LZH$  States for single phase modulators  
$A, B, C, D, E, F, ZL, ZH$  States for three phase modulators  
$m$  Modulation index  
$k_{1.73}, k_1, k_{0.866}, k_{0.5}$  Scaling factors for Bit-Stream SVM units

**Symbols for GSC**

$F_G$  Grid frequency  
$\theta_G$  Grid angle  

$V_G$  Grid voltage vector  
$V_GA, V_GB, V_GC$  Grid phase voltages  
$V_G\alpha, V_G\beta$  $\alpha$ and $\beta$ grid voltages  
$V_GD, V_GQ$  D and Q axis voltage of AC grid  

$U_G$  Output voltage vector of GSC inverter  
$U_{GD}, U_{GQ}$  D and Q axis GSC voltage references  

$V_{DC}$  DC link voltage  
$V_{DC}^*$  DC link voltage reference  

$S_G$  Complex power of GSC  
$P_G$  Real power flow into GSC  
$Q_G$  Reactive power flow into GSC  

$I_G$  GSC current vector  
$I_{GA}, I_{GB}, I_{GC}$  GSC phase currents  
$I_{GD}, I_{GQ}$  D and Q axis current of GSC  
$I_{GD}^*, I_{GQ}^*$  D and Q axis current references of GSC  

$L$  Filter inductance
List of Symbols

\( X_L \)  
Line filter impedance

\( L_{LK} \)  
Leakage inductance of transformer

\( C \)  
Filter capacitance

\( R_D \)  
Filter damping resistance

\( C_D \)  
Filter damping capacitance

\( C_C \)  
Common mode filter capacitance

\( R_{CD} \)  
Common mode filter damping resistance

\( C_{CD} \)  
Common mode filter damping capacitance

\( V_{FS} \)  
Voltage measurement full scale

\( K_{VM} \)  
Voltage measurement gain

\( I_{FS} \)  
Current measurement full scale

\( K_{IM} \)  
Current measurement gain

\( K_{VDC} \)  
DC link voltage measurement gain

\( k_{INV} \)  
Combined inverter and modulator gain

\( k_{MOD} \)  
Modulator gain

\( k_{FF} \)  
Grid voltage feed-forward gain

\( k_{DEC} \)  
Cross axis decoupling gain

\( P_{AC} \)  
AC side power of GSC

\( P_{DC} \)  
DC side power of GSC

\( I_{DC} \)  
Equivalent DC current of GSC

\( I_{LOAD} \)  
DC load current applied to GSC

Symbols for RSC and DFIG

\( k_r \)  
Generator torque constant

\( \theta_S \)  
Stator flux angle

\( \lambda_0 \)  
Nominal stator flux magnitude

\( \omega_c \)  
Filter frequency of stator flux estimator

\( k_1, k_2, k_3, k_4 \)  
Gain coefficients for stator flux estimator

\( N_L \)  
Number of encoder lines

\( k_{\theta S} \)  
Stator flux angle measurement gain

\( k_{\theta R} \)  
Rotor angle measurement gain

\( k_{\theta_{slip}} \)  
Slip angle measurement gain

\( N_{MAX} \)  
Full scale of generator speed measurement system

\( N_S \)  
Speed scaling gain

\( N_E \)  
Maximum output pulse rate of angle encoder

\( N_\omega \)  
Maximum output pulse rate of integer to Bit-Stream converter

\( k_\omega \)  
Generator speed measurement gain

\( \omega_X \)  
Rotor speed measurement signal, clumped

\( k_{EXC} \)  
Excitation controller gain
Chapter 1

Introduction

1.1 Background

In recent years it has been accepted that human activities have caused – and continue to cause –
global climate change [1]. Carbon dioxide emissions from the combustion of fossil fuels have been
identified as a major contributor to this climate change and efforts to reduce the consumption
of fossil fuels have focused upon renewable electricity generation, improved energy efficiency and
electrification of transport systems. Many renewable energy generation systems such as solar,
wind, wave and tide require large-scale power electronics to deliver their energy to existing AC
power networks [2]. Of particular interest is wind power, which is a major source of renewable
electricity; as of 2010 approximately 200 GW of wind generation equipment had been installed
worldwide [3]. The DFIG is commonly used in wind generation systems as it offers variable speed
operation – which maximises the energy captured by the wind turbine – without the use of large
power conversion electronics [2, 4, 5, 6]. Power electronics are also central to efforts to improve
the efficiency of energy consumption. The electrification of transport systems such as trains and
automobiles requires compact, highly efficient induction or permanent magnet motors [7, 8]. Efforts
to improve the efficiency of industrial equipment and domestic appliances such as refrigerators and
air conditioners are leading to the adoption of high efficiency electronically driven motors [9]. The
demand for renewable electricity, electric vehicles and more efficient appliances can only be met
with power electronics.

The increasing demand for power electronics has lead to continuous improvement of the
electronics components, converter topologies, and the control algorithms that manage them. Silicon
based semiconductor devices continue to improve, allowing operation at higher voltages [10], currents,
or frequencies [11]. Next-generation devices which employ Silicon Carbide (SiC) [12] or Gallium
Nitride (GaN) [13] are becoming available and their adoption will deliver further improvements in
converter size and efficiency. The controllers used with these devices have likewise improved: simple
analogue control systems such as voltage mode Pulse Width Modulation (PWM) have been replaced
by various digital control schemes ranging from basic digital PWM [14] to model predictive control
[15]. Digital control systems allow the implementation of complex control algorithms without the
problems of DC offsets, parameter drift and component ageing that may affect analogue control
equipment [14].

Digital control techniques are traditionally implemented using microprocessors. The available
microprocessors have improved over time from 8 bit microcontrollers to high speed 32- or 64-bit
Digital Signal Processors (DSPs). Strict timing deadlines must be met when controlling power
electronics applications, so Real Time Operating Systems (RTOSs) may be used to guarantee that high-priority control tasks are completed within the available time. The use of an RTOS requires great care as very subtle mistakes can cause errors which are difficult to debug [16]. Additionally, microprocessors execute instructions sequentially and as both the complexity of control systems and the switching frequency – and therefore sampling frequency – of power electronic systems continues to increase, microprocessor based systems may simply be unable to complete the requisite control calculations within the available time limit.

One potential solution to both software errors and the limitations of processor operating frequency is to implement hardware based control systems using programmable logic devices such as FPGAs. By implementing control functions in dedicated hardware, resources are not shared and many errors that affect microprocessor based systems cannot occur. Additionally, FPGAs can perform many different functions in parallel, so suitably designed hardware control systems may operate at much higher sampling rates than microprocessor based systems [17, 18]. However, the construction of hardware based control systems by manually describing the controller structure using HDLs is difficult and time consuming. The designer must manage many different facets of the design such as signal bus width and synchronising the movement of data throughout the control system [17, 18]. Although formal design methodologies have been published [17], this remains a challenging process. Graphical design tools such as Altera’s DSP Builder [19] and Xilinx System Designer [20] automatically produce code from schematic diagrams and can assist in control system design, but they require proprietary software and are not portable between vendors.

The Bit-Stream control technique was developed to offer a simple and effective method of implementing control systems using FPGAs. Bit-Stream based control systems are constructed by interconnecting appropriate Bit-Stream processing blocks using a schematic editor such as Altera’s Quartus. The use of schematic editing tools greatly simplifies the task of control system development: the control system is laid out graphically in an intuitive manner and, provided suitable function blocks are available, knowledge of HDLs is not required. A description of the Bit-Stream control concept, signal representation and pre-existing library components is given in Chapter 2. The Bit-Stream technique was originally developed for use with neural networks [21, 22, 23], but has been applied to assorted scalar control problems, such as proportional-integral-derivative temperature regulation and mechanical servo control [21, 22, 24, 25]. Bit-Stream control systems are also well suited for use in power electronics applications. Analogue to Bit-Stream conversion can be performed by inexpensive ΣΔ converters, Bit-Stream signals can be used to control power electronics systems without further processing [26] and the very high sampling rates used by Bit-Stream systems eliminate concerns about signal aliasing. Although Bit-Stream control systems for brushless DC motors [27] and basic open-loop control of three phase induction motors [28] have been reported, no Bit-Stream control system employing vector control techniques was reported prior to the research undertaken in this thesis.

1.2 Motivation

In recent years the desire for renewable electricity has lead to the large scale development of wind energy systems. The DFIG topology is frequently employed in wind energy systems and requires complex control systems. Hardware based control systems offer many advantages for power electronics control systems such as truly parallel operation and low latency. However, the development of hardware based control systems is difficult due to the problems of manually writing HDL code to implement the required numerical operations and synchronising the operation of
various processing elements. Traditionally this has required the designer to manually write HDL code specifically for the control system in question while carefully considering the synchronisation of the data as it passes through the control system. In contrast, Bit-Stream control systems can be developed using schematic tools provided by FPGA vendors and synthesised directly into hardware with no intermediate code generation step. This thesis proposes the development of a Bit-Stream based control system for DFIG applications that deliver the advantages of hardware based digital control without requiring complicated design processes.

1.3 Research Objectives

The main objective of this research is to demonstrate the operation of a DFIG system using a Bit-Stream based control system. This control system must actively control the speed of the generator and provide excitation current to the rotor of the machine to maintain unity power factor operation of the generator at the stator terminals. As Bit-Stream control techniques had never been previously applied to vector control problems, this research will also demonstrate that Bit-Stream control systems are suitable for a variety of vector control problems such as the control of motors, generators and grid-connected inverters. A new library of Bit-Stream blocks for vector control applications that is fully compatible with the existing Bit-Stream control libraries will be developed. Each Bit-Stream based control system will be simulated using a simplified continuous time Simulink model and a detailed discrete time Very high speed integrated circuit Hardware Description Language (VHDL) model to demonstrate that Bit-Stream control systems can be reliably designed and simulated using continuous time models in Simulink only. Bit-Stream control of a DFIG will be demonstrated experimentally using a 2.6 kW DFIG prototype.

As the design of the turbine, gearbox and turbine control systems are mechanical engineering problems, the control of the turbine – including Maximum Power Point Tracking (MPPT) – is outside the scope of this thesis.

1.4 Thesis Organisation

The purpose of this thesis is to demonstrate a Bit-Stream based control system for DFIG applications. As the DFIG control system is complex, the Bit-Stream based control system will be developed in stages. This thesis is arranged as follows:

Chapter 2: Control of Doubly Fed Induction Generators. This chapter presents a overview of the operation of the DFIG, followed by a survey of publications on the control of the DFIG. The generator, GSC and RSC are introduced. The principles of vector control are described and applied to the control of the GSC and RSC. The principles, signal representation and pre-existing library of Bit-Stream components are presented. Finally, the specific control system which will be developed throughout this thesis is proposed.

Chapter 3: Bit-Stream Based Phase Locked Loop. A Bit-Stream based PLL for three phase applications is proposed in this chapter. Bit-Stream based Clarke and Park’s Transformation units which are compatible with this PLL are developed. The proposed PLL is simulated and tested experimentally with a three phase AC source. The vector transformation units and PLL are employed in subsequent chapters of the thesis.
Chapter 4: Bit-Stream Modulator for Single Phase Power Electronics Applications.

Although Bit-Stream signals can be directly applied to power electronics, the high frequency nature of Bit-Stream signals may cause excessive switching losses. This chapter proposes and investigates three different modulation techniques which can be used to convert Bit-Stream reference signals into switch control signals for single phase inverters.

Chapter 5: Bit-Stream Modulator for Three Phase Power Electronics Applications.

In this chapter, the single-phase modulator developed in Chapter 4 is generalised and a family of three-phase Bit-Stream modulators is proposed.

Chapter 6: Bit-Stream Control of Grid Side Converter.

This chapter presents a Bit-Stream based control system for a GSC. The control system regulates the voltage of the DC link by adjusting the real power transfer from the AC grid to the DC link. Detailed simulation and experimental results for a Bit-Stream controlled 2 kW GSC are provided.

Chapter 7: Bit-Stream Control of Rotor Side Converter.

A Bit-Stream based control system for the RSC and generator is presented. This control system provides independent control of the generator torque and magnetic flux and is the first reported Bit-Stream based vector control system for electrical machines to be reported in the literature. Detailed simulation and experimental results from a 2.6 kW DFIG under Bit-Stream control are presented.

Chapter 8: Bit-Stream Control of Doubly Fed Induction Generator.

The GSC and RSC are integrated with supervisory control systems in this chapter to develop a complete Bit-Stream based control system for the DFIG. Soft synchronisation, closed loop control of the generator speed and operation with unity power factor at the stator terminals are demonstrated using detailed simulations and experimental testing of a 2.6 kW DFIG system.

Chapter 9: Conclusions and Future Research Opportunities.

This chapter contains concluding remarks and a brief discussion of future research opportunities.

Appendices A – F. Supplemental information is presented in six appendices.
Chapter 2

Control of Doubly Fed Induction Generators

This thesis proposes the development of a hardware-based control system for DFIG applications. The hardware-based control system will be implemented using Bit-Stream techniques as they offer an intuitive, schematic-based approach to control system design. This chapter outlines the methodology that will be employed to develop a Bit-Stream based control system for the DFIG. The Bit-Stream control technique itself and the pre-existing library of Bit-Stream control blocks are described in Section 2.1. The operating principles of DFIGs and induction machines are outlined in Sections 2.2 and 2.3.

DFIG systems require sophisticated control systems in order to operate. A literature survey of control methods for DFIG systems is presented in Section 2.4. An overview of the vector control techniques common to all modern DFIG control systems is given in Section 2.5. Finally, a Bit-Stream based control system for a 2.6 kW DFIG system is proposed in Section 2.6.

2.1 The Bit-Stream Control Technique

The Bit-Stream control technique is used to implement complex control schemes directly in digital logic chips such as FPGAs. The Bit-Stream control technique is different to the conventional hardware-based control techniques laid out by [17] in two respects: the signal representation and the control processing elements.

2.1.1 Representation of Bit-Stream Signals

Standard digital control systems represent signals using ‘words’ of several bits in parallel. These words may be 8 or more bits wide, and require a corresponding number of wires to carry the signal. In contrast, Bit-Stream signals are only one bit wide. This eases the placement and routing of wires at both the board and chip level of a design. However, a single bit signal may only assume the values of 1 or 0, which is not sufficient for high quality control systems.

The Bit-Stream signaling method employs two different mechanisms to allow the transmission of useful signal information. Firstly, Bit-Stream control systems determine the value of a signal by summing the value of a signal over a period of several samples. This is called a frame. The
length of this frame $N$, in samples, is calculated from the desired resolution of the system $R$, in bits, according to (2.1). This allows for the expression of a signal with adjustable resolution.

$$N = 2^R$$  \hfill (2.1)

Secondly, negative values are represented by comparing Bit-Streams to the zero Bit-Stream $z$, which is defined as a series of alternating ones and zeros. A given Bit-Stream signal $S$ can be compared to $z$ and its instantaneous value determined using Table 2.1. Fig. 2.1 shows how the value of a Bit-Stream signal $S$ is determined. Firstly, the signal is compared to $z$ to determine the instantaneous value of the signal: each sample may have a value of +1 quanta (Q), -1 Q or zero. The value of the signal is found by summing the positive and negative quanta within a frame. In Frame A, the signal has a value of +2 Q. In Frame B, the signal has a value of 0 Q.

The maximum expressible range of a Bit-Stream signal is determined by the frame length as follows:

$$V_{\text{max}} = 2^{(R-1)} - 1$$ \hfill (2.2)

$$V_{\text{min}} = -(2^{(R-1)})$$ \hfill (2.3)

where $V_{\text{min}}$ and $V_{\text{max}}$ express the total range of values available to the Bit-Stream signals in Quanta. Because the Bit-Streams are considered as frames, the sampling rate of the Bit-Stream control system must be greater than that of a standard, multiple-bit system. Typically, such multiple bit systems are sampled at twenty or more times the maximum frequency of interest $F_{\text{MAX}}$. However, in order to represent the same signals using Bit-Streams, the sampling rate must be higher such
2.1 The Bit-Stream Control Technique

that twenty complete frames of bits must be sampled in the same period. Therefore the minimum Bit-Stream sampling rate $F_B$ is given by (2.4).

$$F_B \gtrapprox 20 \times F_{MAX} \times N$$  \hspace{1cm} (2.4)

Bit-Stream control systems have been implemented with sampling frequencies ranging from 500 kHz to 5 MHz. While these sampling rates may appear unreasonably high, they confer two major advantages for control system development. Firstly, sampling effects can be ignored by the designer. Secondly, the designer does not need to consider synchronisation between blocks other than the master clock signal $ggclock$ and the reset signal $init$; processing delays are so short that they are negligible.

2.1.2 Bit-Stream Control Elements

Bit-Stream control systems are developed by interconnecting pre-defined blocks. This section describes the general structure of a Bit-Stream addition block to illustrate how Bit-Stream control blocks are developed. Fig. 2.2 shows the internal structure of a Bit-Stream modulator. The modulator is provided with the master clock signal $ggclock$ and the reset signal $init$. The sample clock $gclock$ and zero signal $z$ are generated by dividing $ggclock$ by two and four, respectively. An input signal $S_i$ is decomposed into positive, negative and zero quanta by comparing it with $z$. A ‘saturating sum-and-carry’ or sat_sac unit integrates these quanta on the falling edge of $gclock$. The output of the sat_sac unit is delivered to an integer to Bit-Stream conversion unit, which produces the output signal $S_o$ and is clocked on the rising edge of $gclock$. Further information about the Bit-Stream control technique is available in [21, 26].

An advantage of this approach is that the Bit-Stream control blocks are interconnected using standardised Bit-Stream signals, which simplifies system design. Additionally, Bit-Stream control blocks saturate in an intuitive manner, as opposed to integer-based control systems which may experience overflow errors. The standard Bit-Stream library includes function blocks which perform:

- Addition
- Subtraction
- Scaling
- Integration
Control of Doubly Fed Induction Generators

- Differentiation
- Integer to Bit-Stream conversion
- Bit-Stream to integer conversion
- Proportional - Integral (PI) control
- Fuzzy control tasks
- Neural network tasks

A disadvantage the current Bit-Stream library components approach lies in the clocking scheme. The clocking scheme causes two significant drawbacks. Firstly, \( g\text{clock} \) signals are generated independently within each control block. This produces timing uncertainties as the delays caused by the clock division process vary. Secondly, processing steps are carried out on both the rising and falling edges of the \( g\text{clock} \) signal, which is unusual in FPGA-based designs, where systems almost inevitably operate on the rising edge of the clock signal. The combination of these two factors makes it very difficult to employ standard timing analysis tools to verify that a given design will meet its timing requirements.

2.2 Overview of Doubly Fed Induction Generators

DFIGs are used extensively in wind generation systems because they allow for Variable Speed Constant Frequency (VSCF) power generation while only transferring a fraction of the total electrical power through electronic converters [29].

The basic structure of a typical DFIG system is shown in Fig. 2.3. It consists of a turbine, Wound Rotor Induction Machine (WRIM) and a pair of power electronic converters; the RSC and GSC. The stator of the generator is directly connected to the external AC grid, and the rotor of the generator is connected to the AC grid via the two power converters. The majority of the input power is transferred directly to the AC grid via the stator windings. Only a small fraction of the input power is transferred through the power converters to the grid. This arrangement requires smaller, less expensive power converters than a system which processes the entire power output of the generator using power electronics [29].

The mechanical power input to the generator \( P_M \) is given in (2.5) as the product of the rotor speed \( \omega_R \) and the mechanical torque \( \tau_M \). The sign convention used in this thesis is that positive

![Figure 2.3: A typical DFIG system used in a wind energy application.](image-url)
values correspond to power flowing into the generator, and positive values of torque accelerate the generator while negative values decelerate the generator.

\[ P_M = \omega_R \tau_M \]  

(2.5)

Assuming that the generator speed is constant, and neglecting losses, the electrical torque developed by the generator \( \tau_E \) counteracts the incoming mechanical torque \( \tau_M \), and the sum of mechanical power, stator power \( P_S \) and rotor power \( P_R \) is zero \( \tau_M + \tau_E = 0 \) \( P_M + P_S + P_R = 0 \).

\[ \tau_M + \tau_E = 0 \]  

(2.6)

\[ P_M + P_S + P_R = 0 \]  

(2.7)

The division of power between the stator and rotor windings is dependent upon the rotor speed, synchronous speed \( \omega_{synch} \) and electrical torque. The synchronous speed is determined by the frequency of the grid and number of poles of the machine, as discussed in Section 2.3. The total mechanical power applied to the rotor can be separated into two components; the stator power and the rotor power. As the magnetic fields within the stator windings rotate at the synchronous speed, the stator power is given by:

\[ P_S = \omega_{synch} \tau_E \]  

(2.8)

Under ideal conditions the rotor power is be determined from (2.7) and (2.8):

\[ P_R = -(P_M + P_S) \]  

(2.9)

\[ P_R = - (\omega_{synch} - \omega_R) \tau_E \]  

(2.10)

The difference between the synchronous speed and the rotor speed is known as the slip speed \( \omega_{slip} \):

\[ \omega_{slip} = \omega_{synch} - \omega_R \]  

(2.11)

\[ P_R = - \omega_{slip} \tau_E \]  

(2.12)

Where \( \omega_{slip} \) is the slip speed of the machine. The slip speed can also be expressed as a slip ratio \( s \):

\[ s = \frac{\omega_{synch} - \omega_R}{\omega_{synch}} \]  

(2.13)

Assuming the generator is operated with constant torque, the stator power remains constant according to (2.8). The rotor power is function of the rotor speed according to (2.12). Fig. 2.4 presents these relationships graphically: in both Fig 2.4(a) and 2.4(b) the generator torque, and therefore stator power, is constant. However, in Fig. 2.4(a) the generator operates below synchronous speed, and \( P_M \) is less than \( P_S \). Some power is circulated from the stator windings back to the rotor windings to maintain the overall power balance of the machine. In Fig. 2.4(b) the generator operates above synchronous speed, and electrical power is produced by both the stator and rotor winding and delivered to the AC grid. This ability to extract power from both windings of the generator leads to the term ‘doubly fed.’

The fraction of the total DFIG power which is transferred through the RSC and GSC is approximately equal to the maximum slip ratio of the DFIG system. Typical DFIG platforms operate with slip ratios in the range of ±25% to ±30% [6, 29]. This requires the use of converters with rated powers of approximately one quarter to one third of the total machine rating, which can lead to significant reductions in the size and cost of converters.
2.3 Operating Principles of Induction Machines

DFIGs use WRIMs to convert mechanical energy to electrical energy. This section provides a brief description of the operating principles of induction machines. As comprehensive discussions of the behaviour of induction machines are available from a variety of sources, only a brief description will be given here. In particular, [30] includes descriptions of the machine operation using both electrical and mathematical models.

Fig. 2.5(a) shows a simplified diagram of a WRIM with shorted rotor terminals. The stator windings are fixed to the frame of the machine and do not rotate. The rotor, and therefore the rotor windings, rotate within the machine at the rotor speed \( \omega_R \). Fig. 2.5(b) shows a typical single phase equivalent circuit of the machine. The symbols \( V_S, I_S, R_S, L_{LS} \) and \( \lambda_S \) represent the stator terminal voltage, current, winding resistance, leakage inductance, and flux vector \(^1\) respectively. \( L_M, I_M \) and \( \lambda_M \) represent the magnetising inductance, magnetising current and air gap flux of the machine. The rotor quantities \( V'_R, I'_R, R'_R, L'_LR \) and \( \lambda_R \) represent the equivalent rotor terminal voltage, current, winding resistance, leakage inductance and flux as referred to the stator winding. The voltage source in the rotor circuit represents the Electro-Motive Force (EMF) induced in the rotor windings [30].

The stator voltage is provided by an external AC supply. Current flows through the stator resistance, leakage inductance and magnetising inductance to set up magnetic fluxes within the machine. The magnetic field within the machine can be expressed in terms of the stator flux, air gap flux or rotor flux. The stator flux is found by integrating the stator EMF \( e_S \), which is equivalent to the voltage applied to the stator windings after IR drop is considered (2.15). The air gap flux can be calculated using (2.16).

\[
\lambda_S = \int e_S dt \tag{2.14}
\]

\[
e_S = V_S - R_S I_S \tag{2.15}
\]

\[
\lambda_M = \lambda_S - L_{LS} I_S \tag{2.16}
\]

As \( R_S \) and \( L_{LS} \) are small, the air gap flux of the machine is largely determined by the AC grid voltage. Because the machine is supplied with alternating current, the air gap flux rotates at the

\(^1\) Technically this is actually the flux linkage vector, but the shorter version is more common in the literature.
synchronous speed, which can be calculated from the AC supply frequency $f_G$ and the number of pole pairs of the machine $P_P$:

$$\omega_{\text{synch}} = \frac{2\pi f_G}{P_P} \quad (2.17)$$

The number of pole pairs must be considered because one mechanical rotation of the machine corresponds to $P_P$ electrical revolutions of the stator flux, neglecting slip. As the angular speed of the stator flux – in electrical terms – is set by the AC grid frequency $2\pi f_G$, adjusting the number of pole pairs is a simple but highly effective method for adjusting the speed of the machine, albeit in discrete steps.

The rotor windings of the machine interact with the air gap flux. If the rotor spins at exactly the synchronous speed, the rotor windings rotate at the same rate as the air gap flux; the flux never cuts through the rotor windings and no EMF is produced. In a typical resistor-based speed control application, no external voltage is applied to the rotor windings, and no current flows. As the electrical torque of the machine is developed by the interaction of the rotor and stator currents, no torque is produced at synchronous speed.

If the rotor windings rotate at greater or less than the synchronous speed, they cut through the air gap flux and produce EMF. This EMF causes current to flow through the rotor windings. The interaction of the currents in the stator and rotor produces torque which is dependent upon the rotor speed. Fig. 2.5(c) illustrates a typical relationship between the speed and torque of a
Figure 2.6: Photograph of the WRIM used for the experimental work of this thesis. Open access panels on the right expose the slip rings and brushes.

WRIM with and without additional external rotor resistance. When \( \omega_R \) is less than \( \omega_{\text{synch}} \), the slip is positive and the machine operates as a motor. When the slip is negative the machine operates as a generator. Fig. 2.6 shows the 2.6 kW WRIM which is used as a generator in this thesis. By connecting appropriate external equipment to the rotor windings, the characteristics of the machine can be adjusted. Prior to the development of low cost Variable Speed Drives (VSDs), WRIMs with external resistors were frequently used to provide basic speed control functionality by adjusting the torque-speed characteristic as shown in Fig. 2.5(c). The addition of extra rotor resistance reduced the gradient of the torque-speed curve and therefore reduced the operating speed of the motor. However, the addition of rotor resistance results in lost energy and almost all such machines have been replaced by squirrel-cage induction machines with electronic VSDs [30].

2.4 A Survey of DFIG Control Methods

The control of DFIG systems has been extensively researched over the past 30 years. This section provides a survey of the existing research into DFIG control and discusses the development from original research into the fundamental operation of a DFIG system through to advanced topics such as sensorless operation, operation within unbalanced networks, fault ride-through and stand-alone operation.

2.4.1 Historical Background

Historically, WRIMs with external rotor resistors have been used to provide variable speed operation of fans and pumps. This approach was more efficient than mechanical throttling methods, but clearly less than ideal as energy was dissipated in the external resistors. The Scherbius drive was developed to return energy from the rotor windings to the main AC supply and improve the efficiency of speed controlled WRIMs. The earliest systems used diode rectifiers on the rotor windings and thyristor based Line Commutated Inverters (LCIs) [31]. These systems represented a great improvement in efficiency over resistor-based speed control systems, but could only operate with motors rotating below synchronous speed and included relatively primitive control systems, as the only available control measure was to adjust the firing angle of the LCI.

Thyristor based cycloconverters were applied to the problem and enabled operation in both
the motoring and generating modes. The introduction of a bidirectional converter to the rotor circuit allowed for more sophisticated control of the machine by adjusting the firing angle of the cycloconverter outputs in line with the output of a speed control loop [32]. However, the use of a cycloconverter limited the useful slip ratio of the machine to approximately $\pm 10\%$. This is one of the earliest recorded DFIG systems.

Following this initial demonstration of DFIG operation, the cycloconverter was replaced by back-to-back current source thyristor inverters which increased the slip ratio range to almost $\pm 100\%$ [33]. An improved cycloconverter-based system offered further improvement and operation with a $\pm 50\%$ slip ratio range by coupling the cycloconverter to the grid using a dual-winding stator arrangement [34].

### 2.4.2 Vector Control of DFIGs

The success of the DFIG following the results presented in [33] can be traced to progress in the fields of power semiconductor manufacture, and advances in control theory and hardware. As the technology matured a large number of manufacturers adopted the DFIG topology for wind generation applications [29].

The thyristor based inverters employed in early applications [31, 32, 33] only permit simple control of the generator by varying the device firing angles. Following the development of improved Bipolar Junction Transistors (BJTs) and Insulated Gate Bipolar Transistors (IGBTs), the current-sourced inverters were replaced with back-to-back voltage sourced converters with a DC link capacitor in the majority of applications [35, 36, 37, 38]. One of these converters is connected to the rotor winding of the generator and the other connects to the AC grid via filter inductors. These converters are known as the RSC and GSC. Most DFIG systems employ voltage-sourced converters for the GSC and RSC, with both converters connected to a common DC link. The average output voltages of the RSC and GSC can be finely controlled using Space Vector Pulse Width Modulation (SVPWM) to provide output voltages with adjustable magnitude and phase [39]. Some systems continue to employ cycloconverters, but these are a minority [35, 40, 41].

The advances in power electronics allowed the implementation of more advanced control systems. In the 1990s a large number of DFIG control algorithms which employed voltage sourced converters and active control of the rotor current were investigated. Yamamoto and Motoyoshi [35] propose the control the magnitude and angle of the rotor current vector with respect to the air gap flux; this offers control of the real and reactive power of the DFIG. However, the real and reactive powers are not completely independent of each other and dedicated real and reactive power control loops are required. Bogalecka, and Krzeminski [36] present approaches to decoupling the active and reactive power of the generator, but the mathematical manipulations required to determine the PWM control signals are complex and non-intuitive. Pena et al. [37] present a simple and elegant solution to these problems: the rotor current control system is oriented with respect to the stator flux vector, which naturally provides independent control of the generator torque and flux; the decoupling of the real and reactive power at the stator terminals follows naturally. These control algorithms are collectively known as Field Oriented Control (FOC) methods.

FOC based DFIG systems inevitably use outer-loop control systems to provide current reference signals for the inner-loop control of the rotor current. Many DFIG systems actively control the real and reactive power flow at the stator terminals using these outer control loops, which allows the DFIG to provide reactive power support to the AC grid if required [35, 36, 38, 42]. The GSC can likewise be used for VAr support, phase imbalance correction or harmonic filtering schemes; this is
not specific to DFIG applications and a wealth of literature exists on these topics [43, 44, 45, 46]. In recent years the direct torque control method originally developed for squirrel cage induction machines [47] has been modified for use in DFIG systems [48]. A similar technique known as Direct Power Control (DPC) has also been applied [49, 50, 51]. Direct torque/power control algorithms can provide simpler control systems than FOC methods as they do not employ inner-loop and outer-loop control systems. A disadvantage of these systems is that the rotor currents are not directly controlled and therefore protection features such as rotor current limiting are difficult to implement.

2.4.3 Sensorless operation

Modern DFIG control algorithms require knowledge of the mechanical angle of the generator shaft to properly orient their Park’s Transformations [35, 37, 38, 42, 52]. As rotor angle sensors can increase the cost and decrease the reliability of machine control systems, sensorless techniques have also been pursued. A variety of approaches have been pursued, ranging from the use of PLLs within the DFIG control algorithm itself in a special case of stator voltage oriented control [53] to the use of Model-Reference Adaptive Subsystem (MRAS) observers which provide estimates of the rotor angle to otherwise conventional control systems [54, 55]. A common downside of sensorless control algorithms is that the rotor current must be non-zero to maintain the stability of the observer. The direct torque/power control methods are also suitable for sensorless operation with similar caveats [49].

2.4.4 Operation Within Unbalanced AC Networks

It is well known that unbalanced AC grid voltages or line parameters can cause undesirable effects in electrical machinery such as increased stator losses and torque oscillation [50]. As DFIG based generators are connected to practical power systems, control structures which can operate under conditions of transmission line asymmetry [57], or phase voltage imbalance [58] have been devised. These techniques generally operate alongside existing rotor current control systems, either by adjusting the rotor control parameters or by adding compensation terms at the specific frequency of interest. More aggressive measures which actively counteract phase imbalances by injecting compensation currents from the GSC, and / or RSC into the AC grid have been proposed [59, 60]. DPC type control schemes which are suitable for operation in unbalanced conditions are also present in the literature [50, 51].

2.4.5 Fault Ride Through

A fault in the wider power system to which a DFIG is connected can cause a sudden and severe drop in the grid voltage. Early wind generation systems would disconnect during such faults to prevent damage. This behaviour is undesirable because it results in the loss of generation capacity within the AC grid when it is needed most [4].

In recent years, regulations have been imposed that require wind generators to remain connected to the AC grid during faults [61, 62]. In general, wind generation DFIGs must be capable of performing a Low Voltage Ride Through (LVRT), during which a short circuit in the AC power network near the DFIG results in a drastic reduction of the stator terminal voltage. This reduction
prevents power export from the generator and can cause excessive current flows within the DFIG system or over-voltage of the DC link.

Various measures have been proposed to mitigate these issues using techniques such as rotor current crowbar systems [63, 64] which effectively short-circuit the rotor windings for the duration of the fault. More advanced schemes provide rotor current damping during the fault and retain control of the generator, but require considerable over-rating of the RSC [65]. Additionally, as the grid voltage is low during the fault, the GSC cannot extract energy from the DC link and electronically controlled shunt resistors must be employed to clamp the DC link voltage [66]. Energy storage systems have been proposed for this task [67, 68] but remain an expensive option. The addition of series resistors to the rotor circuit was shown to be an effective measure for reducing the stresses on the machine and RSC in [69]. Research in this area is ongoing.

DFIG systems are also subject to internal faults. In recent years, research into fault-tolerant operation of DFIGs has resulted in schemes to allow continuous operation despite failures of power switches [70, 71] or current sensors [72, 73]. In the most basic terms, fault tolerance is achieved by including redundant components into the DFIG system and rapidly switching out faulted components if required. Gaillard et al. [70] and Karimi et al. [71] both propose the addition of a redundant phase leg to the power electronics assembly. In the event of a fault within one of the main converter legs, the faulted phase leg is connected to the redundant leg by static transfer switches. An FPGA is used to supervise each phase leg and dispatch the redundant phase leg in the event of a fault. Rothenhagen and Fuchs [72] present a method for fault-tolerant current sensing in which an observer is used to estimate the stator and rotor currents of the generator. If the estimated and measured values diverge to an excessive degree, the current sensor in question is deemed to have failed and the observed current signal is used for control instead. A similar scheme is employed by Karimi et al. to provide fault tolerance to the current sensors used to control the GSC [73].

The field of fault tolerant operation is a good example of the advantages of hardware-based control systems; in [71] and [73] FPGAs are used to monitor electronic components on a continuous basis and react to faults within tens of microseconds. This speed of response would be very difficult to attain in a microprocessor-based system. However, the available literature only describes the implementation of the fault tolerance functions within the FPGA; control calculations are performed by an external processor.

### 2.4.6 Stand-Alone Operation

DFIG systems can be operated in stand-alone or islanded power systems. Although this is not a common usage, operation with balanced [52] and unbalanced [59] loads has been demonstrated.

The operation of any generator or power inverter in an islanded situation raises important safety concerns. Most importantly, a safety hazard might exist where personnel are not aware that an isolated section of a power network remains ‘live’ and dangerous. Secondly, the voltage and frequency must be properly controlled to prevent damage to consumer equipment. Thirdly, the islanded grid cannot be connected to an external AC grid without proper synchronisation. A variety of anti-islanding methods have been developed to detect the islanding condition and disconnect generating equipment [74, 75, 76, 77, 78].
2.5 Principles of Vector Control

Although three phase AC systems can be directly controlled on a per-phase basis, such control can be inconvenient as all three phases interact with each other. The term ‘vector control’ refers to using coordinate transformations to convert voltages, currents, fluxes or other signals from their original per-phase signals into vectors, which are more convenient for use in control systems. This section discusses the Clarke and Park’s Transformations of a three phase voltage signal $V_A$, $V_B$, $V_C$, but could also be applied to any other three phase quantity.

The Clarke Transformation is a very common coordinate transformation which is used to convert three phase measurements into a two phase vector. Although each phase’s voltage $V_A$, $V_B$, $V_C$ can be considered as vectors, only their instantaneous values $v_A$, $v_B$ and $v_C$ can be measured, as shown in Fig. 2.7(a).

![Graphical representation of the Clarke Transformation.](a) original measurements of the phase voltages. (b) Output vector of Clarke Transformation.

![Graphical representation of the Clarke Transformation.](a) original measurements of the phase voltages. (b) Output vector of Clarke Transformation.

The Clarke Transformation (2.18) is used to transform these measurements from the three-phase or $abc$ domain into the two-phase vector on the $\alpha\beta$ plane shown in Fig. 2.7(b). The signal $v_0$ is referred to as ‘zero sequence’ voltage and is simply the common mode voltage of the three phases. In a balanced three-phase supply, this voltage is zero, and so the zero sequence calculation is often omitted.

$$
\begin{bmatrix}
  v_\alpha \\
  v_\beta \\
  v_0
\end{bmatrix} = \frac{2}{3} \begin{bmatrix}
  1 & -\frac{1}{2} & -\frac{1}{2} \\
  0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\
  \frac{1}{2} & \frac{1}{2} & \frac{1}{2}
\end{bmatrix} \begin{bmatrix}
  v_A \\
  v_B \\
  v_C
\end{bmatrix}
$$

(2.18)

The use of a Clarke Transformation reduces the three original input signals to a two-dimensional vector; this reduction can significantly simplify the control systems required by a three-phase system. Calculations can be carried out using standard power systems equations, by expressing the measured signals as complex signals:

$$
V = v_\alpha + jv_\beta
$$

(2.19)

Although controllers can operate directly on signals on the $\alpha\beta$ reference frame [14, 79], $v_\alpha$ and $v_\beta$ are AC quantities. If the voltage vector $V$ is plotted on the $\alpha\beta$ plane as shown in Fig. 2.7(b), it rotates at the angular speed $\omega$ of the AC system. To further simplify the signal processing of the
Figure 2.8: Graphical representation of Park’s Transformation.

System, Park’s Transformation can be used to convert $v_\alpha$ and $v_\beta$ from the stationary $\alpha\beta$ reference frame onto a new $DQ$ reference frame, as shown in Fig. 2.8.

$$\begin{bmatrix} v_D \\ v_Q \\ v_0 \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 0 \\ \sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix}$$

(2.20)

Where $v_D$ and $v_Q$ are the components of the voltage vector on the $DQ$ reference frame and $\theta$ is the transformation angle. As noted previously, the zero sequence component is often ignored. Generally $\theta$ is continuously updated such that:

$$\theta = \int \omega dt$$

(2.21)

This causes the $DQ$ reference frame to rotate around the origin at the same speed as the AC input signal; it is therefore known as the Rotating Reference Frame (RRF) or Synchronous Reference Frame (SRF). As the relative positions of the voltage vector and the $DQ$ reference frame remain constant, the signals $v_D$ and $v_Q$ are DC quantities, which can be easier to analyse and manipulate than the same quantities as measured using the $\alpha\beta$ reference frame. Quantities in the $DQ$ reference frame can be expressed as complex vectors and manipulated using standard equations provided that the same reference angle $\theta$ is used for all transformations. Suitable use of Park’s Transformation can result in significant simplifications of control functions, as shown in the following sections.

### 2.5.1 Vector Control of the Grid Side Converter

An excellent application of the principles of vector control is the control of the power flow through a GSC. This section discusses the control of the GSC in general terms; detailed information, simulation results and experimental results are available in Chapter 6.

Fig. 2.9 shows a high-level schematic of the GSC. An external AC grid is connected to the voltage-sourced GSC via a filter inductor. $V_G$, $U_G$ and $I_G$ represent the AC grid voltage, GSC output voltage and converter current flow, respectively. The filter inductors have a complex impedance of $jX_L$. A closed loop current control system regulates the AC grid current. The complex power of the AC grid $S_G$ is given by:

$$S_G = V_GI_G$$

(2.22)

The power flow through the GSC could be controlled using three single-phase current control loops. However, this approach is problematic as the total power transfer through the GSC would
then be dependent on three voltages and three currents. Vector control techniques can be used to vastly simplify the control process. Equation 2.22 can be expanded using the D and Q axis components of the AC grid voltage and current \( V_{GD}, V_{GQ}, I_{GD} \) and \( I_{GQ} \):

\[
S_G = (V_{GD} + jV_{GQ})(I_{GD} - jI_{GQ}) \quad (2.23)
\]

\[
P_G = V_{GD}I_{GD} + V_{GQ}I_{GQ} \quad (2.24)
\]

\[
Q_G = V_{GQ}I_{GD} - V_{GD}I_{GQ} \quad (2.25)
\]

Where \( P_G \) and \( Q_G \) represent the real and reactive power flow from the AC grid to the GSC. A PLL or similar measurement system is used to set the Park’s Transformations’ reference angle \( \theta_G \) such that \( V_G \) lies on the D axis of the DQ reference frame. The following substitutions are made to further simplify the situation:

\[
V_{GD} = |V_G| \quad (2.26)
\]

\[
V_{GQ} = 0 \quad (2.27)
\]

\[
P_G = V_{GD}I_{GD} \quad (2.28)
\]

\[
Q_G = -V_{GD}I_{GQ} \quad (2.29)
\]

From (2.28) and (2.29), the real and reactive power flow from the AC grid to the GSC are independently controlled by \( I_{GD} \) and \( I_{GQ} \), respectively. As \( I_{GD} \) and \( I_{GQ} \) are DC quantities, a simple Proportional-Integral (PI) controller can be used to regulate each current component and therefore the real and reactive power flow. This is a substantial improvement compared to per-phase control; using vector control techniques, the power flow through the GSC can be determined from only one voltage and two currents.

### 2.5.2 Vector Control of Wound Rotor Induction Machines

As previously shown in Section 2.5.1, a salient feature of the vector control method is the ability to independently control two different quantities within a three-phase system. This section discusses the application of field oriented vector control techniques to the control of the WRIM generator within a DFIG system.

The generator torque \( \tau_E \) is calculated from the rotor current vector \( I_R \) and the stator flux vector \( \lambda_S \):

\[
\tau_E = k_r \text{Im} (I_R^* \lambda_S) \quad (2.30)
\]

Where \( k_r \) is the machine torque constant [30].

Equation (2.30) can be expressed in the DQ domain as:

\[
\tau_E = k_r \left(-I'_{RD}\lambda_{SQ} + I'_{RQ}\lambda_{SD}\right) \quad (2.31)
\]
2.5 Principles of Vector Control

By orienting the $DQ$ reference frame with the stator flux vector as shown in Fig. 2.10, the following approximations can be made:

$$\lambda_{SD} = |\lambda_s| \quad (2.32)$$
$$\lambda_{SQ} = 0 \quad (2.33)$$

Therefore (2.31) can be further simplified to (2.34), which offers direct control of the machine torque by adjusting the $Q$ axis rotor current. The exact method for aligning this $DQ$ reference frame is discussed in detail in Chapter 7. The $D$ axis rotor current is aligned with the stator flux vector, and produces no torque. Instead, $I_{RQ}$ influences the magnetic flux inside the machine: positive values reinforce the magnetic flux of the machine and can be used to offset the reactive power of the machine which would otherwise be drawn from the external AC grid.

$$\tau_E = k_r I_{RQ} \lambda_{SD} \quad (2.34)$$

---

$^2$The $DQ$ reference frames used by the control systems of the GSC and RSC are different.
2.6 Proposed DFIG Control Method

As stated in Section 1.2, the purpose of this thesis is to demonstrate a hardware based control system for DFIG applications. The Bit-Stream control technique will be used for this control system as it allows for convenient implementation of hardware based control systems without requiring complicated design processes. A prototype 2.6 kW DFIG system will be constructed and used to test the Bit-Stream based control systems. Back-to-back voltage-sourced converters will be used in this DFIG as they are well understood, can be finely controlled using PWM or similar techniques, and the use of a fixed DC link voltage provides a substantial energy buffer between the rotor and grid side power flows and enhances stability.

This thesis will develop the Bit-Stream control system in stages. Fig 2.11 presents a partially simplified block diagram of the Bit-Stream control system that is proposed in this thesis. As shown in Fig. 2.11 the control system can be divided into three major components: the controller for the GSC, the controller for the RSC and the outer-loop control system.

Prior to the research presented in this thesis, all reported Bit-Stream control systems focused upon scalar control systems or neural networks [23, 24, 25, 26, 27, 28]. Fundamental components required for vector control applications, such as Clarke and Park’s Transformations, were not available. Chapter 3 discusses the development of Bit-Stream based versions of these transformations.

Figure 2.11: Block diagram of proposed Bit-Stream control system for DFIG applications.
and presents a Bit-Stream based three phase PLL. Modulators used to convert Bit-Stream reference signals into PWM-like gate drive waveforms are presented in Chapters 4 and 5.

The new Bit-Stream elements are interconnected as shown in Fig. 2.11 to form a complete control system for the GSC, as discussed in Chapter 6. In Chapter 7 a Bit-Stream based stator flux estimator is proposed, and elements of the control system developed for the GSC are re-used to produce a Bit-Stream based control system for the RSC. Finally, Bit-Stream based outer-loop control systems are proposed to control the speed and excitation of the generator in Chapter 8. The combination of the control systems for the GSC, RSC and generator speed forms a complete Bit-Stream based control system for the DFIG; the aim of this thesis is achieved. This is the first Bit-Stream based control system for a DFIG to be reported in the literature.

2.7 Summary

This chapter provided a brief overview of the Bit-Stream control technique and DFIG topology, followed by description of the behaviour of induction machines and a survey of the existing literature dedicated to the control of DFIG systems. The basic principles of vector control were introduced and applied to the GSC and WRIM. Finally a Bit-Stream based control system for the DFIG was proposed.
Chapter 3

Bit-Stream Based Phase Locked Loop

A key component of the control system for the GSC is a measurement unit which extracts frequency and phase information from the grid voltage waveforms. This chapter presents a PLL developed using Bit-Stream control elements, which offers the advantages of flexibility and versatility combined with comparable performance to existing PLLs. The PLL was chosen over direct calculation and zero crossing methods because it offers superior performance in situations with noisy or distorted line voltages [80].

Direct calculation techniques have been used in the past to determine the instantaneous phase angle of three phase power systems. To determine the phase angle, most approaches convert the three phase voltages $v_{GA}$, $v_{GB}$ and $v_{GC}$ into two phase equivalents $v_{G\alpha}$ and $v_{G\beta}$ and the phase angle is then calculated from the arctangent of $v_{G\alpha} / v_{G\beta}$ [81]. Various types of filtering may be applied to improve the performance of such systems [82]. Zero crossing detectors can also be used to measure frequencies and angles [80]. This approach is relatively simple, but sensitive to noise and distortion, and although alterations have been proposed to improve the performance under such conditions [83], zero crossing detectors can only update their results twice per cycle.

The PLL is favoured for many AC measurement tasks because it avoids these drawbacks. A variety of PLL techniques have been employed for high performance phase angle measurement in power electronics applications [84, 85, 86, 87, 88, 89]. Reference [85] provides an overview of PLL systems specifically intended for tracking three phase electrical supply systems and highlights some of their advantages and disadvantages. Various improvements can be implemented, such as improved filtering [86] to reject noise and harmonics. Reference [87] proposes the use of phase sequence detection systems to reject imbalance conditions or, if very high performance is required, the use of four separate PLLs – one for each phase and then a final unit for post-processing. In this case, the high performance is attained at the expense of considerable resource usage. Techniques have also been implemented for single phase systems to allow for enhanced control of single phase systems [89].

The proposed Bit-Stream based PLL consists of a phase detector, loop filter and numerically controlled oscillator. The proposed PLL demonstrates a simple PLL structure and is suitable for use in GSC control applications. Similar structures are used in MRAS observers [30, 55]. The proposed PLL is modelled with analogue elements using Matlab/Simulink to establish the expected behaviour of a traditional PLL. The analogue design is then converted into Bit-Stream elements and simulated in full detail, using Mentor Graphics’ ModelSim and VHDL models, to demonstrate that the Bit-Stream PLL behaves in much the same manner as the analogue equivalent. The proposed PLL is implemented using an Altera Cyclone II FPGA and experimentally tested. It is
simple and flexible, operates independently of other systems on the FPGA due to the inherently parallel nature of Bit-Stream systems, and consumes fewer logic resources than a ‘soft core’ microprocessor implementation. The following sections describe the structure of the PLL, the Bit-Stream implementations of each block within it, and finally the performance of the PLL as a complete unit.

3.1 Structure of the Phase Locked Loop

The Phase Locked Loop is, as the name implies, a system which locks the phase of an output signal onto the phase of an input signal. The basic structure of a PLL is shown in Fig. 3.1 and consists of a phase detector, loop filter and an oscillator [90]. The required functionality of each block within the Bit-Stream PLL is discussed below. The details of the Bit-Stream implementation are presented in Section 3.2.

![Figure 3.1: Block diagram of the basic PLL system.](image)

3.1.1 Phase Detector

The phase detector of a PLL is used to compare the phase of the input signal and the oscillator to produce a phase error signal \( u_D \). Typical implementations may use multipliers, edge detectors or other more sophisticated techniques. The proposed PLL is intended for use in a three-phase system, therefore a synchronous or rotating reference frame type phase detector is used [80, 85].

The phase detector uses Clarke and Park’s Transformations, as discussed in Section 2.5, to convert the three phase grid voltages \( v_{GA}, v_{GB} \) and \( v_{GC} \) into vector components \( v_{GD} \) and \( v_{GQ} \). While the PLL is in lock, the grid voltage vector lies along the D axis, so \( v_{GD} \) equals the magnitude of the grid voltage and \( v_{GQ} \) equals zero.

The phase detector output \( u_D \) is equal to \( v_{GQ} \). In order to avoid confusion, the phase detector output will only be referred to as \( v_{GQ} \) beyond this point. The output signal of the phase detector is dependent upon the phase error between the grid and local oscillator. The phase detector gain \( K_D \) must be determined so that the loop filter gains can be selected. \( K_D \) is calculated by determining the output of the phase detector as a function of the grid voltage magnitude \( V_G \), grid phase \( \theta_G \) and oscillator phase \( \theta_{osc} \). Firstly, the phase detector output function is derived in polar form to yield (3.1). Secondly, the phase detector gain is written as the ratio of the output signal \( v_{GQ} \) to the phase error \( \theta_G - \theta_{osc} \) to yield the large signal gain, given by (3.2). Finally, the small signal gain is determined by assuming that the phase error is small and substituting \( \sin(\theta) = \theta \) to yield the small signal gain, and is shown in (3.3) to equal the line voltage magnitude.

\[
v_{GQ} = V_G \sin(\theta_G - \theta_{osc}) \quad (3.1)
\]
\[
K_D = \frac{v_{GQ}}{\theta_G - \theta_{osc}} = V_G \frac{\sin(\theta_G - \theta_{osc})}{\theta_G - \theta_{osc}} \quad (3.2)
\]
\[
K_D = V_G \quad (3.3)
\]
3.1 Structure of the Phase Locked Loop

3.1.2 Loop Filter

The loop filter of a PLL takes the error signal $v_{GQ}$ from the phase detector and creates a speed reference signal $u_F$. Loop filters may be implemented in a variety of ways that range from simple proportional gains to lead lag filters to PI controllers to higher order functions. In this case, the PI controller has been selected for the loop filter because it has a theoretically infinite frequency lock range \([90]\), relatively simple transfer function for loop design, and has already been implemented in Bit-Stream systems \([27]\). More complicated loop filter architectures, such as those proposed in \([86]\), could also be implemented using Bit-Stream elements.

The loop filter transfer function is defined as \([90]\):

$$G_C(s) = K_P + \frac{K_I}{s} = \frac{1 + s\tau_2}{s\tau_1}$$  \(3.4\)

Where $K_P$ and $K_I$ are the controller gains, and $\tau_1$ and $\tau_2$ are the equivalent time constants in seconds.

3.1.3 Controlled Oscillator

The controlled oscillator section of the PLL accepts a speed input $u_F$ from the loop filter and generates $\sin(\theta_{osc})$ and $\cos(\theta_{osc})$ signals accordingly. In this case the system is implemented digitally and so a Numerically Controlled Oscillator (NCO) is used.

The behaviour of the NCO is defined as:

$$\omega_{osc} = K_0 u_F + \omega_0$$  \(3.5\)

Where $K_O$ is the NCO gain in radians per second per unit and $\omega_0$ is the output center frequency in radians per second.

3.1.4 Small Signal Equivalent Model

The overall loop gain of the PLL is determined by the product of the phase detector, loop filter and NCO. A small signal model of the PLL is shown in Fig. \(3.2\) \([90]\). The parameter $\omega_0$ has no impact on the small signal behaviour of the system.

In order to set the dynamic performance of the PLL loop filter, the desired bandwidth and damping must be set. Given that the PLL should reject noise from the utility supply, a bandwidth of 5 Hz was chosen, so $\omega_n = 2\pi \times 5 = 31.42$ rad/s. The damping factor $\zeta$ is set to $= 0.7071,$
which provides optimum dynamic response [90]. These values represent a compromise between the response speed of the PLL and its ability to reject noise and disturbances from the utility, and can be tailored to fit a specific application.

The design equations for the PLL are [90]:

\[
\omega_n = \sqrt{\frac{K_0 K_D}{\tau_1}} 
\]

\[
\zeta = \frac{\omega_n \tau_2}{2} 
\]

By rearranging (3.6) and (3.7), the loop filter time constants are found to be:

\[
\tau_1 = \frac{K_0 K_D}{\omega_n^2} 
\]

\[
\tau_2 = \frac{2\zeta}{\omega_n} 
\]

These time constants can be converted into standard loop filter gain terms using (3.4).

As can be seen in (3.6), the bandwidth of the control loop is dependent on the square root of the phase detector gain \( K_D \). In this case, \( K_D \) is determined by the magnitude of the input voltage \( V_{in} \) (3.1), and as such the loop bandwidth will decrease as the line voltage drops.

The following sections discuss the implementation of the phase detector and NCO, and the selection of Bit-Stream gain settings for the PI controller. A summary of these values is shown in Appendix A.

### 3.2 Bit-Stream Implementation of PLL

The following sections discuss the construction of the complete Bit-Stream PLL unit shown in Fig. 3.3. The PLL is constructed out of Bit-Stream processing blocks, which implement a phase detector consisting of a Clarke and Park’s transformation, a standard PI loop filter and an NCO. The PLL design parameters are presented in Appendix [27].

![Figure 3.3: Bit-Stream PLL implementation.](image)

#### 3.2.1 Phase Detector

The phase detector block implements the Clarke and Park’s transformations described in Section 3.1.1 using Bit-Stream elements. Both transformations require matrix multiplication operations, so a special set of vector scaling elements have been developed for Bit-Stream usage.
These vector scaling blocks are extensions of the standard scaling elements described in [20]. The two-input vector scaling block presented in Fig. 3.4 operates by converting the input Bit-Streams \( S_1 \) and \( S_2 \) into integers using their respective scaling factors \( k_1 \) and \( k_2 \). An integrator and feedback element with weighting factor \( m \) operates such that the output signal \( S_o \) is:

\[
S_o = \frac{k_1 S_1 + k_2 S_2}{m}
\]  

(3.10)

Where \( k_1, k_2 \) and \( m \) are integers. Note that while \( k_1 \) and \( k_2 \) may be positive or negative, \( m \) must always be positive so that the feedback loop inside the block is stable. The block can be easily expanded to include more input terms if necessary.

![Two-input Bit-Stream vector scaling block](image)

**Figure 3.4:** Two-input Bit-Stream vector scaling block.

The Clarke Transformation is implemented using two vector scaling elements as shown in Fig. 3.5(a). Because the vector block gains are set by integers, the factor \( \sqrt{3}/2 \) or 0.8660 must be approximated. The gains of the Bit-Stream vector scaling blocks are set by the numerators \( k_1 \) and \( k_2 \) divided by the denominator \( m \). In this case the settings are \( k_1 \) equals 13, \( k_2 \) equals -13 and \( m \) equals 15. This yields a gain of 0.8667 units; the gain error of this approximation is less than 0.1%. The transformation performed by the Clarke Transformation block can be expressed mathematically as:

\[
\begin{bmatrix}
  v_a \\
  v_b \\
  v_c
\end{bmatrix} = \begin{bmatrix}
  \frac{1}{2} & -\frac{1}{2} & 0 \\
  -\frac{1}{2} & \frac{1}{2} & 0 \\
  0 & 0 & 1
\end{bmatrix} \begin{bmatrix}
  v_A \\
  v_B \\
  v_C
\end{bmatrix}
\]  

(3.11)

Compared to the formal Clarke Transformation (2.18), the Bit-Stream implementation has an additional gain of 1.5 units and does not calculate the zero sequence component.

The Parks transformation (2.20) is likewise implemented using two vector scaling blocks as shown in Fig. 3.5(b) but in this case the \( k \) values of the scaling elements are variable: the oscillator provides \( \sin \theta_{osc} \) and \( \cos \theta_{osc} \) as integer words which are used to implement the desired function. The constant NCO MAX AMPLITUDE is set by the designer to match the output amplitude of the oscillator described in Section 3.2.3.

The PLL is intended for use with a 120 V Line-to-Neutral (L-N) Root Mean Square (RMS) AC supply. The line-to-neutral voltages are sensed using Analogue to Digital Converters (ADCs) based on a Programmable System on Chip (PSoC) device from Cypress Semiconductor. These sensors have an isolated analogue front end and a full scale range of 304 V, which corresponds to a voltage measurement gain of 128/304 or 0.42 Q/V. Given an AC input voltage of 120 V

\[\text{As discussed in Chapter }\]

1

the DFIG system is connected to the AC grid at 230 V line-to-line.
RMS L-N, the peak output of the ADCs will be 71 quanta. The Clarke transformation described above has an overall gain of 1.5 units, so the magnitude of the output from the Clarke and Park’s transformations will be approximately 107 quanta. Given (3.3), the small signal gain of the phase detector $K_D = 107$ Q/rad. An alternative Clarke Transformation unit with a gain of 1 unit and in inverse Park’s Transformation are presented in Appendix A.

### 3.2.2 PI Controller

The PI controller uses a predefined Bit-Stream unit similar to the one described in [27]. The settings for this unit are the word width $W_{\text{Width}}$, which is set equal to 8 to match the desired resolution $R$ of the system, and the gains $K_P$ and $K_I$, which are set by numerator / denominator pairs $K_{Pup}$, $K_{Pdown}$, $K_{Iup}$ and $K_{Idown}$, which are all $R$ bit integers.

The selection of the integrator gain setting is complicated by the inherent gain of the integrator, $K'_I$, which is dependent on the effective number of bits $R$ and the sampling rate $F_B$ according to:

$$K'_I = \frac{F_B}{2^R}. \quad (3.12)$$

Therefore the total gain of the integrator is given by:

$$K_I = \frac{K_{Iup}}{K_{Idown}}K'_I. \quad (3.13)$$

A Matlab script was used to determine the most accurate scaling coefficient pairs available for implementing the desired gains of $K_P^* = 1.69$ and $K_I^* = 37.6$. The resulting parameters are listed in Appendix A and result in the actual gains of $K_P = 1.694$ and $K_I = 37.56$. Although the gain parameters have a resolution of only 8 bits, appropriate selections can yield overall gains within 0.3% of the target settings.

### 3.2.3 Numerically Controlled Oscillator (NCO)

An NCO can be implemented in a number of different ways, including Taylor series expansions, COrdinate Rotation DIgital Computer (CORDIC) functions and direct lookup tables [91]. Reference
proposes a NCO using a Bit-Stream based quadrature oscillator, which is not suitable for the proposed PLL as it has no provision for delivering the phase angle itself to other parts of the control system. Therefore the NCO is implemented using a Direct Digital Synthesis (DDS) technique as it is relatively simple, produces good quality output and can deliver exact phase information. A graphical representation of the NCO is shown in Fig. 3.6.

Figure 3.6: Bit-Stream based numerically controlled oscillator.

The exact details of the NCO are implementation specific, depending on the desired sampling rate, frequency resolution and LookUp Table (LUT) size. In this case, the sampling rate \( F_B \) and desired frequency resolution \( \Delta F \) are set to 500 kS/s and 0.05 Hz, respectively. Therefore the width of the phase accumulator \( P_{width} \) in bits is given by:

\[
P_{width} \geq \log_2 \left( \frac{F_B \Delta F}{\pi} \right)
\]  

which yields a word width of 23.3 bits. The NCO has been implemented with a 24 bit phase word, resulting a frequency resolution of \( \Delta F = 0.0298 \) Hz.

The frequency word input to the phase accumulator is adjustable by the designer provided that its number of bits is large enough to hold the maximum frequency word that may be required. The frequency word value \( F_{word} \) can be calculated as:

\[
F_{word} = 2^{P_{width}} \times \frac{F_{out}}{F_B}
\]  

Where \( F_{out} \) is the desired output frequency.

Next, the LUT must be created and filled with pre-calculated sine wave information. A larger LUT may improve the quality of the oscillator output waveforms at the expense of increased memory consumption. As discussed in [92], for optimum performance of the sine wave LUT the number of phase bits \( P \) of the lookup table should be one greater than the number of output bits \( M \). In this case \( M \) is set equal to \( R \) or 8 bits and \( P \) is set to 9 bits or 512 table entries. Whilst it is possible to compress the sine wave LUT in a number of ways [92], and apply various enhancements to improve the purity of output [93], this chapter describes a simple test system, which has not been highly optimized. The current LUT memory usage is 4 kilobits.

In order to interface the Bit-Stream PI controller to the NCO, the Bit-Stream signal \( u_F \) must be converted to a frequency word. This could be accomplished using a Bit-Stream to integer converter and an integer offset function, at the expense of some small number of logic elements and 2\( R \) bits of additional memory usage [21]. Alternatively, a simple but effective method of converting the Bit-Stream to a frequency word is to use the instantaneous value of the Bit-Stream to select between a maximum frequency word and a minimum frequency word. The phase accumulator inside the NCO acts as an integrator and rejects high frequency noise from this process.
Therefore, the only consideration for the NCO input conversion is the desired frequency range. The PLL is intended to operate in 50 Hz systems, and so the frequency range of 45 Hz to 55 Hz was selected, requiring frequency words of \( F_{\text{word}} = 1510 \) and \( F_{\text{word}} = 1845 \) units, respectively. Finally, the gain \( K_0 \) of the NCO must be calculated in order to determine the required loop gains of the PLL. To determine the gain, a given change in the loop filter output is compared to the resultant change in output frequency. Therefore the NCO gain is:

\[
K_0 = \frac{\Delta \omega}{\Delta u_F} = \frac{2\pi (F_{\text{max}} - F_{\text{min}})}{\Delta u_F} = 0.2454
\]  

(3.16)

### 3.3 Simulation Results

To investigate the performance of the proposed PLL, two different types of simulation are performed. Firstly, an idealised model of the PLL is simulated using Matlab/Simulink to determine the expected behaviour of the PLL. This model uses floating-point signal representation and does not include sampling effects. Secondly, a detailed simulation of the Bit-Stream PLL, including finite resolution and sampling effects, is performed using the ModelSim VHDL simulator to show that the Bit-Stream PLL should operate as expected. In both cases, the PLL parameters are those listed in Appendix A and the PLL begins operation 180° out of phase.

Fig. 3.7(a) shows simulated results of the PLL using the Simulink model. Initially \( v_Q \) is zero, but the PLL is not correctly aligned – \( v_{GD} \) is negative rather than positive. Small disturbances cause the PLL to drift away from the 180° phase shift, reducing \( v_{GQ} \). The loop filter reduces the oscillator frequency from \( t \approx 0.1 \) to \( t \approx 0.2 \) seconds to re-synchronise the PLL, then returns to zero after \( t = 0.25 \) seconds. This simulation shows that the PLL is stable and correctly orients the \( DQ \) reference frame with \( v_{GQ} = 0 \). Given an input voltage of 120 V L-N, \( v_{GD} \) stabilises at 107 quanta, in line with value predicted in Section 3.2.1.

Fig. 3.7(b) shows a simulation of the PLL using the ModelSim model, which is written in VHDL
3.4 Experimental Results

and uses all Bit-Stream elements to implement the proposed PLL. As in the previous simulation, the PLL is initially 180° out of phase. The Bit-Stream PLL correctly detects the phase error and re-locks the oscillator onto the line voltage angle with a 0° phase shift. A comparison of Fig. 3.7(a) and Fig. 3.7(b) indicates that the Bit-Stream PLL response is very similar to the idealised PLL response.

3.4 Experimental Results

The proposed Bit-Stream PLL was tested in hardware using an Altera Cyclone II EP2C35F672C6 FPGA, PSoC-based voltage to Bit-Stream converters and a three phase, 50 Hz, 120 V AC supply (L-N). The total logic usage for the PLL is approximately 350 logic elements and 4 kbits of memory as shown in Table 3.1. For comparison, a soft core Nios II processor would consume approximately 700 logic elements and 8-12 kbits of memory [94]. In order to further validate the performance of the proposed PLL, a microprocessor based PLL with the same structure and controller gains has been implemented using a dSPACE DS1104 controller card. Both experimental PLLs have parameters equal to those listed in Appendix A.

Both PLLs were experimentally tested to validate the proposed PLL by synchronising the PLL with an external three phase supply from an initial phase shift of 180°. The experimental results presented in Fig. 3.8(a) demonstrate that the Bit-Stream PLL correctly orients the DQ reference frame so that \( v_{GD} = 86 \, \Omega \) and \( v_{GQ} = 0 \, \Omega \). The measured phase error between the oscillator phase and AC line voltage zero crossing is 2.0°, of which 1° is due to the low pass filtering of the AC line voltage before it is fed to the ADCs. The D axis output voltage is lower than expected – 86 Q instead of 107 Q as calculated previously – and investigation shows that this is due to compression effects of the ADCs.

Fig. 3.8(b) shows the response of the dSPACE-based PLL to the same 180° phase jump. The PLL used the same internal structure and gain settings as the Bit-Stream PLL, and used 12-bit ADCs at a sample rate of 10 kS/sec to obtain an ‘ideal’ response. A comparison between Fig. 3.8(a) and Fig. 3.8(b) shows that the dynamic response of the Bit-Stream PLL largely matches the expected response. Tests with a variable frequency source showed that the PLL is capable of locking onto and tracking frequencies between 47 Hz and 53 Hz.

---

2For this reason, the PSoC-based ADCs were replaced with the AD7401A-based ADCs described in Appendix B.

<table>
<thead>
<tr>
<th>Component</th>
<th>Logic Elements</th>
<th>Memory (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock sources</td>
<td>44</td>
<td>0</td>
</tr>
<tr>
<td>Clarke Transformation</td>
<td>37</td>
<td>0</td>
</tr>
<tr>
<td>Park’s Transformation</td>
<td>84</td>
<td>0</td>
</tr>
<tr>
<td>Loop Filter</td>
<td>157</td>
<td>0</td>
</tr>
<tr>
<td>NCO</td>
<td>27</td>
<td>4096</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>349</strong></td>
<td><strong>4096</strong></td>
</tr>
</tbody>
</table>
3.5 Summary

This chapter described the development a complete Bit-Stream based PLL for use with three-phase systems. The proposed PLL was simulated using Matlab / Simulink to determine the expected, idealised, behaviour of the PLL, which was in accordance with the design equations. The PLL was then simulated again using a detailed VHDL model of the actual Bit-Stream processing blocks, including sampling effects, quantisation and signal propagation delays. The detailed VHDL simulation results were almost identical to the idealised Simulink results, and showed that the Bit-Stream PLL should operate as expected.

The Bit-Stream PLL was then implemented using an Altera brand Cyclone II FPGA and experimentally tested. The Bit-Stream PLL successfully locked onto the three phase line voltage vector - although some compression effects of the ADCs were seen to reduce the measured line voltage amplitude – and showed very similar dynamic behaviour to the previously simulated PLLs. For the purposes of comparison, a microprocessor-based PLL with identical parameters was implemented using a dSPACE DS1104 rapid control prototyping card. The dSPACE PLL exhibited almost identical response to the Bit-Stream PLL, confirming that the Bit-Stream PLL operated as expected.

The Bit-Stream PLL consumed 349 logic elements and 4 kilobits of memory. In contrast,
instantiating a NIOS II embedded processor using the same Cyclone II FPGA would consume at least 700 logic elements and 8 kbits of memory. The Bit-Stream solution offers equivalent performance to a microprocessor-based PLL and consumes fewer hardware resources.
Chapter 4

Bit-Stream Modulators for Single Phase Power Electronics Applications

The one bit wide signals used in Bit-Stream control systems can in some cases be directly applied to power converters [26]. However, the Bit-Streams used in the DFIG control system switch at very high rates – up to several hundred kilo-Hertz. The IGBT-based converters typically used for control of DFIG systems would incur unacceptably high switching losses at these frequencies. One possible way to reduce the switching losses is to simply reduce the sampling rate $F_B$ of the entire control system, but this is not acceptable in many situations as it would entail a significant reduction in either the resolution or bandwidth of the control system. An alternative solution to the problem is to use some form of modulator to convert a given high-frequency Bit-Stream reference signal into a low-frequency switch drive signal.

Traditionally, the conversion from a continuous reference signal into binary switch control signals is performed using PWM. A wide variety of implementations for analog and digital control systems have been devised [14, 95, 96]. Although the exact implementation details differ, PWM units essentially operate by comparing a reference signal to a carrier oscillator waveform. The state of the switch is determined by whether or not the reference is greater or less than the instantaneous value of the carrier. A wide variety of single- and poly-phase PWM schemes have been developed to address concerns such as specific harmonic elimination [97] and voltage balancing in multi-level converters [98].

However, as previously noted, Bit-Stream signals can be directly applied to power electronics. This suggests that a modulator, which simply down-samples or reduces the switching frequency of the reference Bit-Stream, may be possible. This chapter first discusses the behaviour of a Standard Bit-Stream Down-Sampler (SDBS) when used as a modulator and then proposes a Hysteretically Down-sampled Bit-Stream (HDBS) modulator which offers both superior performance and reduced logic consumption. The HDBS modulator is tested experimentally and compared to a standard carrier-based implementation. It is shown that the Bit-Stream down-sampler approach can deliver lower Total Harmonic Distortion (THD) and switching losses than standard PWM solutions. A method for extending the HDBS method to control three-level full-bridge inverters is then proposed and compared to a standard PWM implementation.
4.1 Two Level Bit-Stream Modulators

Three potential methods for the conditioning of high speed Bit-Streams to low speed switch drive signals are proposed in this section. They are: a fixed frequency PWM unit, an SDBS modulator and an HDBS modulator. Each modulator is used to provide switch drive waveforms to the simplified two-level (2L) single phase inverter shown in Fig. 4.1. A sinewave generator based on an NCO, as discussed in Chapter 3, delivers a sinewave reference signal $S_i$ to the modulator under test. This in turn delivers a reduced frequency switching signal $S_o$ to the power electronics. The switch node voltage $v_S$ and inductor current $i_L$ are measured and analysed.

The following sections discuss each method and compare them in terms of output waveform distortion, simulated switching losses and logic resource consumption. In order to provide a fair comparison between each modulator the fundamental frequency $F_1$, modulation index, DC link voltage $V_{DC}$ and average switching frequency $F_s$ are set to 50 Hz, 0.8 p.u., 700 V DC and 3.2 kHz, respectively in all cases. The inverter uses Semikron SKM50GB123D IGBT modules with a fixed dead time of 5 $\mu$s. All of the Bit-Stream modulators discussed in this chapter have a sampling rate $F_B$ of 500 kHz and a resolution $R$ of 8 bits.

4.1.1 Fixed Frequency Pulse Width Modulators

Because PWM is a well understood technique, a triangle-wave regularly sampled PWM unit is used as a benchmark to which the two other modulation techniques can be compared. Fig. 4.2 shows the basic arrangement of a Bit-Stream to PWM unit: the Bit-Stream reference signal $S_i$ is converted to an integer and then compared to a fixed frequency triangular carrier wave to generate an output waveform with constant frequency and variable duty cycle.

The Two-Level (2L) Voltage Sourced Inverter (VSI) shown in Fig. 4.1 was simulated using Matlab/Simulink to represent an ideal PWM inverter with effectively infinite resolution as a benchmark. The use of an ideal modulator allows for conservative comparisons between the PWM and down-sampling methods. The switch voltage and output current waveforms developed by the
4.1 Two Level Bit-Stream Modulators

Figure 4.3: Simulated behaviour of two-level VSI under PWM control. (a) Switch voltage and output current. (b) Output current spectrum.

PWM-controlled VSI are shown in Fig. 4.3(a). As expected, the output current waveform consists of a 50 Hz sine wave with a triangular waveform superimposed on it at the same frequency as the carrier oscillator, in this case 3.2 kHz. The output current spectrum presented in Fig. 4.3(b) shows sharp ‘spikes’ occur around $F_s$, $3F_s$, $5F_s$ etc.

Because it is difficult to compare two different current spectra, a THD measurement is used. The current THD is calculated by comparing the amplitude of the current harmonics to the fundamental current level:

$$THD = \sqrt{\sum_{n=2}^{\infty} \frac{I_n^2}{I_1^2}}$$  \hspace{1cm} (4.1)

Where $I_1$ is the magnitude of the fundamental (50 Hz) current component, and $I_n$ is the magnitude of the $n$th harmonic. Obviously, it is not possible to measure an infinite number of harmonics, and so the output current THD is calculated using a finite number of harmonics. In this chapter, two different THD values are calculated. ‘Low-order’ THD is measured over the first twenty harmonics (50 Hz to 1 kHz) and represents the distortion introduced by the modulator but not the switching frequency components. ‘High-order’ THD is measured over the first two hundred harmonics (50 Hz to 10 kHz) and represents the distortion introduced by the modulator and the inductor current ripple.

The simulated output current waveforms of the PWM-controlled inverter have low-order and high-order output current THD levels of 2.97% and 11.2%, respectively.

The PWM-controlled 2L VSI was tested experimentally using the apparatus shown in Fig. 4.4. The PWM drive signals were provided by a dSPACE DS1104 rapid control prototyping card and delivered to a Semikron brand Semiteach inverter. The dSPACE card represents an ideal PWM controller as it provides very accurate reference signal generation and pulse width modulation. The two level inverter has the same supply voltage, dead time, filter inductance and output load as those used in the simulation. The switch node voltage and inductor current waveforms are measured using a digital oscilloscope, a differential voltage probe and a clamp on current probe.

The resulting current and voltage waveforms are presented in Fig. 4.5(a). The current waveform...
Figure 4.4: Experimental apparatus used for single phase inverter testing.

Figure 4.5: Experimental behaviour of two-level VSI under PWM control. (a) switch voltage $v_S$ (top) and output current $i_L$ (bottom). (b) Output current spectrum.

consists of a 50 Hz sinusoidal current and a triangular ripple current at 3.2 kHz. The harmonic spectrum of the output current, presented in Fig. 4.5(b), shows that the fixed-frequency PWM modulation produces strong spectral peaks at $F_s$, $3F_s$, $5F_s$, etc. This distribution results in low-order and high-order THD levels of 1.97% and 13.3%, respectively. The low-order THD is dominated by the third harmonic current level of 1.53%, whereas the high-order THD is dominated by the carrier frequency and its harmonics. These results are similar to those predicted by the simulation. Potential sources of error include non-linearities of the inductor and variations of the DC link voltage throughout the switching cycle.

A Bit-Stream implementation of the PWM modulator shown in Fig. 4.2 is expected to consume 108 logic elements and 256 bits of memory for a resolution $R$ of 8 bits. The memory bits are required for the Bit-Stream to integer conversion unit.
4.1 Two Level Bit-Stream Modulators

4.1.2 Standard Down-sampled Bit-Stream Modulators

The frequency nature of a Bit-Stream signal can be reduced by down-sampling. The usual approach to down-sampling a Bit-Stream is presented graphically in Fig. 4.6(a). Two clock signals are required: a fast input clock $CLK_A$ and a slower output clock $CLK_B$. An incoming Bit-Stream $S_i$ is compared to the outgoing Bit-Stream $S_o$, and the difference between them is integrated at each cycle of $CLK_A$. The output of the integrator is used to update the output signal $S_o$ for each cycle of $CLK_B$. By choosing $CLK_B < CLK_A$ the number of transitions in the signal can be reduced, thus reducing the switching rate. This approach consumes significantly fewer resources than the Bit-Stream to integer to PWM approach discussed above because there is no need to convert the incoming signal $S_i$ into an integer as the integrator used in the modulator provides a free Bit-Stream to integer conversion.

The SDBS modulator and 2L VSI shown in Fig. 4.1 were simulated using Mentor Graphics’ ModelSim software. The reference generator, DC link voltage etc. are the same as those previously simulated. $CLK_B$ is set to $F_B/37$ or approximately 13.5 kHz to achieve an average switching frequency of 3.3 kHz. Fig. 4.6(b) shows the simulated voltage and current waveforms delivered by this modulation scheme. One key difference between a Bit-Stream down sampler and a standard PWM approach is immediately apparent: the switching frequency varies throughout the 50 Hz line cycle. The simulated output current spectrum, shown in Fig. 4.6(c), is markedly different to that of the PWM controlled inverter discussed above. Instead of a small number of sharp spectral peaks the switching current components are distributed between 1 kHz and 7 kHz: the output current is spread-spectrum. The low-order and high-order THD values are 5.29% and 10.37%, respectively. The the low order THD level is dominated by the third harmonic of the output current waveform: 2.51%.

On closer examination, the down-sampler shown in Fig. 4.6(b) has one very interesting feature when applied to controlling power converters. When controlling a voltage sourced converter, the input signal $S_i$ represents the desired voltage to be applied to the load while the output signal $S_o$ corresponds to the actual voltage applied. The difference between these two signals is integrated to yield an error $e$ by \( (4.2) \). Because the Bit-Stream sampling rate $F_B$ is very high, the signals $S_i$ and $S_o$ can be considered in continuous time. The current through an inductor $i_L$ can be expressed in terms of the voltage across the inductor $v_L$ and its inductance $L$ by \( (4.3) \). The current error $\Delta i_L$ is given by \( (4.4) \) as the integral of the difference between the desired switch voltage $v^*$ and the actual switch voltage $v_S$.

\[
e = \int S_i(t) - S_o(t) \quad (4.2)
\]

\[
i_L = \frac{1}{L} \int v_L(t) + i_L(0) \quad (4.3)
\]

\[
\Delta i_L = \frac{1}{L} \int (v^*(t) - v_S(t)) \quad (4.4)
\]

By substituting $v^*(t) = kS_i(t)$ and $v_S(t) = kS_o(t)$, \( (4.2) \) and \( (4.4) \) can be compared to show that the current error $\Delta i_L$ is directly proportional to the error $e$ of the Bit-Stream down-sampler:

\[
\Delta i_L = \frac{k}{L} \int (S_i(t) - S_o(t)) = \frac{k}{L} \times e \quad (4.5)
\]

Where $k$ is a scaling factor in Volt-seconds per unit. For the half bridge converter shown in Fig. 4.1, $k = V_{DC}/F_B$ and is independent of the resolution $R$ of the controller. Given this relationship between the error $e$ of the modulator and the error in converter output current, the reason for the distorted average output current can be investigated by observing the trajectory of the error signal.
e within the modulator, as shown in Fig. 4.6(d). As expected, the converter output is inverted when the error passes through zero, but the average error is not well controlled, which leads to a distorted average current waveform.

An implementation for the SDBS modulator shown in Fig. 4.6(a) for $R = 8$ bits is expected to consume 53 logic elements and zero bits of memory. The use of an integrator instead of a Bit-Stream to integer conversion removes the need for extensive memory and the lack of a carrier oscillator and simplicity of the compare to zero operator substantially reduce logic consumption.

### 4.1.3 Hysteretically Down-sampled Bit-Stream Modulators

From (4.5) it follows that in order to achieve good control over the converter output current, the error signal $e$ must be suitably controlled. One enhancement to the SDBS modulator discussed above is the use of two comparators to keep $e$ between an upper and lower threshold using hysteresis as shown in Fig. 4.7(a), hence it is called the HDBS modulator. Given that the error signal $e$ is
4.1 Two Level Bit-Stream Modulators

Figure 4.7: Hysteretic Down-sampling Bit-Stream modulator. (a) Modulator structure. (b) Simulated switch voltage and output current waveforms. (c) Simulated output current spectrum.

Figure 4.8: Experimental behaviour of two-level VSI under HDBS control. (a) Switch voltage $v_s$ (top) and output current $i_L$ (bottom). (b) Output current spectrum.

now constrained between $e_{\text{max}} = H$ and $e_{\text{min}} = -H$, the total inductor current ripple $\Delta I_L$ is:

$$\Delta I_L = \frac{k}{L}(e_{\text{max}} - e_{\text{min}}) = \frac{V_{\text{DC}}}{LF_B} \cdot 2H \quad (4.6)$$

The simulated switch voltage and inductor current of the inverter, which has the parameters listed in Section 4.1, using HDBS modulation with $H = 10$ is shown in Fig. 4.7(b). A visual
comparison of Fig. 4.6(b) and Fig. 4.7(b) suggests that the HDBS method introduces less distortion than the SDPS method, which is confirmed by comparing the output current spectra shown in Fig. 4.7(c) – the spectral lines of the HDBS waveform are generally lower in amplitude than their counterparts in the SDPS current spectrum. The switching harmonics are spread over a frequency range of 1 kHz to 6 kHz. The low-order and high-order output current THD levels are 5.69% and 6.24%, respectively: most of the distortion is due to the third harmonic, which is 2.89%.

The proposed 2L HDBS modulator was then tested experimentally using the 2L VSI. The switch voltage and output current shown in Fig. 4.8(a) are similar to their simulated counterparts, indicating that the modulator operates largely as expected, with variable switching frequency and a sinusoidal output current. The measured output current spectrum presented in Fig. 4.8(b) is also similar to the simulation results. The measured low-order and high-order THD levels are 4.32% and 11.4%, respectively – higher than those produced by the inverter under PWM control. The measured third harmonic level is 3.28%, which is close to the predicted value of 2.89%.

An implementation of the 2L HDBS modulator shown in Fig. 4.7(a) for $R = 8$ bits is expected to consume 43 logic elements and zero bits of memory. The absence of either a carrier oscillator or a clock divider results in minimal logic consumption.

### 4.1.4 Dead Time Compensated HDBS Modulator

The 2L HDBS modulator can be easily extended to include Dead Time Compensation (DTC). The addition of DTC improves the quality of the inverter output current - the magnitude of low-order harmonics are reduced without increasing the average switching frequency of the inverter. Whilst the addition of a current control loop would also improve the low-order THD levels, the control system would require either the addition of harmonic compensation loops or a high-gain, high-bandwidth current control loop. In contrast, the DTC technique proposed below is simple and does not require extension of the main control system.

The proposed DTC technique modifies the output feedback signal $S_o$ of the HDBS modulator so that it more accurately reflects the true output voltage of the half bridge $v_S$ as shown in Fig. 4.9(a). The obvious approach in implementation of this compensation is to directly measure $v_S$ in a manner similar to that proposed in [99]. However, this would require the addition of measurement circuitry, which is undesirable because this signal must be suitably conditioned and may require galvanic isolation. Conversely, it is reasonable to assume that the inductor current $i_L$ would be measured for control purposes, and therefore would be available for use in a DTC scheme. Thus the proposed DTC scheme estimates $v_S$ from the gate drive signals and the sign of the inductor current, as shown in Fig. 4.9(a). A dead time block is added to the modulator to provide dead-time protected gate drive waveforms for Q1 and Q2, and an estimator block is placed in the feedback path. Table 4.1 shows the truth table of this estimator.

<table>
<thead>
<tr>
<th>$Q_1$</th>
<th>$Q_2$</th>
<th>$i_L$</th>
<th>Mode</th>
<th>$v_S$</th>
<th>$S_o$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>&lt; 0</td>
<td>Freewheeling</td>
<td>$V_{DC}/2$</td>
<td>+1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>≥ 0</td>
<td>Freewheeling</td>
<td>$-V_{DC}/2$</td>
<td>-1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>Driving</td>
<td>$-V_{DC}/2$</td>
<td>-1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>Driving</td>
<td>$V_{DC}/2$</td>
<td>+1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>Shoot-through</td>
<td>Undefined</td>
<td>Undefined</td>
</tr>
</tbody>
</table>
Figure 4.9: Hysteretic Down-sampling Bit-Stream modulator with dead time compensation. (a) Modulator structure (b) Simulated switch voltage and output current waveforms (c) Simulated output current spectrum.

Figure 4.10: Experimental behaviour of two-level VSI under HDBS control with DTC. (a) Switch voltage $v_S$ (top) and output current $i_L$ (bottom). (b) Output current spectrum.
A simulation of the 2L HDBS modulator with the parameters listed in Section 4.1, DTC and \( H = 10 \) yields the waveforms and output current spectra shown in Fig. 4.9(b) and (c), respectively. The shapes of the voltage and current waveforms are very similar to those of the uncompensated HDBS modulator, but the output current spectrum shows reduced harmonic amplitudes: the third harmonic has dropped from 2.89% without DTC to 0.49%. The simulated low-order and high-order THD levels are 0.99% and 2.56%, respectively.

The results of an experimental test of the proposed dead-time compensated HDBS modulator are shown in Fig. 4.10(a) and (b). The measured low-order and high-order THD levels are 3.13% and 10.2%, respectively. The third harmonic current component is only 1.51%; the addition of DTC has halved the third harmonic level.

### 4.2 Three Level Bit-Stream Modulators

The 2L HDBS modulator is intended for use with half-bridge inverters. However, many inverter applications use full- or H-bridge topologies, similar to that shown in Fig. 4.11. In comparison to the half bridge inverter, the full bridge inverter requires half the DC supply voltage, which reduces switching losses. Four switches are required, and the topology also offers the potential to generate three different output voltages \((-V_{DC}, 0 \text{ and } +V_{DC})\), providing a better trade off between switching frequency/losses and output current THD.

This section proposes a Three-Level (3L) HDBS modulator for full-bridge VSIs, describes a possible DTC implementation and compares both the normal and DTC methods to a fixed-frequency unipolar PWM controlled inverter.

In order to allow for comparisons between the two- and three-level inverters, the DC link voltage has been set to 350 V, while the inductor, load and average switching frequencies remain fixed at 10 mH, 20 \( \Omega \) and approximately 3.2 kHz, respectively. The Bit-Stream control system has a sampling rate \( F_B \) of 500 kHz and a resolution \( R \) of 8 bits.

#### 4.2.1 Three Level HDBS Modulator

This modulator is an extension of the two-level modulator proposed in Section 4.1. The three-level modulator accepts a reference signal \( S_i \) and delivers two output signals: \( S_A \) controls the A leg of the bridge and \( S_B \) controls the B leg of the bridge. The overall bridge output voltage \( V_S \) is:

\[
V_S = V_A - V_B
\]  

(4.7)

Although it is possible to use a two-level modulator as described above and simply setting
$S_B = -S_A$, the resulting system would only be capable of producing a switch voltage $V_S$ of $+V_{DC}$ or $-V_{DC}$, and has equivalent performance to the two-level modulator. A superior solution is to create a new modulator, which deliberately uses both ‘legs’ of the converter in a coordinated manner to produce three different output voltages depending on the values of $S_A$ and $S_B$. Table 4.2 lists the possible output voltages of the bridge before filtering. The states $ZL$, $N$, $P$ and $ZH$ represent the Zero Low, Negative, Positive and Zero High states of both the modulator and inverter. The states $LZL$, $LN$, $LP$ and $LZH$ are discussed later.

<table>
<thead>
<tr>
<th>$S_A$</th>
<th>$S_B$</th>
<th>$V_{OUT}$</th>
<th>State Names</th>
<th>$S_O$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>$ZL$, $LZL$</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>$-V_{DC}$</td>
<td>$N$, $LN$</td>
<td>$-1$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>$+V_{DC}$</td>
<td>$P$, $LP$</td>
<td>$+1$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>$ZH$, $LZH$</td>
<td>0</td>
</tr>
</tbody>
</table>

The proposed three-level HDBS modulator is shown in Fig. 4.12(a). It replaces the simple flip-flop arrangement of the two-level HDBS modulator with a state machine and a suitable feedback unit to transform the bridge state into an appropriate feedback value. The state machine accepts the top and bottom signals from the error comparator and directly controls the VSI. A possible three-level state machine is shown in Fig. 4.12(b). The state values are set such that bit 1 of the state variable is $S_A$ and bit 0 is $S_B$. This arrangement minimises logic consumption by removing the need for dedicated output logic. A converter transfer function block generates $S_O$ to close the HDBS feedback loop, with the feedback values as shown in Table 4.2. As is the case with the two-level HDBS modulator, the threshold value $H$ sets the inductor current ripple. The current ripple is determined by (4.6), where $k = V_{DC}/(2 * F_B)$.

The performance of the proposed full-bridge HDBS modulator is investigated by simulation of a VHDL model of a single-phase full-bridge inverter, configured as shown in Fig. 4.11. The DC supply voltage, reference frequency, output current, inverter dead time and modulator threshold are 350 V, 50 Hz, 10 A RMS, 5 $\mu$s and 15 units, respectively. Fig. 4.13(a) shows the half-bridge output voltages $v_A$ and $v_B$, the bridge output voltage $v_S$ and the inductor current $i_L$ of the inverter. The average switching frequency is 3.3 kHz. Inspection of Fig. 4.13(a) shows that although the inverter employs all three output levels and generates a sinusoidal output current, the ‘B’ arm of the bridge performs most of the switching operations and therefore will experience significantly higher switching losses. Additionally, when the voltage reference is close to the zero crossing points the modulator is prone to switching unnecessarily – particularly between $t = 0.009$ and $t = 0.011$ seconds. This spurious switching is undesirable as it increases the effective switching frequency, and hence switching losses, without improving the quality of the output waveform. In order to improve

![Figure 4.12: Three level HDBS modulator. (a) Structure. (b) State machine.](image-url)
the performance of the modulator, two enhancements are proposed: firstly, the state machine is modified to balance the switching operations across both legs of the bridge; secondly, the error detectors are upgraded to prevent spurious switching.

Balanced switching is achieved by augmenting the original state machine with an additional set of four states $LP$, $LN$, $LZL$ and $LZH$ as shown in Fig. 4.14. The new states have identical output voltages to the original states; the ‘$L$’ prefix of these states indicates that the last state transition switched the A leg of the inverter. The state machine is defined such that the modulator will then preferentially switch the B leg of the inverter when a further state transition is required. This mechanism interleaves switching of the A and B legs of the inverter. The state values are assigned such that ‘$L$’ states are separated by their respective ‘non-$L$’ states by only one bit, so that only the $S_A$ and $S_B$ values need be passed to the bridge and converter transfer function block.

The proposed method of suppressing spurious switching events is derived from analysis of the error signal $e$. Fig. 4.15(a) shows a representative trajectory for the error signal $e$ of the unmodified HDBS modulator during operation. When $e$ reaches the upper threshold $h^+$, the state moves from some zero state $Z$ to the negative state $N$, as expected. The error signal then decreases until $e$

![Figure 4.13](image_url)

**Figure 4.13:** Simulation results for full-bridge VSI with HDBS modulator. (a) Switch node voltages (top), full bridge output voltage and current (middle). (b) Output current spectrum.

![Figure 4.14](image_url)

**Figure 4.14:** State machine for full-bridge VSI with balanced switching losses.
strikes the lower threshold $h^-$, at which point the state moves back to $Z$. However, the quantized nature of the Bit-Stream system causes the instantaneous value of $e$ to fluctuate and once again strike $h^-$, triggering an unnecessary transition to the positive state $P$.

The unnecessary switching events can be addressed by adaptively shifting the error thresholds as shown in Fig. 4.15(b). When $e$ strikes the lower threshold $h^-$, the modulator enters a zero state and $h^-$ is shifted by a small amount such that the noise of $e$ is ignored. Spurious switching is avoided. Once the error signal reaches the upper threshold, the modulator moves out of the zero state and the threshold is restored. The upper and lower thresholds are given by (4.8) and (4.9) and are dependent on the main threshold setting $H$, the state of the modulator and a new parameter $Lift$ which adjusts the amount by which the thresholds move. Simulation and experimental results show that a $Lift$ value of 2 is sufficient to suppress the spurious switching events.

\[
\begin{align*}
    h^+[k+1] &= \begin{cases} 
        H + Lift & \text{state}[k] \in \{ZH, LZL\} \\
        H & \text{state}[k] \notin \{ZH, LZL\}
    \end{cases} \\
    h^-[k+1] &= \begin{cases} 
        -(H + Lift) & \text{state}[k] \in \{ZL, LZH\} \\
        -H & \text{state}[k] \notin \{ZL, LZH\}
    \end{cases}
\end{align*}
\]

(4.8) (4.9)

The 3L HDBS inverter was simulated with the new state machine, a threshold $H$ of 12, and adaptive threshold $Lift$ of 2. Fig. 4.16(a) and Fig. 4.16(b) show the simulated output voltage and current waveforms of the inverter and output current spectrum for the improved full-bridge HDBS modulator. A visual analysis of Fig. 4.16(a) demonstrates that the switching operations are evenly divided between the ‘A’ and ‘B’ legs of the bridge and that spurious switching events have been eliminated. The reduction in spurious switching events allows for the ripple threshold $H$ to be reduced without increasing the average switching frequency. The output current spectrum presented in Fig. 4.16(b) shows that the enhanced modulator has a spread-spectrum output current which is largely confined between 2.5 kHz and 5 kHz. The simulated low-order and high-order THD values for this VSI are 1.64% and 4.71%, respectively.
4.2.2 Dead Time Compensated Three-Level HDBS Modulator

The proposed HDBS modulator can be enhanced by the addition of a dead time compensation scheme similar to that proposed in Section 4.1.4. In order to apply the DTC scheme, two dead time units are added to the outputs of the state machine – one for each inverter arm – and the

Fig. 4.17(a) shows the experimental switch voltage and current waveforms of the 3L HDBS modulator. The output voltages waveform shows that the 3L HDBS modulator provides a three level output voltage and does not experience spurious switching. The output current spectrum shown in Fig. 4.16(b) is similar to the simulated output spectrum, although the magnitudes of the harmonics are somewhat greater. The measured low-order and high-order THD levels are 2.07% and 6.91%.
state feedback unit is replaced by an output voltage estimator. The proposed DTC compensated HDBS modulator is shown in Fig. 4.18(a). The output voltage estimator block consists of a lookup table similar to Table 4.3. An HDBS modulator with DTC was tested experimentally with $H$ and $Lift$ set to 10 and 5 units$^1$, respectively. It has visually identical operating waveforms to those presented previously in Fig. 4.17(a). The output current spectrum, shown in Fig. 4.18(b), has reduced harmonic amplitude. The low-order and high-order output current THD levels are 0.51% and 6.19%, respectively. The 3L HDBS modulator with DTC consumes 155 logic elements.

$^1$An increase in $Lift$ is required to prevent spurious switching during the dead time interval. Typically $Lift = 2 + T_{dead}F_B$. 

<table>
<thead>
<tr>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>Mode</th>
<th>$i_L$</th>
<th>$v_S = v_A - v_B$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Freewheeling</td>
<td>$&lt; 0$</td>
<td>$+V_{DC}$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Freewheeling</td>
<td>$&gt; 0$</td>
<td>$-V_{DC}$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Freewheeling</td>
<td>$&lt; 0$</td>
<td>$+V_{DC}$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Freewheeling</td>
<td>$&gt; 0$</td>
<td>$0$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Freewheeling</td>
<td>$&lt; 0$</td>
<td>$0$</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Freewheeling</td>
<td>$&gt; 0$</td>
<td>$-V_{DC}$</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
<td><strong>Shoot Through</strong></td>
<td>X</td>
<td>Undefined</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Freewheeling</td>
<td>$&lt; 0$</td>
<td>$0$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Freewheeling</td>
<td>$&gt; 0$</td>
<td>$-V_{DC}$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Driving</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Driving</td>
<td>X</td>
<td>$-V_{DC}$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Freewheeling</td>
<td>$&lt; 0$</td>
<td>$+V_{DC}$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Freewheeling</td>
<td>$&gt; 0$</td>
<td>$0$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Driving</td>
<td>X</td>
<td>$+V_{DC}$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Driving</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td><strong>Shoot Through</strong></td>
<td>X</td>
<td>Undefined</td>
</tr>
</tbody>
</table>

**Figure 4.18:** Three-level VSI with dead-time-compensated HDBS modulator.  
(a) Block diagram of modulator. (b) Output current spectrum.
4.2.3 Comparison with Fixed Frequency Three Level PWM

The experimental full-bridge inverter previously described was placed under PWM control with a fixed switching frequency of 3.3 kHz. Fig. 4.19(a) presents the bridge output voltage \(v_S\) and output current \(i_L\) of the converter. The current waveform consists of a 50 Hz sinusoidal current and a triangular ripple current at 3.3 kHz. Strong switching harmonics are present in the output current waveform as shown in Fig. 4.19(b). The measured output current THD levels for low-order and high-order harmonics are 2.12% and 8.35%, respectively.

![Figure 4.19: Experimental behaviour of full-bridge PWM-controlled inverter.](a) Switch voltage \(v_S\) (top) and output current \(i_L\) (bottom). (b) Output current spectrum.

A summary of the simulated performance of the SDBS, HDBS and PWM modulators discussed in this chapter is presented in Table 4.4. The major factor in the performance of the various inverters is the inverter topology. The half-bridge inverter suffers from increased THD levels due to the fact that it only has two output voltage levels, and increased switching losses due to the greater DC link voltage (700 V). The full-bridge inverter has lower THD of the output current due to it having three possible output voltage levels, and reduced switching losses due to the lower DC link voltage (350 V). The total device switching losses are simulated based upon the on, off and reverse recovery loss curves given in the SKM60GB123D datasheet [100].

In the case of the two-level half-bridge inverter, all of the Bit-Stream modulators offer less overall THD than the PWM modulator, because the PWM approach leads to sharp spectral peaks. In terms of low-order THD, the Bit-Stream modulators without DTC yield the highest levels of distortion, followed by the PWM modulator. The HDBS modulator with DTC offers the lowest THD levels. The switching losses are approximately equal in all cases. In the case of the three-level full-bridge inverter, both the normal and DTC HDBS modulators offer the lower THD than the PWM modulator. The addition of DTC elements offers a moderate reduction on THD levels.

A summary of the logical resource consumption and experimental performance of the HDBS and PWM modulators is provided in Table 4.5. When comparing the simulation and experimental results, it is clear that the low-order THD levels predicted by the simulations are quite similar to the experimentally measured values. However, the simulated high-order THD levels are significantly different to their experimentally measured values. This could be due to a variety of factors such as DC bus voltage variations, non-linearities within the iron-cored inductors, or differences in
the calculation of the current spectra: the simulated THD values are calculated using Matlab’s Fast Fourier Transform (FFT) function, while the experimental THD values are calculated using the output current spectral data provided by an Agilent oscilloscope. In both cases a Hanning window was used, and the Resolution Band Width (RBW) is 10 Hz. Although the simulated and experimental THD levels are different in some cases, the rankings of each modulator remain the same. The HDBS modulators without DTC consume the fewest logic resources, followed by the HDBS modulators with DTC. The PWM modulators consume the greatest quantity of logic resources, because they require a memory-intensive Bit-Stream to integer conversion unit.

The topology is an important factor when selecting a modulator. For two-level inverters, the PWM unit is more suitable for driving two-level inverters as it provides lower harmonic currents in the low-frequency range, which are more difficult to filter out. When driving a three-level inverter, both the basic and dead time compensated HDBS units consume fewer logic resources and generate output currents with lower THD than the PWM-controlled inverter. Therefore an HDBS modulator, with or without dead time compensation, is suitable for this role. The maximum and average switching frequencies of the Bit-Stream modulators can be estimated using the formulae presented in Appendix C.

### Table 4.4: Simulated comparison of SDBS, HDBS and PWM Modulators
Driving Half- and Full-Bridge Inverters

<table>
<thead>
<tr>
<th>Inverter Topology</th>
<th>Modulator Type</th>
<th>Dead Time Compensated</th>
<th>( F_s )</th>
<th>LF THD</th>
<th>HF THD</th>
<th>Switching Losses</th>
</tr>
</thead>
<tbody>
<tr>
<td>Half Bridge</td>
<td>SDBS</td>
<td>No</td>
<td>3.2 kHz</td>
<td>5.29%</td>
<td>10.4%</td>
<td>13.3 W</td>
</tr>
<tr>
<td></td>
<td>HDBS</td>
<td>No</td>
<td>3.2 kHz</td>
<td>5.69%</td>
<td>6.24%</td>
<td>16.6 W</td>
</tr>
<tr>
<td></td>
<td>HDBS</td>
<td>Yes</td>
<td>3.2 kHz</td>
<td>0.99%</td>
<td>2.56%</td>
<td>14.0 W</td>
</tr>
<tr>
<td></td>
<td>PWM</td>
<td>No</td>
<td>3.2 kHz</td>
<td>2.97%</td>
<td>11.2%</td>
<td>15.0 W</td>
</tr>
<tr>
<td>Full Bridge</td>
<td>HDBS</td>
<td>No</td>
<td>3.3 kHz</td>
<td>1.64%</td>
<td>4.71%</td>
<td>7.6 W</td>
</tr>
<tr>
<td></td>
<td>HDBS</td>
<td>Yes</td>
<td>3.4 kHz</td>
<td>1.08%</td>
<td>6.41%</td>
<td>8.0 W</td>
</tr>
<tr>
<td></td>
<td>PWM</td>
<td>No</td>
<td>3.3 kHz</td>
<td>1.76%</td>
<td>6.46%</td>
<td>7.7 W</td>
</tr>
</tbody>
</table>

### Table 4.5: Experimental comparison of HDBS and PWM Modulators
Driving Half- and Full-Bridge Inverters

<table>
<thead>
<tr>
<th>Inverter Topology</th>
<th>Modulator Type</th>
<th>Dead Time Compensated</th>
<th>Logic Element Consumption</th>
<th>( F_s )</th>
<th>LF THD</th>
<th>HF THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Half Bridge</td>
<td>HDBS</td>
<td>No</td>
<td>43</td>
<td>3.2 kHz</td>
<td>4.32%</td>
<td>11.4%</td>
</tr>
<tr>
<td></td>
<td>HDBS</td>
<td>Yes</td>
<td>115</td>
<td>3.2 kHz</td>
<td>3.13%</td>
<td>10.2%</td>
</tr>
<tr>
<td></td>
<td>PWM</td>
<td>No</td>
<td>108 elements + 256b memory</td>
<td>3.2 kHz</td>
<td>1.97%</td>
<td>13.3%</td>
</tr>
<tr>
<td>Full Bridge</td>
<td>HDBS</td>
<td>No</td>
<td>81</td>
<td>3.3 kHz</td>
<td>2.07%</td>
<td>6.91%</td>
</tr>
<tr>
<td></td>
<td>HDBS</td>
<td>Yes</td>
<td>155</td>
<td>3.3 kHz</td>
<td>0.51%</td>
<td>6.19%</td>
</tr>
<tr>
<td></td>
<td>PWM</td>
<td>No</td>
<td>170 elements + 256b memory</td>
<td>3.3 kHz</td>
<td>2.12%</td>
<td>8.35%</td>
</tr>
</tbody>
</table>

### 4.3 Summary

This chapter proposed the use of single phase down-sampling modulators to convert high-frequency Bit-Stream reference signals to low-frequency Bit-Stream signals which can be used to control power inverters. A simple test system consisting of a sine wave reference generator, modulator and two-level half bridge inverter is used to investigate three different modulation techniques: PWM, SDBS and HDBS.
The PWM approach is commonly used in digital and analogue control systems, and is used as a benchmark to which the other modulators are compared. The PWM scheme consumes a large number of logic elements because it requires a carrier oscillator and a Bit-Stream to integer conversion unit. Additionally, the spectrum of the output current produced by the PWM controlled inverter has sharp peaks at the switching frequency and its harmonics. These sharp peaks increase the THD of the output current. The SDBS approach converts the high speed reference Bit-Stream to a reduced frequency Bit-Stream by using a separate low frequency clock to down sample the output. It effectively reduces the frequency of the output signal and delivers a spread-spectrum output current, but suffers from zero crossing distortion. The HDBS approach uses a hysteresis bound to perform the down sampling operation. This eliminates the need for a separate resampling clock, delivers spread-spectrum output currents and significantly reduces the amount of zero crossing distortion. An experimental 50 Hz 2 kW half-bridge inverter was constructed and used to test the PWM and HDBS modulators. The HDBS-controlled inverter delivered an output current with less THD than the PWM-controlled inverter. A simple DTC unit was proposed and added to the HDBS modulator. This resulted in a small improvement in the measured THD levels.

The HDBS modulator was then generalised and a three-level modulator for use with full-bridge inverters was proposed. When compared to a three-level PWM unit using a 50 Hz, 2 kW, full-bridge inverter, the HDBS modulator offered superior THD. The DTC method for the half-bridge inverter was extended to the HDBS modulator for the full-bridge inverter and delivered a small improvement in the measured THD levels. The 3L HDBS modulator with DTC consumes the greatest number of logic elements but provides the lowest output current THD levels.
Chapter 5

Bit-Stream Modulators for Three Phase Power Electronics Applications

In order to drive three-phase power electronics applications, a three-phase Bit-Stream to switch modulator is required. Although it is possible to use an independent single-phase modulator for each phase leg of the inverter, the resulting inverter would be limited to a maximum modulation index $m$ of 0.707. Increasing the modulation index beyond this point will cause distortion due to overmodulation (i.e. clipping). In contrast, a single three-phase modulator may coordinate switching between the phases of the inverter using Space Vector Modulation (SVM) and increase this limit to 0.866 [14]. Without increasing the DC link voltage, SVM techniques can deliver 15% more output voltage before saturation occurs.

Conventional power electronics control systems commonly use SVPWM to perform this modulation [14, 95] and research in this area is continuing. Various modifications to the standard method have been proposed, providing methods to: reduce or mitigate distortion and current ripple [101, 102]; provide spread-spectrum operation [103]; and reduce the number of switching operations per cycle [104]. SVPWM is also used as a modulation technique for a variety of inverters, including multi-level inverters [98, 105], inverters with more than three phases [106, 107] and compound inverter topologies [108]. These techniques all rely upon the use of a numerical control unit to generate per-phase or per-sector duty cycle references, which are compared to a carrier oscillator. The use of the SVPWM technique requires a relatively large quantity of logic resources for an FPGA implementation. Additionally, the conversion of Bit-Stream signals into integer signals requires relatively large buffer memories [26]. As such, a carrier-less method is investigated.

In addition to the carrier-based approaches, numerous other modulation techniques have been investigated, including: hysteretic current controllers [109]; direct state selection such as direct torque/power control for motor drives [48] and active rectifiers and power filters [110, 111]; optimum pulse patterns [112]; and model predictive control [15]. These systems are not modulators as such; rather they are a combined modulator and controller. Although they deliver good results, they are not basic building blocks which may be applied to many different designs.

The HDBS modulation technique described in Chapter 4 uses very little hardware because the modulators require neither carrier oscillators nor memory-intensive Bit-Stream to integer conversions. This makes it attractive for use in systems where the size of logic circuitry is a pressing concern and/or spread-spectrum operation is desired. Similar modulator structures have been proposed to address issues with control bandwidth [113] and modulator resolution [114] of DC-DC converters. However, these are not intended for operation in DC to AC inverters or poly-phase
This chapter describes the extension of the single-phase HDBS modulators to a three-phase SVM based HDBS modulator. The Bit-Stream SVM approach is highly adaptable, and so a family of three similar modulators is proposed, each with a particular trade-off between complexity and performance. In contrast to a standard, carrier-based SVPWM system, the Bit-Stream SVM units are carrier-less, produce spread-spectrum output currents, and do not always require a sector detector. The performance of the proposed modulators is assessed by simulation and experimental testing of a 6 kW three-phase inverter driven by an Altera Cyclone II FPGA and compared to the standard, carrier-based, SVPWM technique. Simulation and experimental results show that the proposed Bit-Stream SVM units successfully generate three-phase output current waveforms with spread-spectrum switching components and similar THD to the carrier-based SVPWM.

The proposed family of Bit-Stream based space vector modulators is intended for use in systems similar to that shown in Fig. 5.1(a). The reference system consists of a constant modulation index \( m \) of 0.8 per unit or 102 Q and an inverse Parks’ Transformation unit, which is controlled by an NCO operating at 50 Hz. The reference system delivers a two phase reference \( u_\alpha + j u_\beta \) to the modulator under test. The modulator performs two tasks: firstly, it transforms the reference signal from the two-phase \( \alpha\beta \) domain to the three-phase domain to provide the three phase commands \( S_A, S_B \) and \( S_C \). Secondly, the modulator must limit the average switching frequency of the output signals in order to prevent excessive switching losses in the inverter.

The proposed Bit-Stream SVM units are based on an extension of the single phase HDBS

![Figure 5.1: The proposed Bit-Stream space vector modulator.](a) Test system for the modulator, consisting of a two-phase reference system, modulator and inverter. (b) Structure of the modulator.
Proposed Three-Phase Modulation Method

This section discusses the general structure of the proposed set of Bit-Stream SVM units. The basic components of the modulator are shown in Fig. 5.1(b) and include a two-phase error integrator, which generates an error vector \( E \); an error box, which asserts collision signals when \( E \) exits a defined area; a state machine which accepts these collision signals and controls the state of the inverter accordingly; and an output voltage feedback block, which derives the output voltage in the \( \alpha \beta \) domain from the state machine output.

### 5.1.1 Error Integrators

The error integrator is responsible for measuring the error between the desired output voltage of the inverter and the actual output voltage. The voltage difference is calculated and integrated to produce an error signal \( E \). In this case, the modulator must track the voltage error between the voltage reference signals \( u_\alpha \) and \( u_\beta \) and the applied voltages \( v_\alpha \) and \( v_\beta \), so two integrators are required. The output of the block is an error vector \( E \):

\[
E = k_1 \int \left( u_\alpha + j u_\beta \right) - \left( v_\alpha + j v_\beta \right) dt
\]  

(5.1)

Where \( k_1 \) is an implementation-dependent scaling factor, and is further discussed in Section 5.1.4.

### 5.1.2 Error Box

The error box generates collision signals if the error vector exceeds a defined threshold; it is essentially a two-dimensional comparator. The error vector \( E \) is tested against an adjustable bounding box in the \( \alpha \beta \) domain. If \( E \) is within the box, no collision signals are asserted. If \( E \) is outside the box, one or more collision signals are asserted, and the state machine moves the inverter into a new state in an attempt to return the error vector to the center of the box. The error box can be any reasonable shape, and produce any number of outputs, but the error box must provide error signals which are suitable for use with the chosen state machine. Sections 5.2 and 5.3 of this chapter discuss Bit-Stream modulators based on square and hexagonal boxes, which produce four and six collision signals, respectively.

### 5.1.3 State Machine

The state machine fulfills two purposes: firstly, it directly defines the state of the inverter switches and secondly it contains the necessary algorithm to move between states when one of the collision signals is asserted. The state transition logic is fixed and is not dependent on the input signal \( u_\alpha + j u_\beta \).
Table 5.1: Inverter states, output voltages and feedback values

<table>
<thead>
<tr>
<th>Inverter State (Phase A, B, C)</th>
<th>State Name</th>
<th>Output Voltage (per unit)</th>
<th>Feedback Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>ZL</td>
<td>$0 + j0$</td>
<td>$0$</td>
</tr>
<tr>
<td>100</td>
<td>A</td>
<td>$1 + j0$</td>
<td>$k_1$</td>
</tr>
<tr>
<td>110</td>
<td>B</td>
<td>$0.5 + j0.866$</td>
<td>$k_{0.5}$</td>
</tr>
<tr>
<td>010</td>
<td>C</td>
<td>$-0.5 + j0.866$</td>
<td>$-k_{0.5}$</td>
</tr>
<tr>
<td>011</td>
<td>D</td>
<td>$-1 + j0$</td>
<td>$-k_1$</td>
</tr>
<tr>
<td>001</td>
<td>E</td>
<td>$-0.5 - j0.866$</td>
<td>$-k_{0.5}$</td>
</tr>
<tr>
<td>101</td>
<td>F</td>
<td>$0.5 - j0.866$</td>
<td>$k_{0.5}$</td>
</tr>
<tr>
<td>111</td>
<td>ZH</td>
<td>$0 + j0$</td>
<td>$0$</td>
</tr>
</tbody>
</table>

The states of the state machine directly correspond to the switch state of the inverter. Because the inverter has three phases, each of which can be high or low, there are a total of $2^3$ or 8 states, each of which is assigned a name in Table 5.1 and corresponds to a particular output voltage vector. For example, the state value 100 indicates that the A phase is high, the B and C phases are low and the output voltage is $1 + j0$. The inverter has two states – all phases low and all phases high – which produce a zero voltage output. These states are labeled as ZL and ZH, respectively, and are treated separately in all the state machines proposed.

The state machine logic is derived heuristically by considering the ‘best’ state to move to following an error box collision. As such, desirable behaviours such as only switching one leg of a converter at a time can be obtained by defining appropriate state transitions. In order to maintain the phase of the modulator’s negative feedback loop, the state machine has positive gain in the $\alpha\beta$ plane – collision signals cause the inverter state to move towards the collision.

5.1.4 Output Voltage Feedback

This block is responsible for feeding back the output voltage $v_\alpha + jv_\beta$ to the error integrators. Generally, this block is simply the lookup table presented below as Table 5.1. The constants $k_1$, $k_{0.866}$ and $k_{0.5}$ are fixed scaling values which are used to approximate the desired output voltage vectors. The selection of these values is a compromise between accuracy and internal word lengths.

The opportunity exists to extend the output voltage feedback logic with enhanced functionality such as dead time compensation, device forward voltage compensation and DC link voltage feed-forward. Only the addition of DTC has been investigated in detail.

5.2 The Square-Box Bit-Stream Space Vector Modulator

This section discusses the implementation of an SVM unit using a simple, square, error box. Both the error box and state machine are discussed and the complete modulator is simulated. Experimental measurements of the output current waveforms and spectra are presented to demonstrate that the modulator operates as expected.

The error box used in this case is a square, the size of which is defined by a threshold value $H$. The error box unit delivers collision signals top, bottom, left and right, as defined in (5.3) – (5.6), to the state machine presented in Fig 5.2. Note that in the interests of clarity, only the transitions between states have been shown: when no collision signals are asserted, the machine remains in a constant state. Additionally, in some cases, the collision signal information is augmented by high
and low signals, which are generated from the sign of \( e_{\beta} \). These signals assist in choosing between possible states where the collision signals alone do not provide a definite trajectory, but do not cause transitions.

In order to make effective use of the zero states of the inverter – ZL and ZH – an adaptive threshold \( h \) is employed. When the inverter is in a non-zero state, \( h = k_1 \times H \), and the inverter operates as expected. When the inverter state moves to ZL or ZH, the adaptive threshold is increased by \( k_1 \times Lift \). The value of Lift represents a compromise between the tracking accuracy of the modulator and the effective suppression of spurious switching intervals; higher values of Lift effectively suppress spurious switching events at the expense of slightly increasing output current THD. Experience with single phase HDBS modulators and simulations of the proposed three-phase HDBS modulator have shown that a Lift value of 2 is sufficient to vastly improve the performance of the modulator at low modulation indices. In general terms, \( h \) is determined by the inverter state and the parameters \( H \) and \( Lift \):

\[
h[k+1] = k_1 H + k_1 \begin{cases} 
Lift & \text{state}[k] \in \{ZL, ZH\} \\
0 & \text{state}[k] \notin \{ZL, LH\}
\end{cases} 
\]  

(5.2)

\[
left = e_\alpha < -h 
\]

(5.3)

\[
right = e_\alpha > h 
\]

(5.4)

\[
top = e_\beta > h 
\]

(5.5)

\[
bottom = e_\beta < -h 
\]

(5.6)

The behaviour of the proposed Bit-Stream SVM unit is complex and cannot be readily analysed using analytical methods. As such, the performance of the modulator is assessed through simulations of the complete modulator using VHDL models of the modulator and inverter. In order to assess the performance of the proposed modulator, a complete open-loop inverter is simulated as shown in

Figure 5.2: State machine for the square-box Bit-Stream SVM unit.
The modulation index signal $m$, NCO and Park’s transformation block as described in Chapter 3 are used to develop the $u_\alpha$ and $u_\beta$ reference signals for the SVM unit, and the outputs of the SVM unit drive a discrete-time model of a six-switch three-phase inverter. The inverter parameters are: DC link voltage $V_{DC} = 600$ V, inductance $L = 10$ mH, resistance $R = 20$ Ω and heat sink temperature $T_S = 80^\circ$C. Junction temperature profiles for this inverter are simulated using the PLECS modelling tool with switching loss tables and junction thermal models extracted from the device datasheet. The switches used are Semikron SKM50GB123D devices [100]. The SVM unit under test has a square error box, and parameters $H = 10$, $Lift = 2$, $k_1 = 30$, $k_{0.5} = 15$ and $k_{0.866} = 26$. In practice, the $Lift$, $k_1$, $k_{0.5}$ and $k_{0.866}$ parameters remain the same for all square box HDBS modulators, and only the threshold $H$ is application-dependent.

The simulated switch drive signals, phase currents and selected IGBT junction temperatures for the square-box Bit-Stream SVM unit and inverter are shown in Fig. 5.3(a). As expected, the three phase currents are sinusoidal, have the same magnitude and are phase shifted by 120 degrees from...
5.2 The Square-Box Bit-Stream Space Vector Modulator

Each other. The output current THD levels are calculated as 5.24%, 5.35% and 4.47%, respectively. However, the A phase switches much less frequently the B and C phases – the average switching frequencies of the A, B and C phases of the inverter are 1.9 kHz, 4.1 kHz and 4.3 kHz, respectively. The effect of this imbalance of switching frequencies is clear when the junction temperature curves are compared: Q1 (A phase) remains significantly cooler than Q3 (B phase) and Q5 (C phase). The junction temperature profiles for Q2, Q4 and Q6 are similar to those for Q1, Q3 and Q5, respectively, and are not presented here in the interests of clarity. Q5 experiences the greatest thermal stress, with a maximum junction temperature of 94°C and a temperature cycle of 10.1°C.

Experimental waveforms taken from an inverter with the proposed modulator and identical inverter parameters to those discussed above are presented in Fig. 5.3(b), and show that the proposed modulator successfully delivers sinusoidal, three-phase current to the load. The complete modulator requires only 102 logic elements when synthesised for an Altera Cyclone II FPGA. Measured THD levels for the A, B and C phases are 4.97%, 5.34% and 5.18%, respectively. The differences between the simulated and experimental THD levels may be due to dead time effects, DC bus voltage variations and iron non-linearity due to the use of laminate-iron inductors. Figure 5.3(c) presents measured the output current spectra of the inverter. The highest magnitude harmonic is the fifth, at approximately 2%. The remainder of the output current harmonics are spread between 3 and 6 kHz, with individual amplitudes generally below 1%.

The uneven distribution of switching losses in the inverter is due to the structure of the VHDL code used to implement the state machine: the left and right signals are tested ‘before’ the top and bottom signals and therefore have higher priority, as illustrated in Fig. [5.4(a)]. This in turn causes the $\alpha$ axis – which is closely associated with the A phase – to be more tightly controlled while the $\beta$ axis – which is more closely associated with the B and C phases – is forced to commutate more rapidly. The priority effect becomes particularly obvious when the modulator enters overmodulation; a simulation of the modulator and inverter with $m = 0.95$ indicates that the A phase will switch at a low average frequency of 1 kHz while the B and C phases both switching at over 11 kHz. During periods of overmodulation, the modulator attempts to switch the B and C phases at $F_B/2$ or 250 kHz. The gate drive circuits used in the experimental inverter setup include dead-time protection units which prevent operation at this frequency.
5.3 The Hexagonal-Box Bit-Stream Modulator

The square-box Bit-Stream modulator does not distribute output current distortion and switching losses equally across the three inverter phases. One reason for this is the implicit assignment of priority to the $\alpha$ component of the error vector, as shown in Fig. 5.4(a). Therefore the use of the hexagonal error box shown in Fig. 5.4(b) is proposed. Instead of producing the four output signals, the hexagonal error box produces six output signals $i$, $ii$, $iii$, $iv$, $v$ and $vi$ which indicate that the error vector lies in one of the regions shown in Fig. 5.4(b). The use of a more sophisticated error detector provides non-overlapping output signals, hence removing the priority effect. In addition, the collision signals $i$–$vi$ correspond well to available inverter states and simplify state machine design. The state machine for the hexagonal-box SVM unit is shown in Fig. 5.4(c). Note that, once again, only transitions between different states are shown.

The hexagonal-box SVPWM unit was simulated and tested with an identical inverter to that discussed in Section 5.2. Due to the different implementation of the error box, the modulator parameters are somewhat modified: while both $H$ and $Lift$ remain at 10 and 2 units, respectively, the $\alpha$ and $\beta$ axis variables are scaled differently. The hexagonal error box shown in Fig. 5.4(b) has boundaries lying at 30 degrees to the horizontal $\alpha$ axis. A new axis, $\beta'$ is defined such that $\beta' = \sqrt{3} \beta$, so that the sector boundary lines lie at 45 degrees on the $\alpha\beta'$ plane, which simplifies the collision detection logic. The relevant scaling values have changed to $k_1 = 26$, $k_{0.5} = 13$, $k_{1.73} = 45$, and the collision values $i$–$vi$ are yielded by:

\begin{align*}
    i &= (e_\alpha > h) \& (e_\alpha > |e_\beta|) \\
    ii &= (e_\alpha + e'_\beta > 2h) \& (e_\alpha < e'_\beta) \& (e_\alpha > 0) \\
    iii &= (-e_\alpha + e'_\beta > 2h) \& (-e_\alpha > e'_\beta) \& (e_\alpha < 0) \\
    iv &= (-e_\alpha > h) \& (-e_\alpha > |e'_\beta|) \\
    v &= (-e_\alpha - e'_\beta > 2h) \& (e_\alpha > e'_\beta) \& (e_\alpha < 0) \\
    vi &= (e_\alpha - e'_\beta > 2h) \& (e_\alpha < -e'_\beta) \& (e_\alpha > 0)
\end{align*}

The simulated waveforms of the inverter under hexagonal-box Bit-Stream SVM control with $m = 0.8$ are shown in Fig. 5.5(a). Once again, the phase currents are sinusoidal, have equal amplitudes and are phase shifted by 120 degrees. The simulated output current THD values are 6.40%, 7.04% and 8.45% for the A, B and C phases, respectively; this is a slight increase above the square-box modulator. The simulated switching frequencies for each arm of the bridge are 4.1 kHz, 4.7 kHz and 3.9 kHz for the A, B and C phases, respectively; the switching frequencies are more evenly distributed. The simulated device junction temperature profiles presented in Fig. 5.5(a) show that the switching losses are also more evenly distributed: all devices share a similar maximum temperature and temperature cycle. Q3 experiences the highest thermal stress with a peak temperature of 92°C and a 9.0°C temperature cycle.

The experimental output current waveforms and spectra are presented as Fig. 5.5(b) and (c), respectively. The output currents are sinusoidal and separated by 120°. The experimental THD values are 5.53%, 5.67% and 5.51%. These values are somewhat lower than predicted by the simulation, however when they are compared to the square-box experimental results, the experimental output current THD of the inverter using the hexagonal-box modulator are somewhat increased. The fifth and seventh harmonics are the largest components of the measured THD values.
5.3 The Hexagonal-Box Bit-Stream Modulator

![Diagram](image)

**Figure 5.4:** Influence of the error box on the state machine. (a) Original square box with $\alpha$ axis priority, (b) hexagonal error box with non-overlapping collision regions, (c) state machine for hexagonal error box.

The use of a hexagonal error-box within the SVM unit improves the balance of THD and switching frequency across the phases of the inverter. While the average THD levels and switching frequencies have increased compared to the square-box modulator, which is undesirable, the simulated peak junction temperatures of the switching devices are reduced, indicating reduced switching losses. The average switching frequency of this modulator can be predicted using (C.37) in Appendix C. This function estimates a switching frequency of 4.75 kHz, which is within 10% of the measured average switching frequency. Although (C.37) is intended for use with single phase modulators, it provides a useful approximation of the switching frequency of Bit-Stream SVM units.
Figure 5.5: Operating waveforms of the hexagonal box Bit-Stream SVM unit with $m = 0.8$. (a) Simulated gate control signals, output currents and device junction temperatures. (b) Experimental output currents. (c) Experimental output current spectrum.
5.4 The Sector-Aware Hexagonal-Box Bit-Stream Modulator

This section proposes the addition of a sector-detection block to the SVM unit. Compared to the square-box SVM unit, the hexagonal-box SVM unit offers improved balance between phases of the inverter at the expense of slightly greater switching frequencies and THD levels. This behaviour can be improved by forcing the modulator to use only the states within the relevant sector, as listed in Table 5.2. A sector detector is added to the existing hexagonal-box SVM unit, and the state machine is augmented to take advantage of this extra information. Because the state machine is confined to the sector of interest, the Lift parameter is no longer necessary to encourage the use of the zero states, and so the threshold \( h = H \) is used by the error box at all times.

The simulated waveforms of the inverter under the control of sector-aware SVM unit with \( m = 0.8 \) are shown in Fig. 5.6(a). The inverter parameters are identical to those previously listed. With the exception of Lift, which has been removed, the modulator parameters are identical to those listed in Section 5.3. The simulated output current THD for operation with \( m = 0.8 \) are 6.82\%, 6.84\% and 6.92\%, respectively – between the simulated THD levels for the square-box and hexagonal-box SVM units. The average switching frequencies of the A, B and C phases are 3.0 kHz, 3.1 kHz and 3.4 kHz, respectively. In comparison to the square-box SVM unit, the average switching frequencies are more evenly spread between phases and the average switching frequency is slightly reduced. The simulated device junction temperature profiles, presented in Fig. 5.6(a), show that the switching losses and device thermal stresses are more evenly distributed than in the square-box case. In this case, the devices experience equal thermal stresses, with a maximum junction temperature of 88\°C, and a temperature cycle of 7.1\°C.

The experimental output current waveforms and spectra are presented as Figures 5.6(b) and (c), respectively. The output current waveforms are sinusoidal and separated by 120\°. The experimental output current THD levels are 5.47\%, 5.04\% and 5.06\% for the A, B and C phases, respectively, with the highest harmonic level occurring at the fifth harmonic. These values lie between the square-box and hexagonal-box SVM units.

The addition of the sector detector significantly increases the logic consumption of the SVM unit: 462 logic elements are required, along with 512 bits of memory which are used to convert the reference Bit-Streams \( u_\alpha \) and \( u_\beta \) into integers prior to the sector detector.

<table>
<thead>
<tr>
<th>Sector</th>
<th>Allowable States</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>A, B, ZL, ZH</td>
</tr>
<tr>
<td>2</td>
<td>B, C, ZL, ZH</td>
</tr>
<tr>
<td>3</td>
<td>C, D, ZL, ZH</td>
</tr>
<tr>
<td>4</td>
<td>D, E, ZL, ZH</td>
</tr>
<tr>
<td>5</td>
<td>E, F, ZL, ZH</td>
</tr>
<tr>
<td>6</td>
<td>F, A, ZL, ZH</td>
</tr>
</tbody>
</table>

Table 5.2: Allowable modulator states with respect to operating sector.
Figure 5.6: Operating waveforms of the sector-aware hexagonal box Bit-Stream SVM unit with $m = 0.8$. (a) Simulated gate control signals, output currents and device junction temperatures. (b) Experimental output currents. (c) Experimental output current spectrum.
5.5 The Hexagonal-Box Bit-Stream Modulator with Dead Time Compensation

The Bit-Stream SVM units discussed in this chapter all produce inverter output currents with spread-spectrum characteristics. However, inverter output currents produced by all three modulators have relatively large harmonic components at the fifth and/or seventh harmonics. This section proposes a DTC system for use with Bit-Stream SVM units with the aim of reducing the magnitudes of these harmonics and therefore reducing the overall THD. This system operates on very similar principles to the single phase DTC schemes proposed in Chapter 4. The proposed scheme aims to improve the quality of the inverter’s output currents by providing better output voltage feedback to the error integrators. This is achieved by extending the standard modulator as shown in Fig. 5.7. A dead time unit has been added to each phase to provide a precise 5 \mu s dead time. The signals \hat{v}_A, \hat{v}_B, and \hat{v}_C represent the estimated output voltages of the A, B, and C phases of the inverter, respectively: each voltage estimate is performed using an output voltage estimator unit, as outlined in Section 4.1.4. The estimated inverter state is then fed back to the error integrators through the output voltage lookup table.

The simulated waveforms of the inverter under the control of the SVM unit with DTC and \( m = 0.8 \) are shown in Fig. 5.8(a). The inverter parameters are identical to those previously listed. The modulator parameters are identical to those listed in Section 5.3. The simulated output current THD for operation with \( m = 0.8 \) for the A, B, and C phases are 5.01%, 4.94% and 4.93%, respectively. The average switching frequencies of the A, B and C phases are 4.3 kHz, 4.5 kHz and 4.1 kHz, respectively. In comparison to the square-box SVM unit, the average switching frequencies are more evenly spread between phases and the average switching frequency is slightly reduced. The simulated device junction temperature profiles, presented in Fig. 5.8(a), show that the switching losses and device thermal stresses are similar to those experienced when using the sector-aware modulator. In this case, Q1 experiences the greatest thermal stress, with a maximum junction temperature of 90°C, and a temperature cycle of 7.9°C. The total switching losses are estimated to be 37 W, which is very similar to those experienced by the hexagonal-box SVM unit without DTC.

The experimental output current waveforms and spectra are presented as Figures 5.8(b) and (c), respectively. The output current waveforms are sinusoidal and separated by 120°. The experimental output current THD levels are 3.60%, 3.51% and 3.51% for the A, B and C phases, respectively, with the highest individual harmonic level of 1.15% occurring at the fifth harmonic. The hexagonal-box SVM with DTC offers the lowest output current THD of all the modulators presented in this chapter. However, the addition of the dead time modules to the modulator increases the number of logic elements required to 505.
Figure 5.7: Schematic of the proposed Bit-Stream SVM with DTC.

Figure 5.8: Operating waveforms of the hexagonal box Bit-Stream SVM with DTC and $m = 0.8$. (a) Simulated gate control signals, output currents and device junction temperatures. (b) Experimental output currents. (c)
5.6 Operation of Bit-Stream Space Vector Modulators in Overmodulation Region

During periods of overmodulation, the proposed Bit-Stream modulators experience a sharp increase in average switching frequencies. This increase is fundamentally due to the fact that, during overmodulation, the inverter cannot produce the desired output voltage vector. Therefore the error vector $E$ will remain outside the boundary of the error box, and the state machine will attempt to change the inverter output state.

When the error vector lies some distance away from the boundary between two error regions, the state machine cannot improve the error vector by switching between inverter states, and so no switching occurs.

When the error vector lies close to the boundary between two error regions, the state machine may change the inverter state. This new state will then cause the error vector to shift from one error region to the next. At the next execution step, the state machine will then revert to the original state. This cycle will repeat a number of times, and causes a burst of very rapid switching events.

Taken together, these two behaviours create a characteristic behaviour consisting of periods of no or low frequency switching interspersed with bursts of very rapid switching. It may be possible to detect this behaviour using a supplementary state machine and then apply mitigation measures to restrict the maximum switching frequency, but this solution has not been investigated.

5.7 Space Vector Pulse Width Modulation

SVPWM is a very common technique for controlling three-phase inverters. This section compares the proposed Bit-Stream modulator to a standard fixed-frequency SVPWM implementation, and considers two criteria: output current THD and projected consumption of logic elements and memory within an FPGA.

A carrier-based fixed-frequency SVPWM unit is used to drive the inverter for the purposes of comparison. The inverter parameters remain unchanged, and the SVPWM unit is operated with the same average switching frequency as the sector-aware hexagonal-box SVM unit: 3.2 kHz. Fig. 5.9(a) presents simulated switch drive waveforms, output currents and device junction temperatures for operation at $m = 0.8$. It is seen that all phases switch at the same frequency and experience similar junction temperature profiles.

The experimental output current waveforms and spectra are shown in Fig. 5.9(b) and (c), respectively. The output currents have equal magnitudes and are separated by 120°, as expected. The spectral content of each output current phase is very similar, and exhibits the sharp spectral peaks usually associated with carrier-based modulation schemes. The experimental output current THD values for operation with $m = 0.8$, $m = 0.95$ and $m = 0.2$ are 5.13%, 4.94% and 16.2%, respectively.

The implementation of a similar SVPWM unit for a Bit-Stream control system would consume 441 logic elements and 512 bits of memory: greater than the square- and hexagonal-box Bit-Stream

\[\text{THD} \implies \text{low frequency switching} \]
5.8 Discussion

Three Bit-Stream based and one carrier-based space vector modulation techniques for the control of a three-phase inverter have been simulated and tested experimentally. Each modulation technique offers a different balance between modulator complexity and performance. Tables 5.3 and 5.4 present summaries of the simulated and experimental behaviour of each modulator, respectively.

The following discussion considers operation with a modulation index \( m \) of 0.8 per unit. The square-box SVM unit offers the lowest logic consumption of only 102 logic elements, which makes it attractive for use in applications where logic resources are at a premium. However, this modulator
Table 5.3: Simulated output current THD levels, average switching frequencies, device temperatures and switching losses of three phase inverter using various Bit-Stream SVM units. $H = 10$ for all HDBS modulators.

<table>
<thead>
<tr>
<th>Modulator Type</th>
<th>Modulation Index</th>
<th>Output Current THD (%)</th>
<th>Average switching frequency (kHz)</th>
<th>Max $T_J$ ($^\circ$C)</th>
<th>Max $\Delta T_J$ ($^\circ$C)</th>
<th>Switching losses (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Square box HDHS</td>
<td>0.80</td>
<td>5.24 5.35 4.47</td>
<td>1.9 4.1 4.3</td>
<td>94</td>
<td>10.1</td>
<td>42</td>
</tr>
<tr>
<td></td>
<td>0.95</td>
<td>10.6 42.3 41.6</td>
<td>1.4 11.8 12.3</td>
<td>101</td>
<td>15.7</td>
<td>59</td>
</tr>
<tr>
<td></td>
<td>0.20</td>
<td>11.3 10.7 11.8</td>
<td>3.6 3.4 3.0</td>
<td>84</td>
<td>2.8</td>
<td>21</td>
</tr>
<tr>
<td>Hexagonal box HDHS</td>
<td>0.80</td>
<td>6.40 7.04 8.45</td>
<td>4.1 4.7 3.9</td>
<td>91</td>
<td>9.0</td>
<td>36</td>
</tr>
<tr>
<td></td>
<td>0.95</td>
<td>28.1 53.0 50.3</td>
<td>35.8 25.5 27.2</td>
<td>102</td>
<td>15.6</td>
<td>58</td>
</tr>
<tr>
<td></td>
<td>0.20</td>
<td>9.10 8.21 8.44</td>
<td>2.5 2.9 3.4</td>
<td>83</td>
<td>2.4</td>
<td>17</td>
</tr>
<tr>
<td>Sector aware hexagonal box HDHS</td>
<td>0.80</td>
<td>6.82 6.84 6.92</td>
<td>3.0 3.1 3.4</td>
<td>88</td>
<td>7.1</td>
<td>26</td>
</tr>
<tr>
<td></td>
<td>0.95</td>
<td>28.1 53.0 50.2</td>
<td>35.8 25.6 27.2</td>
<td>102</td>
<td>15.5</td>
<td>58</td>
</tr>
<tr>
<td></td>
<td>0.20</td>
<td>9.87 8.49 9.03</td>
<td>2.0 2.5 2.2</td>
<td>83</td>
<td>2.2</td>
<td>14</td>
</tr>
<tr>
<td>Hexagonal box HDHS with DTC</td>
<td>0.80</td>
<td>5.01 4.94 4.93</td>
<td>4.3 4.5 4.1</td>
<td>90</td>
<td>7.1</td>
<td>37</td>
</tr>
<tr>
<td></td>
<td>0.95</td>
<td>22.6 22.5 23.0</td>
<td>8.6 9.9 9.1</td>
<td>92</td>
<td>7.9</td>
<td>49</td>
</tr>
<tr>
<td></td>
<td>0.20</td>
<td>13.5 14.0 13.4</td>
<td>7.9 8.2 8.1</td>
<td>84</td>
<td>2.4</td>
<td>32</td>
</tr>
<tr>
<td>Fixed frequency SVPWM</td>
<td>0.80</td>
<td>7.76 7.77 7.76</td>
<td>3.2 3.2 3.2</td>
<td>89</td>
<td>6.4</td>
<td>38</td>
</tr>
<tr>
<td></td>
<td>0.95</td>
<td>8.60 8.61 8.60</td>
<td>2.4 2.4 2.4</td>
<td>90</td>
<td>7.0</td>
<td>14</td>
</tr>
<tr>
<td></td>
<td>0.20</td>
<td>7.07 7.08 7.08</td>
<td>3.2 3.2 3.2</td>
<td>83</td>
<td>2.1</td>
<td>20</td>
</tr>
</tbody>
</table>

Table 5.4: Experimental output current THD levels and average switching frequencies of three phase inverter using various Bit-Stream SVM units. $H = 10$ for all HDHS modulators.

<table>
<thead>
<tr>
<th>Modulator Type</th>
<th>Modulation Index</th>
<th>Output Current THD (%)</th>
<th>Average switching frequency (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Square box HDHS</td>
<td>0.80</td>
<td>4.97 5.34 5.18</td>
<td>1.8 3.5 3.5</td>
</tr>
<tr>
<td></td>
<td>0.20</td>
<td>21.6 22.1 17.6</td>
<td>2.5 2.4 1.4</td>
</tr>
<tr>
<td>Hexagonal box HDHS</td>
<td>0.80</td>
<td>5.53 5.67 5.51</td>
<td>4.1 5.2 4.3</td>
</tr>
<tr>
<td></td>
<td>0.20</td>
<td>18.6 17.9 17.4</td>
<td>2.7 3.2 3.0</td>
</tr>
<tr>
<td>Sector aware hexagonal box HDHS</td>
<td>0.80</td>
<td>5.47 5.04 5.06</td>
<td>2.6 3.2 3.1</td>
</tr>
<tr>
<td></td>
<td>0.20</td>
<td>16.8 15.2 16.7</td>
<td>1.9 2.3 2.2</td>
</tr>
<tr>
<td>Hexagonal box HDHS with DTC</td>
<td>0.80</td>
<td>3.60 3.51 3.51</td>
<td>4.1 5.0 4.1</td>
</tr>
<tr>
<td></td>
<td>0.20</td>
<td>15.4 15.1 14.4</td>
<td>2.6 2.6 2.6</td>
</tr>
<tr>
<td>Fixed frequency SVPWM</td>
<td>0.80</td>
<td>5.24 5.07 5.07</td>
<td>3.2 3.2 3.2</td>
</tr>
<tr>
<td></td>
<td>0.95</td>
<td>4.83 4.83 5.16</td>
<td>1.5 1.5 1.5</td>
</tr>
<tr>
<td></td>
<td>0.20</td>
<td>16.3 16.2 16.1</td>
<td>3.2 3.2 3.2</td>
</tr>
</tbody>
</table>

does not distribute switching cycles – and therefore switching losses – evenly between the three phases. This results in the highest total switching losses and junction temperature stresses. The hexagonal-box SVM unit addresses this issue, but requires 260 logic elements; greater than the square-box SVM unit but fewer than the other modulators presented in this chapter. It offers lower switching losses and junction temperatures than the square-box modulator, but suffers from increased output current THD levels. The addition of a sector detector to the hexagonal-box SVM unit results in improved THD levels similar to those experienced using the square-box SVM unit while reducing the switching frequencies and losses of the inverter. However, the use of a sector detector significantly increases the logic consumption to 456 logic elements and 512 memory bits.
Analysis of the output current spectra of the various SVM units shows that the magnitudes of the fifth and seventh harmonics are greater than the magnitudes of the high frequency harmonics. A hexagonal-box SVM unit with DTC produces a similar output current waveform with greatly reduced fifth and seventh harmonic currents, and correspondingly the lowest output current THD levels of 3.54%, with similar switching losses and junction temperatures to the original hexagonal-box SVM unit. The addition of dead time compensation units increases the logic element consumption of the modulator to 505 logic elements.

A standard SVPWM unit is also discussed in this chapter. As the SVPWM unit employs a fixed frequency carrier oscillator, the output currents of the SVPWM-controlled inverter exhibit sharp spectral peaks, which result in a measured THD level of 5.13%. The SVPWM unit consumes 441 logic elements and 512 bits of memory. A significant advantage of the SVPWM unit is that, unlike the Bit-Stream SVM units presented in this chapter, it can operate in the overmodulation region.

5.9 Line Filters and Harmonic Limits

The modulators discussed in this chapter have used inductors to filter out the high frequency components of the switching voltage waveform. If the inverter is driving a dedicated load, the harmonic content of currents applied to the load is flexible, and is limited by what the load can accept. However, if the inverter is connected to an existing AC grid, various standards exist to define how much harmonic current is acceptable. For example, IEEE standard 1547 [115] specifies requirements for distributed generation equipment, including the harmonic current limits listed in Table 5.5 while the inverter is operating at rated load. The Total Demand Distortion (TDD), which is generally analogous to the THD at rated output current, is limited to 5.0%.

By comparing the harmonic current limits shown in Table 5.5 to the experimental output current spectra presented in this chapter, it is clear that although the overall THD levels (at \( m = 0.8 \)) are almost acceptable, the individual magnitude of the higher order harmonics are unacceptable, especially in the case of the PWM-controlled inverter.\(^2\) One possible solution to this problem is to increase the size of the filter inductor \( L \), but these inductors would then become larger, heavier and more expensive. The spread-spectrum nature of the Bit-Stream modulators results in lower individual harmonic current amplitudes, which reduces the required filter attenuation characteristics.

For this reason, designers frequently employ higher order filters such as the third-order \( LCL \) filter [116, 117], fifth-order \( LCLCL \) filters [118] etc. Distributed, transmission-line type filters, which represent even higher order filters, have been investigated [119]. These filters offer steeper attenuation curves, providing additional attenuation to high-frequency harmonics. Compared to

\(^2\)The carrier frequency of PWM-based inverters is generally set equal to an odd multiple of the fundamental – such as 3.25 kHz – in order to minimise the production even-order harmonics before filtering, thus easing the filter requirements.

| Harmonic Order \( n \) (odd harmonics) | \( n < 11 \) | \( 11 \leq n < 17 \) | \( 17 \leq n < 23 \) | \( 23 \leq n < 35 \) | \( 35 \leq n \) |
| Harmonic Limit (%) | 4.0 | 2.0 | 1.5 | 0.6 | 0.3 |

| Harmonic Order \( n \) (even harmonics) | \( n < 12 \) | \( 12 \leq n < 18 \) | \( 18 \leq n < 24 \) | \( 24 \leq n < 36 \) | \( 36 \leq n \) |
| Harmonic Limit (%) | 1.0 | 0.5 | 0.375 | 0.125 | 0.075 |
a simple, large, $L$ filter, $LCL$ filters offer better filtering effectiveness in terms of cost, size and weight. However, interactions between the $L$ and $C$ elements in these filters cause resonant poles which must be damped [117]. Two basic solutions to this problem exist: a resistor can be added to the $LCL$ filter to provide passive damping at the expense of small power losses, or the inverter can be controlled to provide active damping without further losses. Given the wide output spectrum of the HDBS modulators, damping will almost certainly be required. Although no investigations have been made into the feasibility of active damping an LCL network using an HDBS modulator, the GSC discussed in Chapter 6 uses an LCL line filter with passive damping.

5.10 Summary

This chapter proposes a family of three Bit-Stream based space vector modulators. These modulators use hysteretic techniques to convert two-phase Bit-Stream reference signals into control signals for a three-phase inverter. They employ an internal feedback system and state machine to directly set the state of a three phase inverter without requiring a carrier oscillator. The hysteresis effect is achieved by using a two-dimensional error box to maintain the $\alpha$ and $\beta$ axis current errors within preset bounds. The proposed modulators produce spread-spectrum output currents, and have been demonstrated experimentally using a 6 kW inverter system. The modulators are compared to the very common carrier-based SVPWM method. It is shown that the Bit-Stream modulators deliver spread spectrum output currents with similar THD levels to standard SVPWM control. The simplest modulator consumes only 102 logic elements in an Altera Cyclone II FPGA, while the hexagonal-box Bit-Stream modulator with DTC consumes a similar quantity of logic resources to the conventional SVPWM unit, and offers reduced THD levels. A brief discussion of the relationship between line filters, modulators and harmonic limits is included to demonstrate the potential benefits of spread-spectrum modulation.
Chapter 6

Bit-Stream Control of Grid Side Converter

The GSC is a critical component of the DFIG system discussed in this thesis. The RSC and GSC both require a regulated DC link voltage for proper operation. The GSC is used to regulate this DC link voltage because the rotor side converter is dedicated to the generator. The real power flow through the rotor side converter varies with speed and torque of the generator; the rotor can both absorb and generate real power. As such, the GSC must adjust the power flow between the DC link and the grid to match the demand of the rotor side converter and regulate the DC link voltage.

Although it is possible to convert AC power to DC using a simple diode rectifier, the GSC must be capable of operating in both the rectifying mode, where energy is transferred from the AC grid to the DC link, and the inverting mode, where energy is transferred from the DC link to the AC grid. This requirement has given rise to a family of circuits known as reversible rectifiers [43], active front ends [120] or GSCs [37]. Active switching devices such as IGBTs are used to control the flow of power through these converters, allowing operation in both the rectifying and inverting modes. Additionally, GSCs can generate reactive power if required. The converters used may be based on current sourced or voltage sourced converters [121] and can be controlled using a variety of controllers, including per-phase linear controllers [45], vector controllers [37] and predictive controllers [46]. Typically, these controllers are implemented digitally using microprocessors [14, 37, 45]. This chapter proposes a Bit-Stream based vector control system for the GSC.

A simplified circuit diagram of the GSC described in this chapter is shown in Fig. 6.1. The GSC consists of a line transformer, line filter, IGBTs and DC link. The Bit-Stream based control system developed in this chapter accepts voltage and current measurements from the AC line and DC link as shown in Fig. 6.1, applies appropriate control functions, and delivers gate drive signals to the IGBTs Q1 - Q6. The following sections discuss the GSC specifications, proposed control scheme and the Bit-Stream implementation of the control system. The proposed control system is designed using simplified equivalent circuit models and the Matlab/Simulink modeling software. Detailed simulations of the GSC, line filter and control system are performed using a VHDL model and ModelSim. Finally, the proposed Bit-Stream control system is tested experimentally using a 2 kW GSC prototype.
6.1 Specifications of Grid Side Converter

As discussed in Section 2.5.1, the GSC is used to balance the slip power of the machine and, optionally, provide VAr support to the grid. As such, the rating of the GSC is determined from the maximum expected rotor power, which is approximated by the total generator rating of 2.6 kW multiplied by the maximum slip of 25%; in this case 0.7 kW. Reference [65] provides a detailed methodology for choosing the size of the RSC and GSC. The GSC used in this thesis has a rating of 2 kW to allow for operation during transient events. The reactive power capability of the GSC is set by the degree of VAr support required. As the generator discussed in this thesis is excited via the rotor windings, as discussed in Chapter 8, the GSC does not need to supply reactive support to the generator. However, a grid connected generator may be required to provide reactive power support to the AC grid. The GSC is rated to sink or source 2 kVAR of reactive power to the grid, which corresponds to a total DFIG power factor of 0.8 leading or lagging. The GSC has a total apparent power rating of 2.8 kVA.

The New Zealand standard supply voltage is 400 V L-L RMS, which would require a DC bus voltage of approximately 700 V DC. As available laboratory power supplies are not suitable for use on systems with floating DC busses, and the available programmable loads are rated to 500 V DC maximum, a 400 V to 230 V step down transformer is used to isolate the DC link from the external grid as shown in Fig. 6.1, and the DC link voltage is set to 450 V. The basic specifications for the GSC are listed in Table 6.1. Although the inverter electronics and measurement systems are capable of operation at 400 V AC / 700 V DC, the increased DC bus voltage is unnecessary as the maximum required rotor voltage is expected to be less than 150 V AC.

<table>
<thead>
<tr>
<th>Table 6.1: Grid Side Converter Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quantity</td>
</tr>
<tr>
<td>Rated apparent power</td>
</tr>
<tr>
<td>Rated voltage</td>
</tr>
<tr>
<td>Rated current</td>
</tr>
<tr>
<td>Line frequency</td>
</tr>
<tr>
<td>DC link voltage</td>
</tr>
</tbody>
</table>

6.2 Control System for the Grid Side Converter

The following sections discuss the GSC’s control system. As previously discussed in Section 2.5.1, the real and reactive power flow through the GSC is controlled by adjusting the D and Q components.
of the GSC current vector, respectively. In order to perform this vector control task, three major control sub-systems are required as shown in Fig. 6.2: an AC measurement system to measure these vectors, vector current controllers to control the line current and a Bit-Stream to switch modulator to drive the power electronics. An outer control loop is used to maintain a constant DC link voltage by adjusting the D axis current reference and therefore the active power of the inverter. The proposed Bit-Stream control system has a resolution $R$ of 8 bits and a sampling rate $F_B$ of 1.25 MHz.

### 6.2.1 Measurement System

The measurement system accepts voltage and current measurements from the A, B and C phases of the GSC as shown in Fig. 6.1. The grid voltages $V_{GA}$, $V_{GB}$ and $V_{GC}$ are measured using analogue to Bit-Stream converters with a full scale input $V_{FS}$ of 512 V. The grid currents $I_{GA}$, $I_{GB}$ and $I_{GC}$ are measured using converters with a full scale $I_{FS}$ of 16 A. The voltage and current measurement gains $K_{VM}$ and $K_{IM}$ are given by (6.1) and (6.2) as 0.25 Q/V and 8.0 Q/A, respectively.

$$K_{VM} = \frac{2^{R-1}}{V_{FS}} \quad (6.1)$$

$$K_{IM} = \frac{2^{R-1}}{I_{FS}} \quad (6.2)$$

The per-phase measurements of the grid voltage and current are transformed from the phase domain to the stationary $\alpha\beta$ reference frame using Clarke Transformations. When plotted on the $\alpha\beta$ reference frame as shown in Fig. 6.3, the grid voltage vector $V_G$ rotates around the origin in a circular pattern.

Park’s Transformations are used to transform $V_G$ and $I_G$ – the grid current vector – from the stationary $\alpha\beta$ reference frame to the rotating DQ reference frame. A PLL similar to the one described in Chapter 3 provides a continuously updated angle reference $\theta_G$ to the Park’s Transformation units such that $V_G$ lies along the D axis. The D and Q axis components of the

---

1 Because the GSC control system uses a higher sampling rate and new analogue to Bit-Stream converters, the PLL parameters have been adjusted to those listed in Appendix D.
Figure 6.3: Orientation of grid voltage and GSC current vectors on the $\alpha\beta$ and $DQ$ reference frames.

Grid voltage $V_{GD}$ and $V_{GQ}$ are DC quantities, where:

$$V_{GD} = |V_G|$$  \hspace{1cm} (6.3)  

$$V_{GQ} = 0$$  \hspace{1cm} (6.4)

The D and Q axis components of the current vector $I_{GD}$ and $I_{GQ}$ are likewise DC quantities. The average AC side power $S_G$ of the GSC is the product of the voltage vector $V_G$ and the current vector $I_G$:

$$S_G = V_G I_G^*$$  \hspace{1cm} (6.5)

The average power can be rewritten as a real power $P_G$ and a complex power $Q_G$, and decoupled into D and Q axis components.

$$S_G = P_G + jQ_G = (V_{GD} + jV_{GQ})(I_{GD} - jI_{GQ})$$  \hspace{1cm} (6.6)

$$P_G = V_{GD}I_{GD}$$  \hspace{1cm} (6.7)

$$Q_G = -V_{GD}I_{GQ}$$  \hspace{1cm} (6.8)

Where a positive power value corresponds to power flow from the AC grid into the converter, i.e. rectifying mode. From (6.7) and (6.8) it is clear that the active and reactive power flow through the GSC is directly determined by the D and Q axis grid current components, respectively.

### 6.2.2 Current Controllers

The control system described in this section controls the D and Q axis grid current components in accordance with the current reference signals $I_{GD}^*$ and $I_{GQ}^*$. As previously noted, $I_{GD}$ and $I_{GQ}$ are DC quantities. This allows the use of simple Proportional-Integral (PI) controllers which have zero average tracking error and are easy to tune [37].

An alternative method is to control the current in the stationary $\alpha\beta$ reference frame using Proportional-Resonant (PR) controllers [79] which operate directly on the grid current vector in the $\alpha\beta$ domain. The implementation of PR controllers using Bit-Stream components has not been investigated.
Figure 6.4 shows the single-phase equivalent circuit of the GSC and line filter. As the grid voltage $V_G$ is determined by the power system, the GSC current $I_G$ is controlled by adjusting the output voltage vector of the GSC, $U_G$:

$$I_G = \frac{V_G - U_G}{jX_L} \quad (6.9)$$

Where $X_L$ is the reactance of the line filter, determined by the grid frequency $f_G$ and the filter inductance $L$:

$$X_L = 2\pi f_G L \quad (6.10)$$

Because the GSC current is dependent upon the voltage difference between the grid and the inverter, a voltage feed-forward scheme is used. As shown in Fig. 6.2, the D axis grid voltage is scaled by the feed-forward gain $k_{FF}$ and added to the D axis controller output. Because the Q axis grid voltage is approximately zero, no voltage compensation is applied to the Q axis control loop. Assuming that the output of the D axis PI controller is zero and no current is flowing, the D axis component of the converter output voltage $U_{GD}$ is a function of the grid voltage $V_{GD}$:

$$U_{GD} = k_{INV}k_{FF}k_{VM}V_{GD} \quad (6.11)$$

Where $k_{INV}$ is the combined gain of the modulator and inverter electronics, as discussed in Section 6.2.3. The gain $k_{FF}$ is derived by setting $U_{GD}$ equal to $V_{GD}$ and re-arranging (6.11) to form (6.13). In this case, $k_{FF}$ is set to 1.7 units.

$$k_{INV}k_{FF}k_{VM} = 1 \quad (6.12)$$

$$k_{FF} = \frac{1}{k_{VM}k_{INV}} \quad (6.13)$$

The current flowing through the line inductors causes a voltage difference between $V_G$ and $U_G$. This current is an AC quantity and the complex impedance of the inductors causes this voltage to be phase shifted by approximately 90 degrees. The flow of current in the D axis will affect the Q axis of the converter voltage reference vector and vice versa. The current controllers are capable of compensating for this influence under steady state conditions, but during transient events the cross-coupling is apparent, as shown in Fig. 6.5(a). In order to provide better control of transient currents, cross-axis decoupling can be added to the current control system shown in Fig. 6.2 [14, 37]. When the decoupling gain $k_{DEC}$ is set correctly, changes in the D and Q current components do not affect each other, as shown in Fig. 6.5(b). If $k_{DEC}$ is too large, the two axes become coupled again and the transient response of the current control system is impaired as shown in Fig. 6.5(c). The decoupling gain is given by (6.14) and should, in principle, vary with the frequency of the AC grid. A fixed value of 0.16 units is used in this application because the frequency variation of the AC grid is small and the PI controllers will remove any residual current errors.

$$k_{DEC} = \frac{X_L}{k_{IM}k_{INV}} \quad (6.14)$$
The cross-axis decoupling components of the control system effectively prevent changes in the D axis current from affecting the Q axis control system and vice versa. This allows the current control system to be simplified from a Multiple-Input Multiple-Output (MIMO) system to a pair of identical, independent Single-Input Single-Output (SISO) systems. The response of the current control loops can then be approximated by the simplified model shown in Fig. 6.6. This model is suitable for the initial selection of controller gains, but does not include sampling or switching effects. The current controller gains are selected to deliver a rise time of under 1 ms and a 20% overshoot. The system parameters used in this simulation are listed in Appendix D. The proportional and integral gains are set to 0.75 and 1850 units, respectively.

### 6.2.3 Modulator

The modulator, shown in Fig. 6.2, converts the output of the current control system into gate drive signals which control the inverter switches. The voltage command $u_{GD} + ju_{GQ}$ is converted from the DQ domain to the $\alpha\beta$ domain before the signals are delivered to the modulator.

The modulator has a characteristic gain $k_{MOD}$ which is dependent on the modulation technique chosen. A simple per-phase modulator which does not use space vector modulation techniques has
a characteristic gain of 1. A three phase modulator which employs space vector modulation is used instead because it offers a higher characteristic gain of $2/\sqrt{3}$ or 1.15 units \(^2\). This allows for better utilisation of the DC link voltage and provides increased control margin. A Bit-Stream based space vector modulator with dead time compensation, as discussed in Chapter 5, is used in this role.

For the purposes of simulation, the combined gain of the modulator and inverter, \(k_{INV}\), is calculated using (6.15). For operation with an 8 bit resolution and a 450 V DC bus, the overall gain is 2.34 V/Q.

\[
k_{INV} = V_{DC} \frac{k_{MOD}}{\sqrt{3} \cdot 2^{r-1}}
\]  

(6.15)

### 6.2.4 DC Link Voltage Control

The role of the GSC is to regulate the DC link voltage despite changes in the real power flow through the rotor side converter. The DC link voltage is controlled by adjusting the real power flow through the GSC. As the active power flow is proportional to \(I_{GD}\), a PI controller is used to adjust the D axis current reference \(I_{GD}^*\) as shown in Fig. 6.2. In order to determine the appropriate control gains for this controller, a model of the relationship between the DC link voltage and grid current must be determined.

A simplified model of the DC link control system is presented in Fig. 6.7. To develop this model, three assumptions are made about the GSC and its control system. Firstly, that the real power flow through the GSC is solely determined by the D axis current. Secondly, that the response of the D axis current controller is equivalent to a first order low pass filter with a time constant, \(\tau\), of 500 \(\mu\)s. Thirdly, losses in the line filter and converter switches are ignored. \(I_{LOAD}\) represents the DC link load imposed by the rotor side converter. A positive value of \(I_{LOAD}\) corresponds to a DC load and causes the GSC to operate in the rectifying mode, while a negative value of \(I_{LOAD}\) corresponds to a DC source and causes the GSC to operate in the inverting mode.

\[ P_{AC} = \sqrt{3} \cdot V_G \cdot I_{GD,RMS} \]  

(6.16)

\[ I_{GD,RMS} = \frac{I_{GD,Q}}{\sqrt{2} \cdot K_{IM}} \]  

(6.17)

Where \(I_{GD,Q}\) and \(I_{GD,RMS}\) are the D axis grid currents in quanta and Amperes RMS, respectively. The DC link current, which charges and discharges the DC link capacitance, is determined from

\[^2\text{This gain is independent of the threshold setting of the modulator.}\]
the DC side power $P_{DC}$ using (6.18). For the purposes of analysis, the DC-side power is assumed to be equal to the AC-side power: losses are neglected.

$$I_{DC} = \frac{P_{DC}}{V_{DC}}$$  \hspace{1cm} (6.18)

$$P_{DC} = P_{AC}$$  \hspace{1cm} (6.19)

Equations (6.16) to (6.19) can be combined to yield a transfer function from the D axis current in quanta $I_{GD,Q}$ to the DC link current $I_{DC}$:

$$I_{DC} = \frac{\sqrt{3}V_G \cdot I_{GD,Q}}{\sqrt{2}K_{IM}V_{DC}}$$ \hspace{1cm} (6.20)

The voltage controller gains are chosen using the simplified system shown in Fig. 6.7. A simple PI controller is used in this role as it offers relatively fast response and zero steady state tracking error. The proportional gain of the controller is used to provide fast response to changing DC load currents as shown in Fig. 6.8(a). Integral gain is applied in Fig. 6.8(b) to restore the DC link voltage to the desired level. In this case, the proportional and integral gains are 20 and 490 units, respectively. These gains result in tight control of the DC link voltage, but are subjected to large overshoots during startup, where the DC link capacitor is rapidly charged from approximately 300 V DC to 450 V DC. A soft charge mechanism for the DC link is discussed in Chapter 8.

### 6.3 Line Filter

A line filter is used to interconnect the GSC and the external grid. Because both the external grid and the GSC are voltage sources, a series inductor is used to limit current flow. This is the simplest type of line filter, which is known as an $L$ filter.

The line inductors used for the GSC have an inductance $L$ of 10 mH, sufficient to allow direct connection to the AC grid. However, the isolation transformer shown in Fig. 6.1 has a leakage inductance $L_{LK}$ of 400 µH referred to the secondary side. In principle, the series connection of the
filter inductor $L$ and the transformer leakage inductance $L_{LK}$ should simply behave like a somewhat larger filter inductor. In practice, stray capacitances within the inductors and transformer create resonant circuits. The high-speed voltage transitions of the IGBT-based GSC may excite these resonances and cause high voltage transients within the transformer windings.

Shunt capacitors $C$ are placed at the transformer’s secondary terminals, as shown in Fig. 6.9, to absorb the high frequency currents. The parallel connection of the transformer leakage inductance $L_{LK}$ and the shunt capacitor forms a resonant circuit. This resonant peak is undesirable and is damped with the RC damper components $R_D$ and $C_D$. A similar damped filter has been added between neutral and earth to provide common mode filtering using the components $C_C$, $R_{CD}$, $C_{CD}$. The parameters of the line filter are listed in Appendix D. For simulation purposes the transformer is modeled as a Thevenin voltage source, with per phase winding EMFs $e_A$, $e_B$ and $e_C$ representing the original line voltage multiplied by the transformer turns ratio. All ‘grid’ voltage and currents discussed in this chapter are measured at the locations indicated in Fig. 6.1.

6.4 Bit-Stream Based Control System for the Grid Side Converter

The following sections discuss the implementation of the complete Bit-Stream based control system for the GSC described in Section 6.2. The control system is developed by interconnecting the appropriate Bit-Stream control blocks as shown in the following sections.

Several of these control blocks – adders, subtractors, gains, PI controllers and reference generators – are provided by the original Bit-Stream library [26]. However, several new blocks have been developed specifically for the implementation of vector control systems: the Clarke Transformation, Park’s Transformation and phase locked loop developed in Chapter 3; and the Bit-Stream SVM unit developed in Chapter 5. Each component is written in VHDL code and can be added to a design either by writing appropriate code or by creating schematic symbols, which are then wired together to form the complete control system. The following sections describe the implementation of each control subsection: the measurement system, current controllers, modulator, DC link controller and DC link over-voltage protection. Simplified diagrams of each subsystem are presented in this chapter, and the exact schematic of the control system is presented in Appendix D.

---

3The main inductor $L$ is much larger than the transformer leakage inductance $L_{LK}$, and so plays little part in this resonance.
6.4.1 Measurement System

The measurement system for the GSC consists of the voltage and current sensors discussed in Appendix B coordinate transformation units and a phase locked loop. As shown in Fig. 6.10, the Bit-Stream elements are connected as shown in the original control diagram in Fig. 6.2 with one addition. Signal conditioning blocks have been placed between the input signals from the voltage and current sensors and the main control system. These are required because the ADCs used in the voltage and current measurement units have a minimum operating frequency of 5 MHz, whereas the main control system cannot operate at such a high sampling frequency. Therefore a set of down-sampling blocks is used to convert the sample rate of the measurement signals from 5 MHz to 1.25 MHz. These blocks can also be used to apply scale to the input signals if desired. In this case, gains of 2 and -1 are applied to the current and voltage channels, respectively and the signals VGA, VGB, VGC, IGA, IGB and IGC are delivered to the PLL and coordinate transformation units after scaling. As discussed in Chapter 3, the PLL oscillator angle $\theta_G$ is distributed as a pair of quadrature signals $\cos \theta_G$ and $\sin \theta_G$ to reduce the resource requirements of the Park’s Transformation blocks.

![Diagram of measurement system](image)

Figure 6.10: Bit-Stream implementation of the grid measurement system.

6.4.2 Current Controllers

The GSC current controllers are shown in Fig. 6.11. The basic error calculation and PI controller blocks are taken directly from the existing library, and the Bit-Stream vector scaling block proposed in Chapter 3 are used to implement the D axis voltage feed-forward and cross-axis decoupling gains directly.

The D and Q axis current controllers consist of standard PI controller blocks. The D and Q axis controllers have identical gain settings. The controllers’ P and I gain terms are specified as fractional values, which are determined using the method discussed in Section 3.2.2. An important consideration when using PI controllers is the provision of suitable controller limits on both the output signal and the integrator. Due to the intuitive saturation behaviour of the Bit-Stream control technique, both the outputs and integrator states of the PI controllers are limited between

---

4It is possible to synthesise a small Bit-Stream system for operation at 5 MHz, but this requires careful adjustment of the synthesis parameters. Additionally, the clocking structure of the Bit-Stream components is unusual and not well supported by standard timing analysis tools, which makes verification of the maximum clock frequency difficult.

5The previously stated values of $K_{IM}$ and $K_{VM}$ reflect the combined gains of the sensors and the down-sampling units
2^{R-1} - 1 and -(2^{R-1}), or +127 and -128 Q. In this situation, it is desirable to limit the control outputs to a smaller range. A post-scaling gain \( k_{\text{CONT}} \) of 0.5 units is used to reduce the effective controller output to +63 / -64 Q. When the GSC is not operating, the current control integrators are reset by the \( \text{gsc\_i\_cont\_reset} \) signal.

The control mixing blocks perform the AC line voltage feed forward and cross-axis decoupling functions. The two- and three-input vector scaling blocks developed for use in the PLL effectively sum the controller output signal, line voltage feed-forward and cross-axis terms with adjustable gains. Three gain ratios are required: a controller scaling gain of 0.5 units, a D axis voltage feed-forward gain of \( k_{\text{FF}} \) or 1.7 units and a cross axis decoupling term of \( k_{\text{DEC}} \) or 0.16 units. In order to achieve these three gains simultaneously, the denominator \( m \) of the scaling block is set to 50 units and the numerators \( k_1 \), \( k_2 \) and \( k_3 \) are set to \( m \times k_{\text{FF}} \), \( m \times k_{\text{CONT}} \) and \( m \times k_{\text{DEC}} \), respectively, as shown in Fig. 6.11.

6.4.3 Modulator

Fig. 6.12 shows the inverse Park’s Transformation unit and Bit-Stream modulator which convert the output signals of the current controllers into gate drive commands. A Bit-Stream based space vector modulator with dead time compensation, as discussed in Chapter 5, is used in this role. The modulator threshold, lift parameter and dead time are set to 750 units, 5 units and 11 counts, respectively. If the \( \text{GSC\_inhibit} \) signal is asserted the GSC switches are disabled.

6.4.4 DC Link Voltage Controller

The DC link voltage controller consists of a reference generator, voltage measurement unit (including a down-sampling unit), a PI controller and an over voltage protection system as shown in Fig. 6.13.
The reference is set to the target DC link voltage of 450 V multiplied by the DC link sensor gain of 0.125 Q/V. The resulting value of 56.25 quanta is not achievable, so the simulations are performed with a reference value of 56 quanta, or 448 V DC. Similarly to the current controllers described previously, the proportional and integral gains of the PI controller are set by pairs of numerator and denominator values as listed in Appendix D. The integrator value can be reset by asserting the vdc_cont_reset line.

An over voltage protection unit is employed to protect the GSC circuitry in the event of a fault. The DC bus voltage is constantly monitored by a Schmitt trigger. The Schmitt trigger has a hysteresis band of 2 Q or 16 V, and an offset of 68 Q or 544 V: the Over Voltage Protection signal OVP is asserted if the DC link voltage rises above 560 V DC.

![Figure 6.13: Bit-Stream implementation of the DC link voltage control system.](image)

### 6.4.5 Protection System

In addition to the over voltage protection unit embedded within the DC link voltage controller, the experimental hardware includes temperature sensors and IGBT desaturation protection. In the event of a fault the gsc_i_cont_reset, vdc_cont_reset and GSC_inhibit signals are all asserted to prevent damage to the GSC electronics. The incoming circuit breaker shown in Fig. 6.1 provides a final stage of over current protection. Further details on the protection system – which also includes protection features for the rotor side converter and generator – are provided in Chapter 8.

### 6.5 Simulation Results

The behaviour of the Bit-Stream controlled GSC system is assessed using simplified Matlab/Simulink models and detailed VHDL models. The Simulink models are used to establish the ‘ideal’ response of the control system, and do not include non-ideal behaviour such as signal quantisation, sampling delays or the impact of the modulator. The VHDL models are more detailed, and include the non-ideal effects of quantisation, sampling delays and the switch-mode nature of the Bit-Stream modulator. All simulations are performed assuming that the AC supply is balanced and free of distortion. The secondary side EMFs $e_A$, $e_B$ and $e_c$ are assumed to be sinusoidal voltages with a line to line voltage of 230 V.

The response of the control system to step changes of the Q axis current reference is shown in Fig. 6.14. Initially, the GSC is operating with no DC load and no reactive current command. At time $t = 50$ ms, the Q axis current reference changes from zero to +57 Q, which corresponds to 5 A RMS of inductive current. The reference returns to zero at $t = 100$ ms. At time $t = 150$ ms the Q axis current reference changes from zero to -57 Q, which corresponds to 5 A RMS of capacitive current.
Fig. 6.14(a) shows the response of the control system as modeled in Simulink. The Q axis current very rapidly follows the reference with a small overshoot, while the D axis current is not perturbed. The line currents are sinusoidal and separated by 120°.

Fig. 6.14(b) shows the response of the VHDL model to the same current reference steps. The response of the VHDL model is largely similar to that of the Simulink system, with two points of difference. Firstly, the VHDL model includes switching behaviour, which generates high frequency current ripple. Secondly, at zero current the GSC generates a small quantity of harmonic currents, primarily second harmonics. The results of this simulation show that the Bit-Stream current control system correctly controls the line current vector.

The response of the control system to step changes of DC load current is shown in Fig. 6.15. A 4.44 A or 2 kW load is applied to the DC bus at time $t = 100$ ms, and removed at time $t = 300$ ms.
A -4.44 A or 2 kW source is applied to the DC bus at time $t = 500$ ms, and removed at time $t = 700$ ms. The Q axis reference current is zero throughout the simulation.

Fig. 6.15(a) shows the response of the Simulink model to these load steps. When the load is applied, the DC link voltage drops by approximately 15 V, and smoothly returns to the steady state value of 450 V in approximately 100 ms. When the load is released, the DC link voltage rises by approximately 15 V before recovery. Corresponding voltage transients occur when a DC source is applied to the bus. This simulation shows that the proposed DC link control system successfully maintains a constant DC link voltage even when subjected to large load transients.

Fig. 6.15(b) shows the response of the VHDL model to the same DC load transient. The response of the VHDL model to the load transients is nearly identical to the response of the Simulink model, which indicates that the DC link control system operates as expected.

Figure 6.15: Simulated response of current control loops to step changes in DC load. (a) Response of Simulink model. (b) Response of VHDL model.
6.6 Experimental Results

This section presents experimental results of a 2 kW prototype GSC equipped with the proposed Bit-Stream control system, as shown in Fig. 6.16. The prototype GSC consists of a step down transformer, line filter and three-phase two-level inverter with identical parameters to those used in the simulations. All experiments were conducted with a DC link voltage of 452 V DC and an AC grid voltage, at the transformer secondary terminals, of 237 V L-L RMS.

---

6Due to a small gain error in the DC link voltage sensor, the actual DC link voltage is slightly higher than originally expected.

Figure 6.16: GSC and control system apparatus
6.6.1 Current Control Response

The response of the GSC to step changes in the Q axis current reference, which controls reactive power flow, is shown in Fig. 6.17. In both cases the GSC was operated with no DC load. As shown in Fig. 6.17(a), the Q axis current responds rapidly to the change in reference value from 0 to +5 A RMS (inductive). The current rise time is under 1 ms, and an overshoot of approximately 20% occurs in line with the simulation results. The D axis current is not perturbed by the rapid current transient, although an increase in the inverter losses does cause a small increase in the steady state D axis current to maintain the DC link voltage. Fig. 6.17(b) shows the response of the GSC to a Q axis reference step from 0 to -5 A RMS (capacitive). The Q axis current rise time is less than 1 ms, but the controller exhibits an overshoot of approximately 28%. Once again the D axis current is not perturbed by the sudden change in Q axis current, which demonstrates that the cross-axis decoupling operates correctly. These results demonstrate that the proposed Bit-Stream control system successfully control the grid current vector. The response of the experimental GSC system is very similar to the simulated behaviour, which indicates that the simplified models proposed in Section 6.2 can accurately predict the response of the control system.

![Figure 6.17: Experimental response of the GSC to step changes in reactive current reference. (a) from 0 – +5 A RMS (inductive), (b) from 0 – -5 A RMS (capacitive).](image)

6.6.2 DC Link Transient Response

The DC link transient response to step changes in DC load is shown in Fig. 6.18. In both cases the steady state DC link voltage is 452 V. Fig. 6.18(a) shows the response of the DC link to a step change from no load to a 2 kW load on the DC bus, which causes the GSC to operate in the rectifying mode. The DC link voltage falls by 15 V in the first 20 ms, and is restored to the normal operating point in approximately 100 ms. The phase currents are smoothly controlled during the transient. Fig. 6.18(b) shows the response of the GSC to a step from no load to a 2 kW source on

Note that the steady state DC link voltage was measured using a bench top multimeter and an oscilloscope was used to take transient DC link measurements. The multimeter’s measurement of the steady state voltage is considered to be definitive, whereas the oscilloscope is only used to investigate the DC link transients.
the DC bus: i.e. inverting mode. The DC voltage rises by 15 V in the first 20 ms and is restored to normal levels in approximately 100 ms. In both tests, the DC link exhibited no steady state voltage ripple. These results demonstrate that the DC link voltage is well-controlled.

![Figure 6.18](image)

Figure 6.18: Experimental response of the GSC to step changes in DC load. (a) step from no load to 2 kW load. (b) step from no load to 2 kW source.

### 6.6.3 Current Waveforms

Experimental measurements of the AC line currents were taken using both an oscilloscope and a PA4000 three phase power analyser from AVPower. Fig. 6.19 shows the steady state behaviour of the GSC in the rectifying mode with a 2 kW DC load. The line currents presented in Fig. 6.19(a) consist of sinusoidal 50 Hz currents and approximately 2 A of switching current ripple. As shown in Fig. 6.19(b), the highest harmonic components are the fifth and seventh harmonics, and the switching frequency components of the phase current are spread from 4 kHz to 8 kHz and have amplitudes lower than 1.5%. The line currents are measured at the location shown in Fig. 6.1 so the switching current components applied to the AC grid would be somewhat lower due to the presence of the line filter capacitors. The amplitudes of the first twenty harmonics, as measured using the PA4000 power analyser, are listed in Table 6.2. The measured THD level is 3.11% and the average switching frequency is 5.1 kHz. The DC offset of the phase currents were less than 10 mA.

Fig. 6.20 shows the steady state behaviour of the GSC in the inverting mode with a 2 kW DC source. The line currents consist of sinusoidal 50 Hz currents and approximately 2 A of switching current ripple. The highest harmonic component is the fifth harmonic at 2.8%, and the switching frequency components of the phase current are spread from 4 kHz to 8 kHz and have amplitudes lower than 1.5%. The average amplitudes of the first twenty harmonics, as measured using the PA4000 power analyser, are listed in Table 6.2. The measured THD level is 3.27% and the average switching frequency is 4.3 kHz.
Figure 6.19: Line currents of the GSC when operating in rectifying mode with 2 kW DC load and no reactive current. (a) A phase voltage and phase currents, (b) A phase current spectrum, with bandwidth of 10 kHz and resolution 10 Hz.

Figure 6.20: Line currents of the GSC when operating in inverting mode with 2 kW DC source and no reactive current. (a) A phase voltage and phase currents, (b) A phase current spectrum.

6.6.4 Losses and Efficiency

The power losses and efficiencies of the GSC were calculated for a range of values, as shown in Table 6.3. The GSC has a standby loss of approximately 60 W, which increases to a maximum of 179 W at maximum active and reactive load. Efficiencies vary between 92% and 95% at full load. In general, increased reactive power flow – whether inductive or capacitive – reduces the efficiency due to increased current flow. If the GSC is operated at unity power factor the efficiency at full load improves to between 94% and 95%.
Table 6.2: Harmonic current measurements, as measured by PA4000 power analyser.

<table>
<thead>
<tr>
<th>Harmonic Number</th>
<th>Amplitude (%)</th>
<th>Harmonic Number</th>
<th>Amplitude (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rectifying</td>
<td>Inverting</td>
<td>Rectifying</td>
<td>Inverting</td>
</tr>
<tr>
<td>1</td>
<td>100</td>
<td>2</td>
<td>0.25</td>
</tr>
<tr>
<td>3</td>
<td>0.40</td>
<td>4</td>
<td>0.41</td>
</tr>
<tr>
<td>5</td>
<td>2.21</td>
<td>6</td>
<td>0.27</td>
</tr>
<tr>
<td>7</td>
<td>0.49</td>
<td>8</td>
<td>0.63</td>
</tr>
<tr>
<td>9</td>
<td>0.24</td>
<td>10</td>
<td>0.58</td>
</tr>
<tr>
<td>11</td>
<td>0.58</td>
<td>12</td>
<td>0.81</td>
</tr>
<tr>
<td>13</td>
<td>0.77</td>
<td>14</td>
<td>0.21</td>
</tr>
<tr>
<td>15</td>
<td>0.18</td>
<td>16</td>
<td>0.43</td>
</tr>
<tr>
<td>17</td>
<td>0.29</td>
<td>18</td>
<td>0.65</td>
</tr>
<tr>
<td>19</td>
<td>0.49</td>
<td>20</td>
<td>0.46</td>
</tr>
</tbody>
</table>

Table 6.3: Power loss and efficiency measurements of the GSC at various operating points.

<table>
<thead>
<tr>
<th>Reactive Power Demand</th>
<th>DC Power Demand</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-2 kW</td>
</tr>
<tr>
<td>Inverting</td>
<td>Rectifying</td>
</tr>
<tr>
<td>2 kVAR Inductive</td>
<td>157 W</td>
</tr>
<tr>
<td></td>
<td>92%</td>
</tr>
<tr>
<td>0 kVAR</td>
<td>102 W</td>
</tr>
<tr>
<td></td>
<td>95%</td>
</tr>
<tr>
<td>-2 kVAR Capacitive</td>
<td>150 W</td>
</tr>
<tr>
<td></td>
<td>92%</td>
</tr>
</tbody>
</table>

6.6.5 Over Voltage Protection

The over voltage protection system is intended to operate at 550 V DC, and was tested using an adjustable DC power supply. Over voltage protection trips at 565 V and the converter can be reset once the DC bus voltage falls below 530 V.

6.6.6 FPGA Resource Consumption

Table 6.4 presents a summary of the FPGA resources consumed by the proposed control system. These resource consumption figures include adjustable parameter units for the PLL, PI controllers, modulator and over voltage protection.
### Table 6.4: Logic consumption of the proposed GSC control system.

<table>
<thead>
<tr>
<th>Control Region</th>
<th>Component</th>
<th>Resource Utilisation</th>
<th>Logic Elements</th>
<th>Memory Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock processing</td>
<td>Clock divider</td>
<td></td>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>Measurement system</td>
<td>Input down-sampling units</td>
<td></td>
<td>112</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Clarke transformations</td>
<td></td>
<td>78</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Park’s transformations</td>
<td></td>
<td>168</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Phase Locked Loop</td>
<td></td>
<td>347</td>
<td>4096</td>
</tr>
<tr>
<td>Current controllers</td>
<td>Reference generators</td>
<td></td>
<td>73</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Error calculation</td>
<td></td>
<td>31</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>PI controllers</td>
<td></td>
<td>373</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Control mixing</td>
<td></td>
<td>333</td>
<td>0</td>
</tr>
<tr>
<td>Modulator</td>
<td>Inverse Park’s Transformation</td>
<td></td>
<td>84</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Modulator</td>
<td></td>
<td>505</td>
<td>0</td>
</tr>
<tr>
<td>DC link voltage control</td>
<td>Reference generator</td>
<td></td>
<td>58</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Error calculation</td>
<td></td>
<td>15</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>PI controllers</td>
<td></td>
<td>310</td>
<td>0</td>
</tr>
<tr>
<td>Interlocking and protection</td>
<td>Interlock unit</td>
<td></td>
<td>189</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Over voltage detector</td>
<td></td>
<td>110</td>
<td>0</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td><strong>2786</strong></td>
<td><strong>4096</strong></td>
</tr>
</tbody>
</table>

6.7 Summary

This chapter described the development of a complete GSC and control system for interfacing the DC link of the doubly fed induction generator to the external AC grid. The proposed GSC system consists of a 230 V L-L AC supply, line filter, inverter, 450 V DC link and a Bit-Stream control system. The Bit-Stream control system consisted of a three phase AC measurement system, a vector current control system and a three phase modulator. An outer-loop DC link voltage control system automatically adjusts the grid current to maintain a constant DC link voltage and allows the GSC to operate in either the rectifying or inverting mode as required.

The Bit-Stream control system was constructed by assembling pre-defined Bit-Stream functional elements, ranging in complexity from the simple sum, difference, gain and integrator units originally developed [21] to the more sophisticated phase locked loop and space vector modulator elements discussed in Chapters 3 and 5. The control system gains were developed using simplified models of the grid current and DC link voltage control loops, then simulated with an idealised Simulink model and a detailed VHDL model to determine the expected behaviour of the system. Finally, experimental testing of a 2 kW GSC system demonstrated that the proposed Bit-Stream control system showed very similar response characteristics to both the Simulink and VHDL modeling results, successfully controlling the reactive power and DC link voltage of the GSC. Measurements of the grid current waveforms using a three phase power analyser yielded THD readings of approximately 3.3% under load. The close correspondence between the Simulink models and experimental results demonstrates that Bit-Stream control systems can be accurately modeled using standard modeling software, aiding the control system design process.
Chapter 7

Bit-Stream Control of Rotor Side Converter

The DFIG is a combination of a WRIM, an RSC and a GSC. The DFIG arrangement is capable of operating at a constant electrical frequency despite large changes in the generator shaft speed, which makes it well suited for use with wind turbines [37]. In order to operate over a large speed range, the RSC is used to inject or extract controlled currents into or from the generator’s rotor terminals. This chapter proposes a Bit-Stream based control system for the RSC which provides independent control of the generator torque and excitation using vector control techniques. As discussed in Chapter 2, the control of the rotor current vector is central to the majority of DFIG control algorithms that have been published in the literature; additional functionality such as sensorless operation or fault ride-through capabilities can be achieved by augmenting the control system proposed in this chapter. This is the first Bit-Stream based vector control system for electrical machinery to be reported in the literature.

As shown in Fig. 7.1, the RSC and generator control equipment consists of an external AC grid, the WRIM, the RSC and the GSC. The stator of the generator is connected to a 230 V AC grid, and the rotor of the generator is connected to the RSC. The Bit-Stream based control system developed in this chapter accepts voltage, current and speed measurements from the generator, applies appropriate control functions, and delivers gate drive signals to the IGBTs Q7-Q12. The GSC is discussed in detail in Chapter 6. The following sections discuss the RSC specifications, proposed control system and Bit-Stream implementation of the control system. The proposed

Figure 7.1: Circuit diagram of the WRIM and RSC.
control system is designed using Matlab/Simulink modelling software. Detailed simulations of the RSC, generator and control system are performed using a VHDL model and Mentor Graphics’ ModelSim. Finally, a 2.6 kW experimental prototype is used to verify that the combination of the generator, RSC and control system operates as expected. This control system only provides control of the rotor current vector: speed and excitation control systems are discussed in Chapter 8.

### 7.1 Rotor Side Converter Specifications

The proposed RSC control system is intended for use with a 3.7 kW WRIM, the parameters of which are listed in Table 7.1. The specifications of the RSC are determined from the WRIM parameters and the expected slip range of the generator. As shown in Fig. 7.1, the stator of the generator is connected to a 230 V L-L AC supply via contactor K2, which is used to synchronise the generator to the grid. This chapter only considers the operation of the synchronised generator; K2 is always closed. The maximum available torque available from the generator in this configuration is 20 Nm.

The generator is specified to operate over a ±25% slip range – or between 750 and 1250 Revolutions Per Minute (RPM) – with a corresponding maximum slip power of approximately 500 W. The GSC provides a regulated 450 V DC supply to the RSC, and is rated at 2 kW to provide a margin for operation during transient events. The RSC must be capable of delivering 8.4 A RMS at up to 300 V RMS to the rotor winding. The RSC specifications are summarised in Table 7.2.

Although the generator used in these experiments is rated for operation with 400 V L-L at the

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated voltage $V_S, V_R$</td>
<td>400 300</td>
</tr>
<tr>
<td>Rated current $I_S, I_R$</td>
<td>9.5 8.4</td>
</tr>
<tr>
<td>Resistance $R_S, R_R$</td>
<td>1.38 1.61</td>
</tr>
<tr>
<td>Leakage inductance $L_{LS}, L_{LR}$</td>
<td>9.48 5.33</td>
</tr>
<tr>
<td>Magnetising inductance $L_m$</td>
<td>127  mH</td>
</tr>
<tr>
<td>Number of pole pairs $P_P$</td>
<td>3</td>
</tr>
<tr>
<td>Rated torque $\tau_{nom}$</td>
<td>37.3 Nm</td>
</tr>
<tr>
<td>Synchronous speed</td>
<td>1000 RPM</td>
</tr>
<tr>
<td>Machine turns ratio $N_{RS}$</td>
<td>0.75</td>
</tr>
<tr>
<td>AC line voltage $V_{AC}$</td>
<td>230 V RMS L-L</td>
</tr>
<tr>
<td>AC line frequency $f_G$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Machine inertia $J$</td>
<td>0.11 kg m^2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated voltage</td>
<td>300 V RMS L-L</td>
</tr>
<tr>
<td>Rated current</td>
<td>8.4 A RMS</td>
</tr>
<tr>
<td>Rotor frequency</td>
<td>0 - 12.5 Hz</td>
</tr>
<tr>
<td>DC link voltage</td>
<td>450 V DC</td>
</tr>
</tbody>
</table>

Although the generator used in these experiments is rated for operation with 400 V L-L at the
7.2 Control System for RSC

The following sections discuss the control system for the RSC. As previously discussed in Chapter 2, the rotor current vector is manipulated to control the generator torque and flux. In order to perform this vector control task, three major control subsystems are required, as shown in Fig. 7.2: a measurement system, current controllers and a Bit-Stream to switch modulator. The proposed Bit-Stream control system has a resolution $R$ of 8 bits and a sampling rate $F_B$ of 1.25 MHz.

The D and Q axis rotor current references $I_{RD}^*$ and $I_{RQ}^*$ are provided by external control systems. In this chapter, which considers only the generator and the RSC, the current references are set manually. Chapter 8 discusses outer loop control systems which control the generator speed and excitation using these reference signals.

![Figure 7.2: Block diagram of proposed control system for the RSC.](image-url)
7.2.1 Measurement System

The measurement system of the proposed control system fulfills two roles: determining the slip angle of the generator and transforming the rotor current signals from the phase domain to the rotating DQ reference frame. The Clarke and Park’s transformation units employed in the measurement system are identical to those used in Chapter 6, but the PLL is replaced in this case by the stator flux estimator and slip angle calculation elements. The stator voltages $V_{SA}$, $V_{SB}$ and $V_{SC}$ are measured with respect to neutral with a gain $K_{VM}$ of 0.25 Q/V. The rotor currents $I_{RA}$, $I_{RB}$ and $I_{RC}$ and stator currents $I_{SA}$, $I_{SB}$ and $I_{SC}$ are measured with a gain $K_{IM}$ of 8 Q/A.

The generator speed $\omega_R$ is measured using an optical encoder which outputs 500 pulses per mechanical revolution. This section focuses on the development of the stator flux estimator and slip angle reference system.

The generator produces torque – and hence power – by the interaction of magnetic fields developed by the rotor and stator windings. Using the FOC technique outlined in Section 2.5.2, the torque production of the generator is given by (2.34), reproduced here as (7.1). The alignment of the rotor current measurements to the stator flux are shown graphically in Fig. 7.3(a).

$$\tau_E = k_\tau I_{RQ} \lambda_{SD} \tag{7.1}$$

Where $k_\tau$ is the machine torque constant given by (7.2). For the generator parameters listed in Table 7.1, the torque constant is 3.1406 N.m/A.Wb.

$$k_\tau = \frac{3}{2} P_P \frac{L_M}{L_M + L_{LS}} N_{RS} \tag{7.2}$$

However, the rotor current transformations are not performed using the stator flux angle $\theta_S$. This is because the rotor moves within the generator. The physical angle of the rotor $\theta_R$ would likewise rotate the rotor current vector within the generator if no compensation is applied. As such, the actual transformation angle used in this case is the slip angle $\theta_{slip}$, which reflects the angle

---

The exact parameters of the ADCs used in this control system are presented in Appendix B.
between the stator flux vector and the rotor windings themselves as shown in Fig. 7.3(a). The slip angle is given by:

$$\theta_{\text{slip}} = \theta_S - P_P \theta_R$$  \hspace{1cm} (7.3)

The number of pole pairs $P_P$ is considered because each mechanical rotation of the generator corresponds to $P_P$ electrical rotations. The rotor angle $\theta_R$ of the generator is determined by integrating the generator speed $\omega_R$, as shown in Fig. 7.2.

The stator flux vector $\lambda_S$ is estimated based on measurements of the stator voltage $V_S$ and current $I_S$. The stator flux vector $\lambda_S$ is the integral of the stator EMF vector $E_S$:

$$\lambda_S = \int E_S dt$$  \hspace{1cm} (7.4)

$E_S$ can be found by subtracting the stator’s IR drop from the stator terminal voltage:

$$E_S = V_S - R_S I_S$$  \hspace{1cm} (7.5)

The stator flux magnitude $\lambda_S$ and angle $\theta_S$ can then be extracted from the flux vector. However, direct integration is not practical due to difficulties with initial conditions and errors in the calculation of $E_S$. DC offsets are a particular concern [30], especially at low speeds where the magnitude of $E_S$ is small. Fortunately, the stator of a DFIG unit is connected to an external AC grid, which delivers approximately constant voltage and frequency to the stator and maintains a relatively large EMF vector. Advanced flux estimator structures can effectively reject small DC offsets and initial condition errors [122], but the issue of extracting $\theta_S$ from $\lambda_S$ remains.

A standard microprocessor implementation generally uses an arctangent function to perform this extraction – e.g. $\theta_S = \text{atan2}(\text{Im}(\lambda_S), \text{Re}(\lambda_S))$. However, the synthesis of such functions (for example, the CORDIC algorithm) in FPGA logic is difficult and would consume significant numbers of logic elements [123]. Instead, the feedback-based estimator shown in Fig. 7.4 is employed [30]. This estimator simultaneously integrates the stator EMF vector and decomposes the stator flux vector into polar coordinates. The NCO developed in Chapter 3 is reused in the stator flux estimator.

The stator flux estimator requires four different gain settings. Three of these – the nominal flux $\lambda_0$, the stator resistance compensation gain $k_{RS}$ and the frequency scale factor $k_f$ – are set by system parameters and can be found using (7.6) – (7.8). The NCO used in this case has a phase integrator width $P_{\text{width}}$ of 24 bits. For the generator used in this study, $\lambda_0$ is 47 Q, $k_{RS}$ is 0.69 and $k_f$ is 1828. The gain $\omega_e$ is adjustable and determines the speed of response of the estimator. In this case, $\omega_e$ = 488 rad/sec and the estimator settling time is approximately 100 ms.

![Figure 7.4: Block diagram of the stator flux estimator.](image-url)
\[ \lambda_0 = \sqrt{\frac{2}{3}} V_S K_{VM} \]  
\[ k_{RS} = R_S K_{VM} K_{IM} \]  
\[ k_f = \frac{F_f 2^{\text{width}}}{F_B} \times 2^{R-1} \frac{\lambda_0}{\lambda_0} \]

A rotor phase offset signal \( \theta_{OST} \) is used to align the phases of the stator and grid voltages; it is manually adjusted to remove any offset between the ‘true’ and measured shaft angles.

The conversion from the rotor phase currents \( I_{RA}, I_{RB} \) and \( I_{RC} \) to the rotor current vector \( I_{RD} + jI_{RQ} \) is accomplished using Clarke and Park’s transformations.

### 7.2.2 Rotor Current Controllers

The rotor current control system shown in Fig 7.2 is very similar to the system used in Chapter 6. The rotor current vector is controlled in the DQ domain using PI controllers.

Cross-axis decoupling terms such as those used in [37] may be added to improve the transient response of the rotor current but are not used in this case for two reasons. Firstly, the maximum slip frequency of the generator is expected to be 12.5 Hz, so the cross axis coupling effect is smaller than that experienced in the GSC. Secondly, the variable frequency nature of the RSC would require relatively complicated variable-gain compensation systems.

The proportional and integral gains of the controller are set to 0.25 and 9.6 units, respectively.

### 7.2.3 Modulator

A similar modulator to that described in Chapter 6 is used to convert the output signals of the rotor current controller into gate drive signals for the RSC.

### 7.3 Bit-Stream Implementation of Control System for the RSC

The following sections discuss the implementation of the complete Bit-Stream based control system for the RSC described in Section 7.1. The control system is developed by interconnecting the appropriate Bit-Stream control blocks as shown in the following sections.

Several of the control systems developed for use with the control system for the GSC are re-used in the control system for the RSC; the current control system is very similar and the modulator section is identical. However, the measurement system is much more complex and a new stator flux estimator and slip angle calculation system have been developed specifically for use in this control system. The following sections describe the implementation of the measurement system – including the stator flux estimator and slip angle calculation system – current controllers, modulator and protection systems. Simplified diagrams of each subsystem are presented in this chapter, and the exact schematic of the control system is presented in Appendix F.
7.3 Bit-Stream Implementation of Control System for the RSC

7.3.1 Measurement System

The measurement system for the RSC consists of analogue to Bit-Stream converters, a rotary encoder, a stator flux estimator, slip angle calculator and rotor current transformations. Analogue to digital converters are used to measure the stator voltages, stator currents and the rotor currents as shown in Fig. 7.1. A schematic outlining the Bit-Stream based generator measurement system is shown in Fig. 7.5. Because these ADCs require a minimum sampling clock rate of 5 MHz, down-sampling units are employed to convert the 5 MHz ADC sampling rate to the 1.25 MHz Bit-Stream sampling rate and apply scaling factors to the signals.

The most complex component of the rotor current measurement system is the stator flux estimator proposed in Section 7.2.1. A Bit-Stream based implementation of the estimator is shown in Fig. 7.6. Two changes have been made: the filter elements have been created using explicit feedback networks and the integrators used within these filter blocks have been adapted to provide both Bit-Stream and integer outputs. The stator flux estimator outputs the stator flux magnitude \( \lambda_S \) as an 8 bit integer. The NCO uses the phase accumulator and look up table specifications discussed in Chapter 3 and outputs the stator flux angle \( \theta_S \) as a 9 bit integer.

The low-pass filters are constructed using gain blocks \( k_1 - k_4 \) and integrators which have been modified to produce dual Bit-Stream and integer outputs. The gain values are given as follows:

\[
k_1 = \frac{2\pi f_G}{K_I} (7.9)\]

\[
k_2 = \frac{\omega_e}{K_I} (7.10)\]

2. The previously stated values of \( K_{IM} \) and \( K_{VM} \) reflect the combined gains of the sensors and the down-sampling units.
Where \( k_f' \) is the inherent integrator gain as given by (3.12). Because \( k_4 \) is unity the scaling block is replaced by a direct connection. The division operation is performed using a Bit-Stream scaling block with a variable gain of \( \lambda_0/\lambda_S \). During normal operation, \( \lambda_S \) is positive. When \( \lambda_S \leq 0 \) the scaling block acts as an integrator, and the estimator rapidly increases the stator flux estimate until \( \lambda_S > 0 \). The selection of values for \( \lambda_0 \) and \( k_f \) are as previously discussed in Section 7.2.1, and the exact parameters used are listed in Appendix E.

An HEDS-5540 optical angle encoder is used to measure the rotor angle of the generator. This encoder delivers two signals, ENC_A and ENC_B, to the control system, which can be processed to determine the direction of rotation based upon their phase relationship, as shown in Fig. 7.7. The resolution of the encoder is specified in terms of the number of encoder lines \( N_L \), in this case 500. The quadrature signals are decoded to produce four output pulses per line as shown in Fig. 7.7; the encoder and decoder together deliver 2000 pulses per revolution. A counter is used to sum these signals and provide a true angle output. The counter must reset itself at 2000 counts – i.e. 1998, 1999, 0000, 0001 etc. – so that one ‘revolution’ of the counter corresponds to one revolution of the shaft.
The slip angle $\theta_{\text{slip}}$ is calculated from the stator flux and rotor angles according to (7.3). Although conceptually simple, the scale factors must be considered carefully; (7.3) is expressed in terms of radians, but the angles within the control system are represented using integer signals. The stator flux angle $\theta_S$ and slip angle $\theta_{\text{slip}}$ are represented by 9 bit integer signals with a range of 0 – 511 counts. The rotor angle $\theta_R$ is represented by an 11 bit integer with a range of 0 - 2000 counts. The corresponding gains $k_{\theta S}$, $k_{\theta_{\text{slip}}}$ and $k_{\theta R}$ are given by:

$$k_{\theta S} = \frac{2\pi}{512}$$

$$k_{\theta_{\text{slip}}} = \frac{2\pi}{512}$$

$$k_{\theta R} = \frac{2\pi}{2000}$$

Equation (7.3) can then be rewritten to include these scaling terms and simplified.

$$k_{\theta_{\text{slip}}} \theta_{\text{slip}} = k_{\theta S} \theta_S - P_P k_{\theta R} \theta_R$$

$$\theta_{\text{slip}} = \frac{k_{\theta S}}{k_{\theta_{\text{slip}}}} \theta_S - P_P \frac{k_{\theta R}}{k_{\theta_{\text{slip}}}} \theta_R$$

$$\theta_{\text{slip}} = \theta_S - 3\frac{2\pi}{500} \theta_R = \theta_S - 3\times 512 \frac{\theta_R}{2000}$$

The final required scale factor is 0.768 units. This is approximated by the factor 393/512 or 0.7676 units as shown in Fig. 7.8. The multiplication is performed using a standard multiplier element, which is often available in dedicated hardware in an FPGA, and the division is performed using a binary shift operation because hardware division consumes large numbers of logic elements. This scale factor is approximate but results in an effective error of less than 0.1 degrees.

The generator protection system and the generator speed control loop discussed in Chapter 8 both require a generator speed measurement. The processed rotary encoder output consists of a direction signal $\text{dir}$ which indicates the direction of rotation and a $\text{count}$ signal, which can be converted into a positive, negative or zero signal using the multiplexers shown in Fig. 7.8. An $\text{out gen word}$ block from the Bit-Stream library is used to convert these pulsed signals into a Bit-Stream speed signal $\omega X$. The speed scaling factor $N_S$ is used to set the maximum measurable

---

3 This calculation could be simplified by the use of an encoder which delivered 512 pulses per revolution; the scaling factor would be simplified to a factor of exactly 0.75. However, commonly available angle encoders deliver 100, 200, 500 or 100 pulses per revolution and must be subject to less convenient scaling factors.
shaft speed $N_{\text{MAX}}$ in RPM. The generator is expected to operate between 750 and 1250 RPM, so $N_{\text{MAX}}$ is set to 1500 RPM. The parameter $N_S$ is determined by comparing the number of pulses per second provided by the angle encoder and decoding unit $N_E$ (7.19) to the number of quanta per second which the out_gen.word can deliver $N_\omega$ (7.20). From (7.21), the target value of $N_S$ is 12.5 units, which is rounded down to 12 units. This yields a maximum measurable speed of 1562 RPM.

\[
N_E = \frac{4N_LN_{\text{MAX}}}{60} \quad (7.19)
\]

\[
N_\omega = \frac{F_B}{2} \quad (7.20)
\]

\[
N_S = \frac{N_\omega}{N_E} = \frac{60F_B}{8N_LN_{\text{MAX}}} \quad (7.21)
\]

The combined speed sensor gain $k_\omega$ is then determined from the ratio of the maximum speed to the maximum output signal (7.23), yielding a total gain of 0.782 Q/\text{rad/s}.

\[
k_\omega = \frac{2\pi}{60} \times \frac{N_{\text{MAX}}}{2^{R-1}} \quad (7.22)
\]

\[
k_\omega = \frac{\pi F_B}{4N_LN_S2^{R-1}} \quad (7.23)
\]

The use of the parameter $N_S$ to adjust the speed measurement gain has a drawback. The out_gen.word block is usually provided with an input of zero, and sometimes provided with an input of $N_S$. As the out_gen.word block converts the incoming signal into Bit-Stream quanta at the earliest possible opportunity, the Bit-Stream signal $\omega_X$ consists of a clump of positive quanta followed by a clump of zero quanta, as illustrated in Fig. 7.9. This clumping effect can cause undesirable saturation effects in Bit-Stream systems. The low pass filter shown in Fig. 7.8 is used to de-clump $\omega_X$ and produce a useful speed measurement signal $\omega_R$. The low pass filter is very similar to those used in the stator flux estimator, with gains $k_1$ and $k_2$ both set to one. The filter has a time constant of approximately 200 $\mu$s.

![Figure 7.9: Illustration of the effects of clumping on the speed measurement signals $\omega_X$ and $\omega_R$](image)
7.3.2 Rotor Current Controllers

The rotor current controllers are shown in Fig. [7.10] Standard PI controllers are used, and no cross-axis decoupling or feed-forward terms are required.

![Bit-Stream implementation of the rotor current control system.](image)

Figure 7.10: Bit-Stream implementation of the rotor current control system.

The D and Q axis PI controllers consist of standard PI controller blocks with equal gain settings. The controllers’ P and I gain terms are specified as fractional values using the method outlined in Section 3.2.2 The final values for the control parameters are presented in Fig. 7.10 and Appendix E. The output of the current controllers is limited to $\pm 32$ Q by post-scaling elements with a gain of 0.25 units. Given an inverter gain $k_{INV}$ of 2.34 V/Q from (6.15), up to 92 V L-L RMS can be applied to the rotor.

7.3.3 Modulator

Fig. [7.11] shows the inverse Park’s Transformation unit and Bit-Stream modulator which convert the output signals of the current controllers into gate drive commands. A Bit-Stream based space vector modulator with dead time compensation, as discussed in Chapter 6, is used in this role. The modulator threshold, lift parameter and dead time are set to 750 units, 2 units and 4.4 $\mu$s, respectively. If the RSC_inhibit signal is asserted the RSC switches are disabled. The characteristic gain of the modulator and inverter $k_{INV}$ is calculated to be 2.34 V/Q from (6.15).

![Bit-Stream implementation of the modulator for the RSC.](image)

Figure 7.11: Bit-Stream implementation of the modulator for the RSC.

7.3.4 Under and Over Speed Protection

Under and over speed protection is provided using the Schmitt trigger units shown in Fig. [7.12] The speed thresholds are set based on the desired over- and under-speed trip points of 1300 RPM and 700 RPM divided by the speed sensor gain $k_\omega$. As the Schmitt trigger units have a hysteresis
band of $2^{-1}/64$ or 2 Q, the overspeed threshold is set 2 Q below the calculated value and the underspeed threshold is set 2 Q above the calculated value.

When the generator exceeds the maximum speed limit, the OSP signal is asserted, the generator is disconnected from the AC grid and the RSC is disabled. Likewise the generator and RSC are disabled if the speed drops below the minimum speed limit. A detailed description of the DFIG protection systems is given in Chapter [8].

### 7.4 Simulation Results

The behaviour of the Bit-Stream controlled RSC and generator is assessed using simplified Matlab/Simulink models and detailed VHDL models. The Simulink models are used to establish the ‘ideal’ response of the control system, and do not include non-ideal behaviour such as signal quantisation, sampling delays or switching current ripple. The VHDL models are more detailed, and include the non-ideal effects of quantisation, sampling delays and switching current ripple. The simulations are performed assuming that the stator of the generator is directly connected to a three phase 230 V L-L RMS supply, and the DC link is maintained at 450 V by the GSC and associated control system discussed in Chapter [6]. The stator flux magnitude is approximately 0.6 Wb for these simulations. In all simulations, the D axis rotor current references $I_{RD}$ is set to a constant value of 50 Q – or 6.25 A peak – to completely magnetise the generator without drawing any reactive power from the stator connections. The Q axis reference $I_{RQ}$ sets the generator torque and is adjusted depending on the simulation under consideration. The maximum operating current of the generator’s rotor winding is 8.4 A RMS, or 11.9 A peak. As the D axis current is set to 6.25 A peak, the Q axis current must be less than 10.1 A peak. The Q axis reference current is therefore limited to $-80 \leq I_{RQ}^* \leq 80$ Q. Positive values of $I_{RQ}^*$ correspond to motoring mode and negative values correspond to generating mode. Two scenarios were simulated: a Q axis current reference step at a constant speed of 750 RPM and a generator speed sweep from 750 RPM to 1250 RPM with a constant Q axis current reference.

The response of the control system to step changes of $I_{RQ}^*$ is shown in Fig. [7.13]. The generator operates at 750 RPM or 25% slip throughout the simulation. This is a challenging condition for the rotor current control system as the frequency of the rotor currents is at its maximum and therefore the axes experience their greatest degree of cross-coupling. Initially, the generator operates with $I_{RQ}^* = 0$ or zero torque. At time $t = 100$ ms, the Q axis current reference changes from zero to -80 Q or -10 A peak. From the generator torque equation (7.1), this 10 A reference current should correspond to an electrical torque of approximately 19 Nm. The current reference returns to zero at time $t = 400$ ms.

Fig. [7.13(a)] shows the response of the control system as modelled in Simulink. The rotor current is initially 4.4 A RMS at 12.5 Hz. At time $t = 100$ ms the Q axis rotor current rapidly increases
and tracks the Q axis current reference within approximately 50 ms. The response of the Q axis current controller is stable and well damped, with a time constant of approximately 20 ms. Some cross-coupling into the D axis current and oscillation is observed, but the D axis current is restored and the oscillation is damped away. The generator develops an electrical torque $\tau_E$ of 20.1 Nm. This is somewhat higher than expected because the flow of current from the stator to the AC grid causes the stator EMF to increase, which in turn increases the stator flux. When the Q axis current reference returns to zero the Q axis current and generator electrical torque follow. The oscillation of the D and Q axis currents is caused by rapid changes in the applied rotor voltage impacting the generator flux; if the Q axis reference current is varied slowly instead of instantaneously, the magnitudes of these oscillations are reduced.

Fig. 7.13(b) shows the response of the VHDL model to the same current reference steps. In general, the response of the VHDL model is identical to that of the Simulink model, with the addition of switching current ripple; the Simulink model does not include switching effects. When the Q axis rotor current is low, the rotor currents are subject to a small amount of distortion at 75 Hz, due to small errors in the dead time compensation scheme. It is important that the rotor current control systems operate correctly over the entire operating speed range of the generator. Fig. 7.14 shows the rotor currents of the generator during a speed sweep from 750 RPM to 1250 RPM or 25% slip to -25% slip over 10 seconds. $I_{RD}$ and $I_{RQ}^*$ are set to 50 Q and -80 Q, respectively. Fig. 7.14(a) shows the response of the Simulink model to the
speed sweep. The frequency of the rotor phase currents varies with the shaft speed of the generator, but the amplitudes of the rotor phase currents remain constant. The D and Q axis rotor currents are regulated and the generator torque is regulated at 20 Nm throughout the test. This shows that the RSC’s control system is capable of controlling the generator torque independently of the shaft speed. Fig. 7.14(b) shows the response of the VHDL model to an identical speed sweep. The overall response of the VHDL model is very similar to that of the Simulink model, neglecting the addition of switching current ripple.

7.5 Experimental Results

This section presents the experimental results of the RSC and generator when controlled by the proposed Bit-Stream control system using the apparatus shown in Fig. 7.15. The DC link was provided by the GSC described in Chapter 6. The stator of the generator is connected to a 230 V L-L AC supply. All experiments were conducted using a fixed D axis current reference of 49 Q, which is sufficient to fully magnetise the generator; the stator winding of the generator draws no reactive power from the AC grid. A variable speed drive and cage induction motor were used as the prime mover in these experiments. The generator speed was controlled by the VSD. This section provides experimental results which verify that the RSC, generator and control system provide closed loop control of the rotor current vector and that the over- and under-speed protection
systems operate at the desired speeds.

### 7.5.1 Rotor Current Control Response

The response of the RSC, generator and proposed control system to step changes in the Q axis current reference is shown in Fig. 7.16. The generator operates at 750 RPM or 25% slip, and the D axis current reference is set to 49 Q. Fig. 7.16(a) shows the response of the rotor current control system to a Q axis reference step change from 0 Q to -80 Q. The D axis current remains approximately constant, and the Q axis current tracks the Q axis current reference in a stable and well damped manner with a time constant of approximately 20 ms. Fig. 7.16(b) shows the response of the rotor current control system to a Q axis reference step change from -80 Q back to 0 Q. Once again, the D axis current remains approximately constant and the Q axis current rapidly tracks its reference. The experimental response of the rotor current vector to the step changes in the Q axis current reference are similar to the simulated response, and demonstrate that the proposed control system is capable of rapidly adjusting the rotor current and therefore generator torque. However, the D and Q axis currents experience some ripple at approximately 12 Hz. This is due to a deviation in the shaft to which the rotor angle is mounted, and cannot be easily compensated out.

The response of the RSC, generator and proposed control system to a speed sweep 750 RPM to 1250 RPM over 10 seconds is shown in Fig. 7.17. During the speed sweep the rotor phase currents
Figure 7.16: Experimental response of D and Q axis rotor currents to a step change in the Q axis current reference, at 750 PRM, (a) from 0 to -80 Q and (b) from -80 to 0 Q.

Figure 7.17: Response of rotor phase currents during a speed sweep from 750 RPM to 1250 RPM.

remain sinusoidal and well controlled. This result demonstrates that the Bit-Stream control system is capable of regulating the machine torque over the entire operating speed range.

7.5.2 Over- and Under-speed Protection Systems

The over- and under-speed protection systems were tested by manually adjusting the speed of the generator during operation. The over speed protection trips at 1300 RPM and the underspeed protection trips at 705 RPM.
7.5.3 FPGA Resource Consumption

Table 7.3 presents a summary of the FPGA resources consumed by the proposed control system. These resource consumption figures include manual current reference units and adjustable parameter settings for the PI controllers and over- and under-speed protection.

Table 7.3: Logic resource consumption of the proposed control system for the RSC.

<table>
<thead>
<tr>
<th>Control Region</th>
<th>Component</th>
<th>Resource Utilisation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Logic Elements</td>
</tr>
<tr>
<td>Clock processing</td>
<td>Clock divider</td>
<td>4</td>
</tr>
<tr>
<td>Measurement system</td>
<td>Input down-sampling units</td>
<td>144</td>
</tr>
<tr>
<td></td>
<td>Clarke transformations</td>
<td>117</td>
</tr>
<tr>
<td></td>
<td>Stator flux estimator</td>
<td>500</td>
</tr>
<tr>
<td></td>
<td>Angle reference system</td>
<td>150</td>
</tr>
<tr>
<td>Current controllers</td>
<td>Reference generators</td>
<td>68</td>
</tr>
<tr>
<td></td>
<td>Error calculation</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>PI controllers</td>
<td>392</td>
</tr>
<tr>
<td></td>
<td>Control mixing</td>
<td>30</td>
</tr>
<tr>
<td>Modulator</td>
<td>Inverse Park’s Transformation</td>
<td>84</td>
</tr>
<tr>
<td></td>
<td>Modulator</td>
<td>505</td>
</tr>
<tr>
<td>Interlocking and protection</td>
<td>Interlock unit</td>
<td>189</td>
</tr>
<tr>
<td></td>
<td>Overspeed detector</td>
<td>143</td>
</tr>
<tr>
<td></td>
<td>Underspeed detector</td>
<td>143</td>
</tr>
<tr>
<td>TOTAL</td>
<td></td>
<td>2499</td>
</tr>
</tbody>
</table>

7.6 Summary

This chapter described the implementation of a Bit-Stream control system for the RSC of the DFIG system. The proposed system consists of a generator, RSC and a Bit-Stream control system. The stator of the generator was connected to a 230 V AC supply, and the rotor of the generator was directly connected to the RSC. The proposed Bit-Stream control system consists of a generator measurement system, a vector current control system and a three phase modulator. The control system accepts two input signals which are used to control the RSC and therefore the generator: a D axis current reference, which adjusts the excitation field of the generator, and a Q axis current reference which adjusts the torque produced by the generator.

The behaviour of the generator, RSC and control system was assessed in two different situations. Firstly, the response of the generator to a step change in the Q axis current reference was simulated using a simplified system model in Matlab / Simulink. This simulation showed that the rotor current vector was controlled in a stable, well damped manner with a time constant of approximately 20 ms. A second simulation of the same scenario was performed using a detailed VHDL model of the generator, converter and control systems using Mentor Graphics’ ModelSim software, with effectively identical results. An experimental prototype was constructed and subjected to the same reference current step, with similar results. The agreement between the simplified model, detailed model and experimental results demonstrated that the proposed Bit-Stream control system is capable of controlling the generator torque as required. Secondly, the response of the system to a
change in shaft speed from 750 RPM to 1250 RPM was simulated and tested experimentally. Once again, the simplified Matlab / Simulink model was used to establish the expected response of the system; the generator torque was regulated to a constant value independent of the generator speed. The response of the detailed VHDL model to an identical test scenario produced almost identical results, however the Bit-Stream speed measurement system is susceptible to clumping effects and requires post filtering. This is the only aspect of the Bit-Stream based RSC control system which was not accurately predicted by the Simulink models. The Bit-Stream control system was used to control a 2.6 kW DFIG prototype system, which demonstrated that the proposed control system is capable of regulating the rotor current vector and therefore torque of the generator over the entire operating speed range.
Chapter 8

Bit-Stream Control of Doubly Fed Induction Generator

A typical DFIG system consists of a generator, RSC, GSC and their associated control systems. Bit-Stream based control systems for the GSC and RSC were proposed and verified in Chapters 6 and 7, respectively. However, neither of these control systems is suited for stand alone applications; the control system of the GSC causes significant DC link voltage overshoot during startup, and the control system of the RSC only controls the magnetic flux and torque production of the generator. A DFIG system must regulate the speed, rather than the torque, of the generator and be capable of starting up without excessive current flow or voltage overshoot.

This chapter proposes a set of Bit-Stream based control systems which integrate the previously described RSC and GSC into a fully-functional DFIG system. A supervisory control system sequences the start up of the GSC, RSC and generator synchronisation process, as well as providing fault protection. Bit-Stream based control systems for speed control, excitation control and DC link soft charge are proposed.

A schematic diagram of the 2.6 kW DFIG system discussed in this chapter is shown in Fig. 8.1. The electrical equipment consists of a 400 V to 230 V transformer, generator, RSC and GSC. Contactors K1 and K2 provide inrush current limiting and generator synchronisation control, respectively. The following sections discuss the proposed Bit-Stream control systems and their Bit-Stream implementation. The proposed control system is then simulated using the MATLAB / Simulink modeling software to establish the expected behaviour of the DFIG system. Detailed simulations of the generator and proposed control systems are performed using a VHDL model and Mentor Graphics’ ModelSim to verify that the Bit-Stream control elements operate in the expected manner. Finally, a 2.6 kW experimental prototype is used to verify that the entire DFIG system, including generator, GSC, RSC and control systems, operates as expected.
8.1 DFIG Specifications

The proposed Bit-Stream control system for the DFIG is intended for use with the GSC described in Chapter 6 and the generator and RSC described in Chapter 7. The generator parameters are listed in Chapter 7.1 and Table 8.1 summarises the major parameters of the DFIG system.

8.2 Control System for DFIG

A control block diagram of the proposed control system for the DFIG is shown in Fig. 8.2 The proposed control system is intended for use as a supervisory control system to manage the behaviour of the GSC discussed in Chapter 6 and the RSC discussed in Chapter 7. It provides soft start functionality and manages the synchronisation and speed control of the generator. The control system provides supervisory control of the previously developed control systems for the GSC and RSC. A supervisor system sequences the operation of the GSC and RSC and provides protection for the GSC and generator. A generator excitation control system adjusts the D axis rotor current to provide inrush-free synchronisation of the generator, and unity power factor operation of the generator – at the stator terminals – during normal operation. A speed control system controls the speed by adjusting the Q axis rotor current reference.

8.2.1 Supervisory System

The supervisory system provides interlocking and protection functions to the DFIG system. It independently enables the GSC’s control system, RSC’s control system, synchronisation contactor K2 and speed control system. The supervisor accepts user commands and fault signals to control the operation of the generator.
8.2 Control System for DFIG

<table>
<thead>
<tr>
<th>Table 8.1: Summary of DFIG Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>Operating voltage</td>
</tr>
<tr>
<td>Operating frequency</td>
</tr>
<tr>
<td>Synchronous speed</td>
</tr>
<tr>
<td>Maximum operating speed</td>
</tr>
<tr>
<td>Minimum operating speed</td>
</tr>
<tr>
<td>Maximum generator torque</td>
</tr>
<tr>
<td>Maximum generator power</td>
</tr>
<tr>
<td>Voltage measurement gain</td>
</tr>
<tr>
<td>Current measurement gain</td>
</tr>
<tr>
<td>Speed measurement gain</td>
</tr>
</tbody>
</table>

A number of different fault signals are supplied to the supervisor; most of these result in the shutdown of the GSC, RSC and generator. Each fault signal is passed through a de-glitching filter, which ignores spurious fault signals with durations shorter than 3 $\mu s$. The fault signal is then latched to allow the operator to determine the cause of a shutdown. Table 8.2 lists the protection signals which are considered by the supervisor. Most faults result in a complete shutdown of the GSC and RSC and the opening of the stator contactor $K_2$, and are reset by the Clear command. However, the speed protection logic is only considered when the generator is operational; this allows testing of the GSC when the generator is not operational.

In the absence of faults, the supervisor is used to enable the various components of the DFIG system in a sequential manner using the state machine shown in Fig. 8.3. The user controls the DFIG system using four inputs: GSC, RSC, Synch and Clear. These inputs are used to change the DFIG operating modes and reset faults.

Initially, the supervisor waits for the auxiliary supply to stabilise. Following this, the supervisor moves to the Error state. The user asserts the Clear signal to move to the Ready state, from which the GSC may be enabled by asserting the GSC signal. After a brief delay for the DC link soft start procedure outlined in Section 8.2.2, the RSC is enabled and the generator is excited by
Table 8.2: DFIG Protection Signals

<table>
<thead>
<tr>
<th>Fault</th>
<th>Signal Name</th>
<th>Protection Action</th>
<th>Reset By</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSC over temperature</td>
<td>TEMP1</td>
<td>Complete shutdown</td>
<td>Clear</td>
</tr>
<tr>
<td>GSC IGBT error</td>
<td>ERROR1</td>
<td>Complete shutdown</td>
<td>Clear</td>
</tr>
<tr>
<td>RSC over temperature</td>
<td>TEMP2</td>
<td>Complete shutdown</td>
<td>Clear</td>
</tr>
<tr>
<td>RSC IGBT error</td>
<td>ERROR2</td>
<td>Complete shutdown</td>
<td>Clear</td>
</tr>
<tr>
<td>DC link over voltage</td>
<td>OVP</td>
<td>Complete shutdown</td>
<td>Clear</td>
</tr>
<tr>
<td>Auxiliary supply failure</td>
<td>AUX</td>
<td>Complete shutdown</td>
<td>Clear</td>
</tr>
<tr>
<td>Generator over speed</td>
<td>OSP</td>
<td>Generator shutdown</td>
<td>Clear or GSC</td>
</tr>
<tr>
<td>Generator under speed</td>
<td>USP</td>
<td>Generator shutdown</td>
<td>Clear or GSC</td>
</tr>
</tbody>
</table>

asserting the RSC command. The generator excitation procedure is described in Section 8.2.3. The generator can be synchronised to the grid using the Synch signal, at which point K2 is closed and the speed control loop is enabled. The supervisor is implemented using a standard finite state machine approach.

### 8.2.2 DC Link Soft Start

Before the GSC switches are enabled, the DC link is charged to approximately 330 V DC due to uncontrolled rectification through the IGBTs’ anti parallel diodes. If the DC link voltage controller gains listed in Chapter 6 are used to regulate the DC link voltage, a large voltage transient occurs and the DC link voltage may exceed the over voltage protection threshold of 565 V. To avoid this large transient event, the DC link voltage control system is operated with reduced gains – $K_{VP} = 3$, $K_{VI} = 0$ – for 250 ms to charge of the DC link without excessive current flow or DC link voltage overshoot. After the initial charging period has elapsed, the DC link control gains are restored to their normal values of $K_{VP} = 20$, $K_{VI} = 488$.

### 8.2.3 Excitation Control System

Although the WRIM can be directly connected to the AC grid without first being magnetised, undesirable inrush currents would flow as the magnetic field is established within the generator. A preferable approach is to establish this magnetic field before the generator contactor K2 is closed by injecting the appropriate magnetising current into the generator’s rotor windings. This process is called excitation.

The magnetisation of the generator can be investigated using the equivalent circuit shown in Fig. 8.4. The stator current is measured and the stator flux is estimated. The rotor current is actively controlled by the RSC using the control system described in Chapter 7. The stator current is measured and the stator flux is estimated. The rotor current is actively controlled by the RSC using the control system described in Chapter 7.

The magnetising current $I_M$ of the generator is calculated from the magnetising flux $\lambda_M$ according to (8.1). The magnetising flux can be calculated from the stator flux and current according to (8.2).

\[
I_M = \frac{\lambda_M}{L_M} \tag{8.1}
\]

\[
\lambda_M = \lambda_S - L_{LS}I_S \tag{8.2}
\]
During the excitation process, the stator current is zero, and all magnetisation current must be supplied by the rotor windings. Because no stator current flows, the stator and magnetisation fluxes are equal, which allows for direct calculation of the magnetising current:

$$I_R' = I_M = \frac{\lambda_S}{L_M} \tag{8.3}$$
However, during the initial excitation process the stator flux vector is not well known. Although closed loop control systems can be employed to actively control the stator voltage or flux vector before synchronisation occurs \cite{124,125}, a simple solution to this problem is to initially operate the stator flux estimator described in Chapter 7 using the grid voltage $V_G$ instead of the stator voltage $V_S$. Because $V_G$ is supplied externally, the ‘stator’ flux measurement is stable. During the synchronisation process the stator and grid voltage are matched, and so this approximation is acceptable. Once $K_2$ is closed, the stator and grid voltages are identical and the approximation becomes exact. The stator voltage sensors are only required to check that the generator is correctly synchronised before $K_2$ is closed.

Equation (8.3) can be rewritten in Cartesian form to decouple the D and Q axis components of the desired rotor current. As the stator flux estimator is specifically designed to orient the D axis of the reference frame to the stator flux, $\lambda_{SQ}$ is zero.

$$I'_R + jI'_Q = \frac{\lambda_{SD} + j\lambda_{SQ}}{L_M}$$

(8.4)

$$I'_R = \frac{\lambda_{SD}}{L_M}$$

(8.5)

$$I'_Q = 0$$

(8.6)

However, (8.5) is expressed in terms of true currents and fluxes, while the signals available in the Bit-Stream control system include measurement gains, the generator turns ratio and the scale factor of $2\pi f_G$ applied by the stator flux estimator, as discussed in Chapter 7. When these factors are considered, the excitation current reference $I'_R$ is set to:

$$I'_R = k_{EXC}\lambda_S$$

(8.7)

Where $k_{EXC}$ is the excitation scaling constant, and is given by:

$$k_{EXC} = \frac{K_{IM}}{2\pi f_G L_M N_{RS} K_{VM}}$$

(8.8)

The generator can be excited using the simple control system shown in Fig. 8.5. For operation with the generator parameters listed in Chapter 7, $k_{EXC}$ is equal to 1.069 units. This technique is extremely simple, but requires an exact measurement of the generator’s magnetising inductance and rotor angle. Feedback-based techniques such as those proposed in \cite{124,125} can be employed to synchronise the machine without exact measurements, but increase the complexity of the control system; it can be more difficult to develop extra control loops than to accurately measure the machine parameters.

When the generator is synchronised to the grid, the effective rotor impedance is equal to $R_R + R'_S + X_{LR} + X'_M$, as the grid impedance is very low. When the generator’s stator terminals are disconnected from the grid the effective impedance increases to $R_R + X_{LR} + X'_M$, which is much greater. The rotor current controller gains are increased from their normal settings during this time period to provide rapid control of the generator magnetising current.
8.2 Control System for DFIG

8.2.4 Speed Control System

The Bit-Stream based speed control system operates by varying the Q axis rotor current reference. The speed control loop is designed using the simplified generator model presented in Fig. 8.6. The Q axis rotor current control loop is modeled as a 20 ms time constant, in line with the response characteristics obtained in Chapter 7, and the generator is modeled as a torque source using Eq. (7.1).

The parameters of this simplified model are taken from the DFIG parameters listed in Table 8.1 and Chapter 7. For operation at 230 V AC, the stator flux of the generator $\lambda_S$ is approximately 0.60 Wb and the generator torque constant $k_\tau$ is 3.14 N.m/A.Wb.

The speed controller adjusts $I_{RQ}^*$, and therefore the generator torque, to adjust the rotor speed. A PI controller is used because it offers zero steady state error and is easy to tune. The controller’s proportional and integral gains are set based on the required transient response of the generator to changes in the speed reference or mechanical torque.

The Bit-Stream PI controller used in this system saturates at $+127$ Q or $-128$ Q, but in order to comply with the rotor current limits derived in Chapter 7, the PI controller output is limited to $\pm80$ Q. This is achieved using a post-scaling block with a gain of 80/127 as shown in Fig. 8.6. This post-scaling and the inherent Bit-Stream integrator gain $K_I'$ impact the selection of controller gains. The integral gain parameters are set deliver the minimum practical gain of 1/127, which yields an overall integral gain of 24.2 units. The proportional gain is set to 6.3 units to achieve a stable response to a speed reference step.

The response of this simplified speed control model to step changes in the speed reference signal $\omega_R^*$ and the mechanical torque input $\tau_M$ are shown in Fig. 8.7(a) and (b), respectively. In both cases, the DFIG system operates with an initial speed reference of 75 Q or 903 RPM and no mechanical input torque.

Fig. 8.7(a) shows the response of the simplified model to a speed reference step from 74 Q or 903 RPM to 90 Q or 1098 RPM. The speed follows the reference step with a rise time of 0.11 s and a 24% overshoot. This overshoot occurs due to the combined phase delays of the integrator within the control system and the characteristic response time of the rotor current control system. It

\[ \text{If a further reduction in gain is required a second scaling block may be placed in series with the input of the controller.} \]
could be reduced by decreasing the integral gain term, but this would difficult as the gain setting is already at a minimum and the PI controller would have to be modified. Increasing the proportional gain would not be particularly effective in this situation as the output of the PI is already saturated. In an experimental system, mechanical losses such as friction and windage are expected to provide mechanical damping effects and reduce this overshoot.

Fig. 8.7(b) shows the response of the simplified model to a mechanical input torque step from 0 Nm to 15 Nm. The speed control system does not include a torque sensor, and takes no immediate action. The additional input torque accelerates the generator, at which point the speed control system reduces the generator torque to return the generator to the desired speed. Speed fluctuations are inevitable in this situation; the speed control system can only respond to changing input torque after the speed has increased or decreased.

The speed control loop is enabled 50 ms after the synchronising contactor K2 is closed; this allows the contactor to close and the rotor current controllers to stabilise before the generator is required to produce torque. In a wind turbine generator application, the speed is usually adjusted using an MPPT algorithm to capture the maximum possible energy from the wind resource. As this thesis does not consider the characteristics of wind turbines or their governors, MPPT is not investigated.

### 8.3 Bit-Stream Control of DFIG System

The Bit-Stream based control system for the DFIG is developed by interconnecting the appropriate Bit-Stream control blocks and existing control systems for the GSC and RSC.

---

2 The sign convention used in this thesis holds that positive torques accelerate the generator and negative torques decelerate it.
The DFIG control system does not interface directly with either the GSC or RSC. Instead, the supervisory state machine described in Section 8.2.1 provides enabling, gain scheduling signals and current reference signals to the existing control systems for the RSC and GSC. The following sections describe the implementation of each control subsection: the supervisor system, DC link soft start, excitation current reference system and speed control system. Simplified schematics of each subsystem are presented in this chapter, and a DFIG control system schematic is presented in Appendix F.

8.3.1 Supervisory System

The supervisory system is implemented directly as a finite state machine using VHDL code. The state diagram of the supervisor is shown in Fig. 8.3.

8.3.2 DC Link Soft Start

The DC link soft start system is a simple extension to the existing control system for the GSC that is described in Chapter 6. The only modification to the original control system is the addition of a switched parameter unit to the DC link voltage control system, as shown in Fig. 8.8. A new control signal \( DC\_link\_gain \) is used to select between the soft start gains and the normal operation gains.

![Figure 8.8: Bit-Stream Implementation of the DC link soft start mechanism.](image)

8.3.3 Excitation Control System

The excitation control system is constructed using a simple Bit-Stream scaling element which implements the required gain \( k_{ESC} \) as a fractional gain of 77/72.

8.3.4 Speed Control System

The Bit-Stream speed control system for the DFIG is implemented using a standard Bit-Stream based PI controller, post scaling unit and a multiplexer as shown in Fig. 8.9. During the initial excitation process, \( I_{*RQ} \) is set to zero in accordance with (8.6). When the \( DFIG\_enable \) signal is asserted, \( I_{*RQ} \) is set by the speed controller. A 50 ms delay is applied between the command to close \( K2 \) and enabling the speed control loop to allow time for the contactor to close.

The Bit-Stream PI controller’s output naturally saturates at 127 Q and -128 Q. As discussed in Chapter 7, the Q axis rotor current must be less than 80 Q to avoid exceeding the rotor current...
rating. A scaling block is used to multiply the PI controller’s output by a fixed ratio of 80/127 which effectively provides this scaling. The proportional and integral gains of the PI controller are those shown in Fig. 8.9.

### 8.4 Simulation Results

This section presents the results of simulations which investigate the DC link soft start behaviour, generator excitation and synchronisation and speed control behaviour. These simulations are performed using the parameters listed in Table 8.1. Unless otherwise stated, the simulations are performed with an AC supply voltage, DC link voltage and generator speed of: 230 V L-L at the transformer’s secondary terminals, 450 V DC and 74 Q or 903 RPM, respectively.

For each scenario, two simulations are performed; firstly, a MATLAB/Simulink model which does not include sampling delays, quantisation errors or switching current ripple is used to establish the expected response of the DFIG system. Secondly, a detailed VHDL model of the Bit-Stream control system and DFIG equipment – which very precisely models the effects of sampling delays, quantisation errors and switching current ripple – is used to verify that the Bit-Stream control system is functionally equivalent to the Simulink control system. For convenience, the speed reference and measurement signals have been scaled from Bit-Stream Quanta to RPM.
8.4 Simulation Results

8.4.1 DC Link Soft Start

The simulated behaviour of the GSC during the DC link soft start is shown in Fig. 8.10. Initially, the generator, RSC and GSC are disabled and the DC link is charged to approximately 330 V DC by the uncontrolled rectification of the anti-parallel diodes within the GSC. At time $t = 50$ ms, the GSC is enabled with reduced DC link voltage controller gains. At time $t = 300$ ms the DC link voltage controller gains are restored to their full values.

The Matlab/Simulink model results presented in Fig. 8.10(a) indicate that the DC link is gently charged to approximately 440 V DC during the soft start period. The peak grid phase current is approximately 9 A, which is within the current rating of the GSC. At the end of the soft charge period there is a small DC link voltage error which is rapidly corrected. A small current transient is observed at this time. The VHDL model results presented in Fig. 8.10(b) are largely similar, except for the addition of switching current ripple and different phase angles of the grid current. These results show that the DC link soft charge control system successfully reduces peak current demand and DC link over voltage transients.

Figure 8.10: Simulated DC link soft charge procedure using (a) Simulink model and (b) VHDL model.
8.4.2 Excitation Control System

The simulated behaviour of the generator excitation control system during the synchronisation of
the generator is shown in Fig. 8.11. Initially the generator is rotating at 900 RPM, the RSC is
disabled and K2 is open. At time \( t = 100 \text{ ms} \), the RSC is enabled, and rotor currents are injected
into the generator to excite it. During this period the RSC current controller uses high gain settings
and the speed control system is disabled. At time \( t = 350 \text{ ms} \), the RSC current control gains are
reduced to their normal levels and K2 is closed.

The response of the Simulink model is shown in Fig. 8.11(a). Initially the rotor and stator
currents are zero, as expected. Once the RSC is enabled, rotor currents are injected into the
generator. At time \( t = 350 \text{ ms} \) the synchronising contactor closes. A small surge current of under
0.5 A flows through the stator windings, indicating that the synchronisation imposes little stress on
the generator. The speed control system is enabled at time \( t = 400 \text{ ms} \), which causes the generator
to produce torque, which in turn causes stator currents to flow.

The response of the VHDL model is shown in Fig. 8.11(b). Similar rotor currents are injected
into the generator during the excitation process. When the K2 closes at \( t = 350 \text{ ms} \), small stator
currents flow, and the rotor current ripple increases. This is due to the changing impedance of the
generator, as discussed in Section 8.2.3.

The low stator current inrush experienced by both the Simulink and VHDL models of the DFIG
shows that the proposed synchronisation method delivers a low-stress generator synchronisation.

![Figure 8.11: Simulated synchronisation of the DFIG to the AC grid using Simulink and VHDL models.](image-url)
8.4.3 Speed Control System

The performance of the speed control system is simulated under two difference scenarios. In both cases the speed reference and mechanical input torque are set to 903 RPM and 0 Nm, respectively. The response of the generator to a step change in speed reference from 74 Q or 903 PRM to 90 Q or 1098 RPM is simulated first to establish that the speed control loop is capable of tracking the speed reference. The response of the generator to a step change of input mechanical torque from 0 Nm to 15 Nm is then simulated to establish that the speed control system is capable of adjusting to different levels of input torque.

Fig. 8.12 shows the simulated response of the generator to step changes of the speed reference. Initially the generator operates at a constant speed of 903 RPM with zero turbine torque. At time $t = 1$ s, the speed reference is increased to 1098 RPM. The speed reference is returned to 903 RPM at time $t = 2.5$ s.

The response of the Simulink model is shown in Fig. 8.12(a). The generator initially operates at 903 RPM following the synchronisation procedure presented in Fig. 8.11(a). At time $t = 1$ s, the speed reference steps from 903 RPM to 1098 RPM. The generator accelerates smoothly, experiences a 20% speed overshoot and settles to a steady state speed of 1098 RPM after approximately 1 s, as predicted by the simplified speed control loop model discussed in Section 8.2.4. At time $t = 2.5$ s the speed reference is returned to 903 RPM. The generator then decelerates, experiences a 20% speed undershoot and settles to 903 RPM. The lower plot of Fig. 8.12(a) shows the Q axis current reference and actual current during the simulation. The current reference briefly saturates at 80 Q immediately after the reference step and the actual Q axis current is stable and well controlled.

The response of the VHDL model is shown in Fig. 8.12(b). It is essentially identical to the response of the Simulink model, and confirms that the Bit-Stream based control system is suitable for use in the speed control role.

Fig. 8.13 shows the simulated response of the generator to step changes of the input mechanical

![Figure 8.12](image_url)

**Figure 8.12:** Simulated response of the generator to a speed reference step using (a) Simulink and (b) VHDL models.
torque. Initially, the generator operates at a constant speed of 900 PRM with zero mechanical torque input. At time $t = 4$ s, the mechanical torque is increased to 15 Nm. The turbine torque is returned to 0 Nm at time $t = 5.5$ s.

The response of the Simulink model is shown in Fig. 8.13(a). The generator initially operates at 903 RPM following the speed controller test procedure presented in Fig. 8.12(a). At time $t = 4$ s, the mechanical torque input steps from zero to 15 Nm. The generator accelerates to a peak speed of 986 RPM, and the speed is restored in approximately 0.7 seconds. At time $t = 5.5$ s, the mechanical torque input is removed and the generator decelerates to a minimum speed of 821 RPM. Once again, the generator is restored to its original speed in approximately 0.7 seconds. This simulation shows that the speed control system is robust against changes in the mechanical torque supplied to the generator.

The response of the VHDL model is shown in Fig. 8.13(b). It is essentially identical to the response of the Simulink model, and confirms that the Bit-Stream based speed control system is suitable for use with varying mechanical torque inputs.

![Figure 8.13: Simulated response of the generator to a turbine torque step using (a) Simulink and (b) VHDL models.](image)

### 8.5 Experimental Results

This section presents experimental results taken from the experimental 2.6 kW DFIG system described in this and previous chapters. Figures 7.15 and 8.1 show a photograph and schematic of the DFIG system under test. A number of experimental tests were performed to assess the performance of the supervisory, DC link soft start, excitation and speed control systems. The parameters and settings of these experimental tests are identical to those used in the simulations discussed in Section 8.4. This allows for direct comparison of the experimental and simulated responses of the machine. In general, the response of the simulated and experimental DFIG systems were similar, which demonstrates that the proposed Bit-Stream control systems successfully provide
full control of the DFIG. The following sections discuss the behaviour of the supervisory, DC link soft start, excitation and speed control systems.

Although the WRIM used in this system is rated for operation with 400 V L-L on the stator winding, the DFIG operates with a reduced voltage of 230 V L-L for the reasons outlined in Section 7.1.

8.5.1 Supervisory System
The behaviour of the supervisory system was verified experimentally. The response to each fault signal was independently checked to verify that it caused the appropriate protective action to be taken according to Table 8.2.

8.5.2 DC Link Soft Start
The behaviour of the GSC during the initial DC link soft charge procedure was tested experimentally. As shown in Fig. 8.14, the initial DC link voltage is approximately 330 V DC. When the GSC is enabled, a peak phase current of 8.3 A is observed, in line with the predicted values. The DC bus then charges to approximately 430 V DC during the soft start period, and is rapidly charged to 452 V DC when the soft charge period ends. This result demonstrates that the proposed DC link soft start functionality prevents DC link voltage overshoot and reduces current inrush.

![Figure 8.14: Experimental test results of the DC link soft charge procedure.](image)

8.5.3 Excitation Control System
The behaviour of the excitation system was assessed by performing a generator synchronisation procedure. The generator was operated at 1000 RPM and excited using the RSC and proposed excitation control system. The synchronising contactor K2 command and stator phase currents are shown in Fig. 8.15. After a brief delay of approximately 28 ms the stator contactor closes, and a small inrush current flows to the stator. The peak inrush currents are under 2 A, which shows that the synchronisation operation places little stress on the generator.
The power factor of the generator’s stator windings was measured at a variety of speeds and mechanical torques, as listed in Table 8.3 and found to be above 0.98, which demonstrates that this simple excitation control technique is capable of providing excitation control. When the generator is producing no torque, very little active power flows, which causes the power factors to decrease. While this may appear to be a poor response, the actual reactive power flow at zero torque is only 60 VAr. An additional reactive power control loop could be added to the excitation control system to provide closed loop VAr control if desired.

### Table 8.3: Measured Power Factor of Stator Winding

<table>
<thead>
<tr>
<th>Generator Torque (Nm)</th>
<th>Speed (RPM)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>750</td>
</tr>
<tr>
<td>-20</td>
<td>0.983</td>
</tr>
<tr>
<td>-10</td>
<td>0.982</td>
</tr>
<tr>
<td>0</td>
<td>0.476</td>
</tr>
</tbody>
</table>

#### 8.5.4 Speed Control System

The behaviour of the speed control system was tested by experimentally testing the response of the generator to speed reference steps from 903 RPM to 1098 RPM. The experimental results of this test are shown in Fig. 8.16. A visual analysis of the speed response reveals two pieces of information: firstly, the speed measurement has a significant oscillating component and secondly, the average speed of the generator is controlled in a stable and well damped manner. Prior to this test, the mechanical torque $\tau_M$ was adjusted to compensate for the friction and windage losses of the prime mover and generator.

Further investigation of the experimental DFIG prototype revealed that the shaft to which the shaft angle encoder was fixed is misaligned and oscillates during operation. This in turn leads to a cyclic disturbance of the speed measurement which cannot be trimmed out. This disturbance is fed through to the Q axis rotor current reference due to the proportional gain term of the PI controller. However, the speed response is stable and well damped even when subjected to this disturbance, which demonstrates that the proposed Bit-Stream control systems are robust against speed measurement errors. The experimental results presented in Fig. 8.16(a) and (b) were...
imported into Matlab, filtered, scaled and re-plotted to yield the results shown in Fig. 8.16(c) and (d). The filtered speed signal is stable and well damped, exhibiting an overshoot of approximately 10%. This overshoot is somewhat lower than that predicted by simulations, and is likely due to the extra mechanical damping caused by the friction and windage of the motor/generator set, which was not modeled.

![Figures 8.16(a), 8.16(b), 8.16(c), and 8.16(d)](image)

**Figure 8.16:** Experimental response of the generator to a speed reference step from 903 RPM to 1098 RPM, unfiltered, from 1098 RPM to 903 RPM, unfiltered, from 903 RPM to 1098 RPM, filtered and from 1098 RPM to 903 RPM, filtered.

The response of the generator and its speed control system to step changes in mechanical input torque was then tested. Fig. 8.17 shows the response of the generator to a +15 Nm input torque step and then a -15 Nm input torque step. Prior to this test, the speed reference was set to 903 RPM and the mechanical torque $\tau_M$ was adjusted to compensate for the friction and windage of the prime mover and generator; the torque steps were applied on top of this compensating torque. As shown in Fig. 8.17(a) and 8.17(b), changes in the mechanical torque input cause brief deviations of the speed, which are removed by the speed control system. After the speed signals were filtered to yield the results shown in 8.17(c) and (d), the maximum and minimum transient speeds were determined to be approximately 980 and 820 RPM, respectively; the simulated and experimental response to mechanical torque input changes is very similar.
128  Bit-Stream Control of Doubly Fed Induction Generator

![Diagram](image)

**Figure 8.17:** Experimental response of the generator to a turbine torque step
from 0 Nm to 15 Nm, unfiltered, (b) from 15 Nm to 0 Nm, unfiltered, (c) from 0 Nm to 15 Nm, filtered and (d) from 15 Nm to 0 Nm, filtered.

### 8.5.5 FPGA Resource Consumption

The complete implementation of the proposed DFIG control system, consisting of the GSC, RSC and supervisory control systems discussed in this and previous chapters, consumes approximately 5800 logic elements and 12 kb of memory. Table 8.4 summarises the logic element consumption.

<table>
<thead>
<tr>
<th>Control Region</th>
<th>Component</th>
<th>Resource Utilisation</th>
<th>Memory Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control system for GSC</td>
<td></td>
<td>2782</td>
<td>4096</td>
</tr>
<tr>
<td>Control system for RSC</td>
<td></td>
<td>2495</td>
<td>8192</td>
</tr>
<tr>
<td>Supervisory State Machine</td>
<td></td>
<td>122</td>
<td>0</td>
</tr>
<tr>
<td>Excitation control system</td>
<td>Scaling unit</td>
<td>126</td>
<td>0</td>
</tr>
<tr>
<td>Speed Control System</td>
<td>Reference generator</td>
<td>58</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Error calculation</td>
<td>8</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>PI controller</td>
<td>310</td>
<td>0</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td>5779</td>
<td>12288</td>
</tr>
</tbody>
</table>
8.6 Summary

This chapter described the implementation of a Bit-Stream control system for a DFIG system. The proposed control system consists of a supervisory state machine, DC link soft start system, excitation control system and speed control system. The control systems for the GSC and RSC, which were proposed in Chapters 6 and 7, respectively, control the GSC and RSC currents according to references generated by the DFIG control blocks.

The proposed supervisory state machine provides a simple user interface, coordinates generator protection, and sequences the DFIG start up operations. A DC link soft start method was developed to prevent excessive DC link voltage overshoot during startup. The excitation control system was designed using the single phase equivalent circuit of the generator, and provides a very simple yet capable method for exciting the generator before synchronisation and then fully magnetising the generator during operation so that no reactive current flows through the generator’s stator windings. The speed control system was designed using a simplified model of the generator, and uses a PI controller to provide robust control of the speed.

The behaviour of the DFIG control system was assessed in four different situations. In each case, two types of simulation were performed: an idealised simulation was performed using Matlab/Simulink to establish the expected behaviour, followed by a detailed simulations using VHDL models and ModelSim to confirm that the control system provided the desired functionality. In each case, the behaviour of the Simulink and VHDL models was very similar, which demonstrates that the Bit-Stream control elements operate in a predictable manner.

The behaviour of the DC link soft start system was tested by simulation and experiment, and shown to reduce the AC inrush current to less than 10 A and reduce the DC link voltage overshoot to negligible levels.

The behaviour of the excitation system was tested by simulation and experiment and shown to correctly magnetise the generator. During the synchronisation process the stator current inrush was very low, and during operation the stator windings experienced minimal reactive power flow, which indicates that the excitation control system provides the correct magnetisation current to the generator. Reactive current can be supplied to the external grid by the GSC if required.

The speed control system of the generator has been simulated and experimentally tested. The speed control system provides stable closed-loop control of the speed, and its control parameters are selected using a simplified linear control model. When simulated using either this model or a detailed VHDL based model, the speed is stable and has zero steady state error. Experimental measurements confirm these results, with two differences: firstly, the generator’s angle encoder is attached to an off-center shaft which causes a cyclic disturbance of the speed measurement. That the speed control loop functions with such a disturbance shows that it is relatively insensitive to disturbances. Secondly, the measured speed overshoot is 10%, as opposed to the simulated value of 20%. This is likely due to mechanical damping factors such as friction and windage which were not included in the simulated generator models.

The experimental results presented in this chapter prove that the Bit-Stream control technique is suitable for the control of DFIG systems. Additionally, the response of the Simulink and VHDL based simulations are very similar to each other. This demonstrates that Bit-Stream control systems operate in a predictable manner, and that Simulink models, which are vastly more convenient than VHDL models for a designer to use, can be used to design any desired control systems.
Chapter 9

Conclusions

This chapter includes concluding remarks, a list of contributions to the field of Bit-Stream control arising from this thesis, and a discussion on possible avenues of future research.

9.1 Conclusions

DFIG systems are often used in wind power generation applications as they allow VSCF power generation without requiring large, expensive power converters. However, successful operation of the DFIG relies upon the control systems employed for its RSC and GSC. These control systems are typically implemented using microprocessors, which suffer from two weaknesses: the difficulty of developing control software which reliably coordinates the operation of numerous control tasks, and a steady decrease in the time available to execute the control algorithms. Hardware based control systems using FPGAs offer significant advantages in this application because the hardware control system can employ dedicated hardware for all control processes. The use of dedicated hardware means that there is no need to share computing resources and many tasks can be performed in parallel, which significantly reduces the time required to execute the control algorithm.

The aim of this thesis was to demonstrate control of a DFIG system using a hardware-based control system. The Bit-Stream technique was used to implement this control system as it is a convenient method for implementing control systems in FPGAs. Control systems can be constructed schematically using standard FPGA design tools; provided the required library components are available, the designer does not have to be familiar with HDLs. However, Bit-Stream control systems had only been used to control scalar systems prior to the research carried out in this thesis. The control of DFIGs requires complex vector control systems to manage the GSC and RSC and a number of new Bit-Stream control blocks were required to construct the required control functions. A new library of Bit-Stream blocks for vector control applications was developed in Chapter 3 to 5 of this thesis:

- Clarke Transformation units were developed to convert three phase measurement signals into two-phase vectors in the $\alpha\beta$ reference frame.
- Park’s Transformation units were developed to transform two-phase signals from the stationary $\alpha\beta$ to rotating $DQ$ reference frame.
- A three phase PLL, which measures the phase angle of the AC grid voltage, was developed and tested experimentally. The PLL is used in the control system for the GSC.
• A family of single-phase modulators which convert Bit-Stream signals to gate drive signals for single-phase inverters was developed. Experimental results from a 2 kW inverter demonstrate that these modulators offer superior output current THD levels than a standard PWM solution.

• A family of three-phase modulators which convert two-phase Bit-Stream reference signals into gate drive signals for three phase inverters was developed. Experimental results from a 6 kW inverter demonstrated that these modulators offer superior output current THD levels than a standard PWM solution.

These new Bit-Stream control blocks for vector control applications were used to develop a Bit-Stream based control system for the GSC, as discussed in Chapter 6. The GSC regulates the DC link voltage of the DFIG system by controlling transfer of power from the DC link to the AC grid and vice versa. The GSC can also be employed to inject reactive current into the AC grid if necessary, but this functionality was not used in this thesis. The proposed Bit-Stream control system was designed using continuous-time control models and simulated using both a simplified Simulink model and a detailed VHDL model. The results of simulations produced by these models were very similar; the principal difference was that the VHDL model included switching current ripple and the Simulink model did not. The performance of the proposed Bit-Stream control system was demonstrated experimentally using a prototype 2 kW GSC system. The GSC regulates the DC link voltage to approximately 450 V DC and has an efficiency of approximately 95% at full load. The output current has a spread-spectrum characteristic and a measured THD level of approximately 3.3%.

The Bit-Stream control system for the GSC was modified and expanded to control the RSC and generator. The PLL used in the control system of the GSC was replaced by a stator flux estimator and slip angle calculation system. By orienting the control system to the stator flux vector, this control system provides independent control of the torque- and flux-producing components of the rotor current vector, which naturally decouples the real and reactive power production of the generator. The control system, RSC and generator were simulated using both a simplified Simulink model and a detailed VHDL model. The simulation results produced by these two models were, in general, similar. However, the rotor speed measurement system proposed in this chapter is susceptible to Bit-Stream ‘clumping’ effects, which are easily mitigated but will only be apparent when a detailed simulation of the system is performed using the VHDL model. The proposed Bit-Stream control system for the RSC was tested experimentally using a 2.6 kW DFIG prototype, which has a rated speed range of 750 to 1250 RPM and maximum torque of 20 Nm. The control system for the RSC regulates the rotor current vector of the machine only, and does not apply speed or excitation control.

Chapter 8 presented a Bit-Stream control system for the DFIG. This control system adds a supervisor, generator speed controller and excitation control system to the existing control systems for the GSC and RSC. The supervisor provides interlocking and protection functions for the generator, and the excitation control system allows for simple, soft synchronisation of the generator to the AC grid. During operation, the generator speed is actively controlled and the magnetising current of the generator is provided by the RSC. These control systems were simulated using Simulink and VHDL models of a DFIG system. In general, the simulated responses of the Simulink and VHDL models are similar to each other. The proposed Bit-Stream control systems were tested experimentally using a 2.6 kW DFIG prototype. The machine protection systems were tested successfully, the DC link soft charge system was shown to reduce the inrush currents to under 10 A and soft synchronisation of the generator to the AC grid was demonstrated. Once synchronised,
the generator was subjected to step changes of the speed reference and mechanical torque input. The Bit-Stream control system successfully regulated the speed of the generator. The power factor of the generator, measured at the stator terminals, was maintained above 0.98 over the operating range of the machine.

9.2 Contributions

Three journal papers and seven conference papers were published following research undertaken in this thesis. These papers are:


9.3 Future Research Opportunities

This thesis has demonstrated a Bit-Stream based control system for DFIG applications. However, the control system was designed to control the generator with a balanced AC grid and no fault ride through requirements. Topics for future research into the control of DFIGs would be to enhance the control system to provide sensorless control, permit operation in an unbalanced AC grid and/or provide fault ride through capabilities.

Additionally, several potential improvements could be made to the Bit-Stream modulators proposed in Chapters 4 and 5. Both the single- and three-phase modulators produce spread spectrum outputs, which are desirable in terms of meeting harmonic current limits. However, the spread spectrum nature of the output current causes difficulties with resonant effects if $LCL$ type output filters are used; in this thesis the problem was overcome by using passive damping resistors, which is inefficient. Active damping methods, which employ the converter itself to damp out these resonances, are preferred as they require fewer components and reduce losses. A detailed study into the behaviour of the HDBS- and SVM-type modulators could potentially establish methods to apply active damping to an output $LCL$ filter, which would confer advantages in terms of size, cost and efficiency. The Bit-Stream SVM units proposed in Chapter 5 are not suitable for use in the overmodulation region because overmodulation leads to vastly increased switching frequencies. Research into methods to limit the maximum switching frequency in these cases would greatly facilitate the adoption of the technology.

Although the control systems developed in this thesis are intended for use in DFIG applications, they could be modified for use in a variety of vector control applications. The control system for the GSC could be used as a grid connected inverter or active rectifier without further modification. The control system for the RSC could be modified for use with squirrel cage induction machines or permanent magnet machines.

Finally, modifications to the core Bit-Stream library could yield dramatic improvements in terms of design verification and achievable sampling rates. The present Bit-Stream control elements operate using a main clock $ggclock$ and a second clock $gclock$. As a separate $gclock$ signal is generated within each Bit-Stream control block, and operations are performed on both the rising and falling edges of $gclock$, standard FPGA timing analysis tools do not produce predictable results. This would greatly hamper efforts to commercialise the technology as it is not currently possible to guarantee that a given Bit-Stream control system will meet specified timing requirements. A potential solution to this problem is to replace the $ggclock$ / $gclock$ approach with a single clock signal and to apply pipeline principles to the internal elements of the Bit-Stream system. This would allow for automatic and robust timing analysis, but would require a complete redesign of the Bit-Stream library.
Appendix A

Parameters for Bit-Stream PLL

The PLL is designed with a sampling rate $F_B$ of 500 kHz and a resolution $R$ of 8 bits. It is intended for use with a 120V RMS L-N grid at 45 – 55 Hz.

The analogue to Bit-Stream converters used for the PLL testing were PSoC-based. They have a gain $k_{VM} = 0.420 \text{ Q/V}$ and are isolated using ISO124 isolating op-amps.

The PLL design parameters are: $\omega_n = 31.42 \text{ rad/s}, \zeta = 0.7071, K_D = 107 \text{ Q/rad}, K_0 = 0.245 \text{ rad/s/Q}$ and $\omega_0 = 314.2 \text{ rad/s}$. From these values, the controller gains are: $\tau_1 = 0.0266 \text{ s}$, $\tau_2 = 0.0450 \text{ s}$, $K_P \text{ (target)} = 1.69$ and $K_I \text{ (target)} = 37.6$.

A Matlab script is used to find the gain parameters which offer the closest gains to those desired. In this case $K_{Pup} = 83$, $K_{Pdown} = 49$, $K_{Iup} = 1$, $K_{Idown} = 52$. The apparent gain of the $K_I$ pair is very small because the inherent integrator gain is approximately 1953 units per second; the overall proportional and integral gains are 1.694 and 37.56 units, respectively.

However, the PLL control loop has positive feedback, and these gains are apparently unstable. In practice, the non-linear nature of the phase detector allows the PLL to lock onto the grid voltage vector with a 180° phase shift: while $v_{GQ}$ is zero as expected, $v_{GD}$ is negative. This undesirable phase shift is corrected by inverting the gains by setting $K_{Pup} = -83$ and $K_{Iup} = -1$.

![Figure A.1: Additional vector transformation units: (a) Clarke Transformation with unity gain and (b) inverse Park’s Transformation.](image-url)
Appendix B

Analogue to Bit-Stream Converters

The Bit-Stream control systems discussed in this thesis operate directly on single bit signals provided by real-world sensors. Typically, these signals are analogue voltages and currents. As with the majority of digital control systems, analogue to digital converters are required to convert voltages and currents into the digital domain. Σ – ∆ ADCs are used for this task, as their output signals are directly compatible with the Bit-Stream control methodology [21].

A number of different ADC implementations have been employed in Bit-Stream control tasks: direct implementations using comparators and logic ICs; synthesis of ADCs using the programmable analogue blocks of PSoC devices; and commercially available Σ – ∆ ADC chips.

Direct implementations using comparators, flip flops and discrete integrators were originally investigated in [21]. These converters successfully convert analogue voltages to Bit-Streams, but require large amounts of PCB real estate and suffer from DC offset problems.

In order to address these concerns, an integrated converter was developed and implemented using Cypress Semiconductor’s PSoC system on chips. A single CY8C29466 device can be used to implement four analogue to Bit-Stream converters, each of which consumes vastly less PCB real estate. These ADCs typically require a 5 V supply and measure a signal of ±1.25 V on a 2.5 V offset. The designer may choose to sacrifice one ADC channel to provide a 2.5 V signal earth to the analogue electronics, which furnish signals to the converters. This effectively eliminates DC offsets on the signal inputs and allows for one set of three phase voltage signals to be digitised by a single IC. It should be noted that such ADCs are ratiometric; the PSoC supply rail is used as the reference and must be properly regulated.

A minimum of six current measurements are required to control the DFIG system: two grid side converter currents, two stator currents and two rotor currents. Ideally, nine current sensors would be used to measure all three phases, but this is not strictly necessary, as one of the phase currents may be inferred from the other two. The measurement of phase currents is complicated by two issues: firstly, the sensed current must be converted into a voltage for conversion and secondly, the current signals must be isolated. Early experiments with Hall Effect current transducers (LEM LTS 15-NP) and PSoC converters successfully performed the desired current to Bit-Stream conversion, but were bulky and suffered from DC offset problems.

1If current signals are fed through a closed loop Hall Effect sensor (such as the LEM LTS 15-NP) before the sensor is supplied with auxiliary/control power, the internal magnetic components may become permanently magnetised, leading to large DC offsets. The sensors can be returned to normal functionality by performing a degaussing procedure.
One of the strengths of the Bit-Stream control method is that each signal is represented by a single digital bit. The designer can therefore operate the $\Sigma - \Delta$ ADCs on the ‘hot’ side of the circuit, removing the need for costly analogue isolation components, and transfer one clock signal and one data signal across the isolation barrier in a digital form. A number of manufacturers produce integrated $\Sigma - \Delta$ ADCs which are well suited to measuring current signals. Table B.1 lists a number of the available converters. The listed converters all feature low-voltage differential inputs suitable for direct connection to current shunt resistors. They may include internal clock oscillators, or accept external clocks. For FPGA-based designs, it is important that all clocks be tightly controlled and aligned with each other, and so ADCs with external clock inputs are required. In addition, some devices are available with isolation barriers inside the chip. The Analog Devices AD7401(A) and the Avago ACPL-796J devices are suitable for this application because they both feature integral isolation barriers and external clock inputs. The AD7401A based cards offer superior accuracy in terms of gain and DC offset, and so are the preferred ADCs.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Input Range</th>
<th>Clock Source</th>
<th>Isolation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Avago</td>
<td>HCPL-786</td>
<td>±200 mV</td>
<td>Internal</td>
<td>Optocoupler</td>
</tr>
<tr>
<td>Avago</td>
<td>ACPL-796J</td>
<td>±200 mV</td>
<td>External</td>
<td>Optocoupler</td>
</tr>
<tr>
<td>Texas Instruments</td>
<td>AMC1203</td>
<td>±280 mV</td>
<td>Internal</td>
<td>Capacitor</td>
</tr>
<tr>
<td>Texas Instruments</td>
<td>ADS1203</td>
<td>±250 mV</td>
<td>Int. / Ext.</td>
<td>None</td>
</tr>
<tr>
<td>Analog Devices</td>
<td>AD7400A</td>
<td>±250 mV</td>
<td>Internal</td>
<td>Transformer</td>
</tr>
<tr>
<td>Analog Devices</td>
<td>AD7401A</td>
<td>±250 mV</td>
<td>External</td>
<td>Transformer</td>
</tr>
</tbody>
</table>

An integrated, isolated, voltage and current sensor card is shown in Fig. B.1(a). It packs a current shunt, voltage divider, two AD7401A ADCs and an isolated power supply into a total PCB area of 23 cm$^2$. When mounted on a base board, as shown in Fig. B.1(b) these card are stacked at 11 mm intervals.

Each measurement card requires a 3.3 V logic supply – this is supplied by the FPGA board – and isolated 5 V DC supply. The isolated supply will be directly connected to 400 V AC circuits and requires safety isolation. A large number of low cost, PCB mounted, isolated power supply modules are available, but these generally only provide a 1 kV isolation level. In order to comply with IEC isolation standards, the isolation methods used must provide at least 2.5 kV isolation to meet Category I (minimum) requirements. Ideally, the isolation barriers used should provide at least 4 kV of isolation to meet Category II requirements. Finally, seven (for minimum sensor configuration) to ten (for full sensor configuration) isolated supplies are required for the voltage and current measurements. Given the expense of purchasing suitable modules and the large number of channels required, an isolated current loop concept has been used to provide these isolated supplies. The concept is illustrated in Fig. B.2. A half-bridge inverter is ballasted with an inductor to provide a constant AC current$^2$ – in this case 600 mA RMS at 100 kHz – and small current transformers are used to tap off power for each sensor card. The current loop is fed through a hole and toroidal current transformer in each PCB to deliver multiple, regulated, outputs at low cost. The current loop conductor is insulated with heatshrink or silicone sleeving to provide the requisite degree of isolation.

Seven measurement cards were constructed and tested, with the results shown in Table B.2. The target gains are 4 Q/A for the current sensors (32 A full scale), 0.25 Q/V for the line voltage

---

$^2$A capacitor is placed in the circuit for DC blocking capabilities only. The current loop operates significantly above the LC resonant frequency.
measurements (512 V full scale) and 0.125 Q/V for the DC bus measurement (1024 V full scale). Note that the voltage dividers used in these measurement cards included trimming potentiometers, which allows for precise adjustment of the voltage gain. The current channels use 10 mΩ, 3 W shunt resistors (WSL3637R0100) and do not include any trimming.

<table>
<thead>
<tr>
<th>Location</th>
<th>Voltage Channel</th>
<th>Current Channel</th>
<th>Card Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC link</td>
<td>-0.1264 0.02</td>
<td>N/A</td>
<td>7</td>
</tr>
<tr>
<td>Grid A</td>
<td>-0.2495 0.00</td>
<td>3.988 0.00</td>
<td>1</td>
</tr>
<tr>
<td>Grid B</td>
<td>-0.2495 0.06</td>
<td>3.993 -0.01</td>
<td>9</td>
</tr>
<tr>
<td>Grid C</td>
<td>-0.2499 0.02</td>
<td>3.997 0.01</td>
<td>6</td>
</tr>
<tr>
<td>Stator A</td>
<td>-0.2499 0.01</td>
<td>3.987 -0.06</td>
<td>4</td>
</tr>
<tr>
<td>Stator B</td>
<td>-0.2500 0.01</td>
<td>4.001 0.00</td>
<td>10</td>
</tr>
<tr>
<td>Stator C</td>
<td>-0.2497 0.01</td>
<td>3.983 0.01</td>
<td>5</td>
</tr>
<tr>
<td>Rotor A</td>
<td>N/A N/A</td>
<td>3.988 0.00</td>
<td>2</td>
</tr>
<tr>
<td>Rotor B</td>
<td>N/A N/A</td>
<td>3.992 0.01</td>
<td>8</td>
</tr>
<tr>
<td>Rotor C</td>
<td>N/A N/A</td>
<td>3.981 -0.01</td>
<td>3</td>
</tr>
</tbody>
</table>
Appendix C

Prediction of HDBS Modulator Switching Frequency

The switching frequency of the HDBS modulator is indirectly determined by the modulation index and the modulator threshold. This appendix presents the derivations of approximate switching frequencies for the two-level and three-level HDBS modulator.

C.1 Two-level HDBS modulators

The average and maximum switching frequencies for the two-level HDBS modulator are derived as follows. This analysis assumes that the average switching frequency $F_S$ is much lower than the Bit-Stream sampling rate $F_B$, and approximates the discrete-time Bit-Stream modulator using continuous-time functions.

Consider the error trajectory shown in Fig. C.1. The gradients $m_1$ and $m_2$ are given by:

\[ m_1 = \frac{2u}{N} - 1 \] 
\[ m_2 = \frac{2u}{N} + 1 \] 

Where $u$ is the instantaneous voltage reference signal. Time periods $t_1$ and $t_2$ can be determined from:

\[ t_1 = \frac{-2H}{m_1} \frac{1}{F_B} \]
\[ t_1 = \frac{2H}{1 - \frac{2u}{N}} F_B \]  
\[ t_2 = \frac{2H}{m_2} F_B \]  
\[ t_2 = \frac{2H}{1 + \frac{2u}{N}} F_B \]  
\[ t_1 = t_1 + t_2 \]

The total switching period \( t_s \) is the sum of \( t_1 \) and \( t_2 \):

\[ t_s = \frac{2H}{F_B} \left( \frac{1}{1 - \frac{2u}{N}} + \frac{1}{1 + \frac{2u}{N}} \right) \]

\[ t_s = \frac{HN}{F_B} \frac{N}{N^2 - u^2} \]

The estimated instantaneous switching frequency \( \hat{f}_S \) is then given by:

\[ \hat{f}_S = \frac{N}{H N^2} u^2 F_B \]

From this equation, the maximum instantaneous switching frequency \( \hat{f}_{S_{\text{max}}} \) is calculated by setting \( u \) equal to zero:

\[ \hat{f}_{S_{\text{max}}} = \frac{N^2}{H N^2} F_B \]

\[ \hat{f}_{S_{\text{max}}} = \frac{F_B}{4H} \]

By observation, the switching frequency is zero when \( u \) is equal to \( N/2 \) or \( -N/2 \). The switching frequency curve is shown in Fig. C.2.

\[ f_r \]

\[ f_{S_{\text{max}}} \]

\[ -\frac{N}{2} \]

\[ \frac{N}{2} \]

\[ u \]

Figure C.2: Switching frequency curve for two-level HDBS modulator.

The average switching frequency is then estimated by averaging the average switching frequency during one fundamental period of the output frequency. It is assumed that the reference signal \( u \) is a sinusoid with a magnitude \( U \):

\[ u(\theta) = U \cos \theta \]  
\[ \hat{f}_{S_{\text{avg}}} \]
C.2 Three-level HDBS modulators

The average switching frequency $\hat{F}_S$ can then be estimated by:

$$\hat{F}_S = \frac{1}{2\pi} \int_0^{2\pi} \hat{f}_S(u(\theta))d\theta$$  (C.14)

$$\hat{F}_S = \frac{F_B}{2\pi H N^2} \int_0^{2\pi} \frac{N^2}{4} - (U \cos \theta)^2 d\theta$$  (C.15)

$$\hat{F}_S = \frac{F_B}{2\pi H N^2} \left[ \frac{N^2}{4} 2\pi - U^2 \int_0^{2\theta} \cos^2 \theta d\theta \right]$$  (C.16)

$$\hat{F}_S = \frac{F_B}{2\pi H N^2} \left[ \frac{N^2}{4} 2\pi - U^2 \pi \right]$$  (C.17)

$$\hat{F}_S = \frac{F_B}{2H} \left[ \frac{1}{2} - \frac{U^2}{N^2} \right], |U| \leq \frac{N}{2}$$  (C.18)

C.2 Three-level HDBS modulators

The derivation of the switching frequency estimates for the three-level HDBS modulator is very similar to that of the two-level modulator. The major difference lies in the gradients of the error trajectory. This derivation assumes that the modulator is operating with $u$ greater than zero; operation with $u$ less than zero can be inferred based on the inherent symmetry of the modulator.

$$m_1 = \frac{2u}{N} - 1$$  (C.19)

$$m_2 = \frac{2u}{N}$$  (C.20)

$$t_1 = \frac{-2H}{m_1} \frac{1}{F_B}$$  (C.21)

$$t_1 = \frac{2H}{1 - \frac{2u}{N}} \frac{1}{F_B}$$  (C.22)

$$t_2 = \frac{2H}{m_2} \frac{1}{F_B}$$  (C.23)

$$t_2 = \frac{2H}{\frac{2u}{N}} \frac{1}{F_B}$$  (C.24)

The total switching period $t_s$ is the sum of $t_1$ and $t_2$:

$$t_s = t_1 + t_2$$  (C.25)

$$t_s = \frac{2H}{F_B} \left( \frac{1}{1 - \frac{2u}{N}} + \frac{1}{\frac{2u}{N}} \right)$$  (C.26)

$$t_s = \frac{HN}{F_B} \frac{1}{u(1 - \frac{2u}{N})}$$  (C.27)
Hence:

\[ \hat{f}_S = \frac{u(1 - \frac{2}{N}u)}{HN}F_B \]  \hspace{1cm} (C.28)

By symmetry, it is expected that the switching frequency is given by the absolute value of the reference signal as shown in Fig. C.3. This can be expressed as:

\[ \hat{f}_S = \frac{|u|(1 - \frac{2}{N}|u|)}{HN}F_B \]  \hspace{1cm} (C.29)

The maximum switching frequency occurs for \(|u|\) equal to \(N/4\):

\[ \hat{f}_{S_{\text{max}}} = \frac{\frac{N}{4}(1 - \frac{2}{N}\frac{N}{4})}{HN}F_B \]  \hspace{1cm} (C.30)

\[ \hat{f}_{S_{\text{max}}} = \frac{F_B}{8H} \]  \hspace{1cm} (C.31)

![Figure C.3: Switching frequency curve for three-level HDBS modulator.](image)

The average switching frequency is determined in a similar manner to the two-level converter.

\[ \hat{F}_S = \frac{1}{2\pi} \int_0^{2\pi} \hat{f}_S(u(\theta))d\theta \]  \hspace{1cm} (C.32)

\[ \hat{F}_S = \frac{F_B}{2\pi HN} \int_0^{2\pi} \left( |u| - \frac{2}{N}u^2 \right) d\theta \]  \hspace{1cm} (C.33)

\[ \hat{F}_S = \frac{F_B}{2\pi HN} \int_0^{2\pi} \left( U \cos \theta \right) \left( |u| - \frac{2}{N}U^2 \right) d\theta \]  \hspace{1cm} (C.34)

\[ \hat{F}_S = \frac{F_B}{2\pi HN} \left( U \int_0^{2\pi} |\cos \theta|d\theta - \frac{2}{N}U^2 \int_0^{2\pi} \cos^2 \theta d\theta \right) \]  \hspace{1cm} (C.35)

\[ \hat{F}_S = \frac{F_B}{2\pi HN} \left( 4U - \frac{2\pi}{N}U^2 \right) \]  \hspace{1cm} (C.36)

\[ \hat{F}_S = \frac{UF_B}{HN} \left[ \frac{2}{\pi} - \frac{U}{N} \right], |U| \leq \frac{N}{2} \]  \hspace{1cm} (C.37)
Appendix D

Parameters Listings for Control of Grid Side Converter

This appendix lists the parameters of the grid side converter and its Bit-Stream control system. Table D.1 lists the electrical parameters of the system, and Tables D.2, D.3 and D.4 list the parameters of the Bit-Stream control system.

The complete schematic of the Bit-Stream control system for the grid side converter control system is presented in Appendix F.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter module</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SKM50GB123D SKM50GB123D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SKM50GB123D SKM50GB123D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IGBT module</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SKM50GB123D SKM50GB123D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SKM50GB123D SKM50GB123D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IGBT voltage rating</td>
<td>1200</td>
<td>V</td>
</tr>
<tr>
<td>IGBT current rating</td>
<td>50</td>
<td>A</td>
</tr>
<tr>
<td>Converter bus capacitance</td>
<td>1100</td>
<td>μF</td>
</tr>
<tr>
<td>Heat sink thermal resistance</td>
<td>0.13</td>
<td>K/W</td>
</tr>
<tr>
<td>Gate drive dead time $T_D$</td>
<td>4.4</td>
<td>μs</td>
</tr>
<tr>
<td>DC link capacitance $C_{DC}$</td>
<td>2200</td>
<td>μF</td>
</tr>
<tr>
<td>Main filter inductance $L$</td>
<td>10</td>
<td>mH</td>
</tr>
<tr>
<td>Main filter resistance $R_L$</td>
<td>0.25</td>
<td>Ω</td>
</tr>
<tr>
<td>Transformer leakage inductance (referred to secondary) $L_{lk}$</td>
<td>440</td>
<td>μH</td>
</tr>
<tr>
<td>Transformer winding resistance (referred to secondary) $R_X$</td>
<td>0.5</td>
<td>Ω</td>
</tr>
<tr>
<td>Line filter capacitance $C$</td>
<td>6.6</td>
<td>μF</td>
</tr>
<tr>
<td>Line damping capacitance $C_D$</td>
<td>20</td>
<td>μF</td>
</tr>
<tr>
<td>Line damping resistance $R_D$</td>
<td>6.8</td>
<td>Ω</td>
</tr>
<tr>
<td>Common mode line filter capacitance $C_C$</td>
<td>2.2</td>
<td>nF</td>
</tr>
<tr>
<td>Common mode line damping capacitance $C_{CD}$</td>
<td>4.7</td>
<td>nF</td>
</tr>
<tr>
<td>Common mode line damping resistance $R_{CD}$</td>
<td>970</td>
<td>Ω</td>
</tr>
</tbody>
</table>
### Table D.2: Bit-Stream parameters for GSC control system.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling rate $F_B$</td>
<td>1.25</td>
<td>MHz</td>
</tr>
<tr>
<td>Resolution $R$</td>
<td>8</td>
<td>bits</td>
</tr>
<tr>
<td>Voltage measurement gain $K_{VM}$</td>
<td>0.25</td>
<td>Q/V</td>
</tr>
<tr>
<td>Current measurement gain $K_{IM}$</td>
<td>8</td>
<td>Q/A</td>
</tr>
<tr>
<td>DC link measurement gain $K_{VDC}$</td>
<td>0.125</td>
<td>Q/Q</td>
</tr>
<tr>
<td>Inherent integrator gain $K'_I$</td>
<td>4883</td>
<td>per second</td>
</tr>
</tbody>
</table>

### Table D.3: Phase locked loop parameters for GSC control system.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase detector gain $K_D$</td>
<td>47.0</td>
<td>Q/rad</td>
</tr>
<tr>
<td>Operating frequency range</td>
<td>45 - 55</td>
<td>Hz</td>
</tr>
<tr>
<td>Maximum frequency command $F_{word,max}$</td>
<td>738</td>
<td></td>
</tr>
<tr>
<td>Minimum frequency command $F_{word,min}$</td>
<td>604</td>
<td></td>
</tr>
<tr>
<td>Oscillator gain $K_0$</td>
<td>0.2454</td>
<td>rad/s/Q</td>
</tr>
<tr>
<td>Closed loop bandwidth $\omega_n$</td>
<td>31.42</td>
<td>rad/s</td>
</tr>
<tr>
<td>Control loop damping $\zeta$</td>
<td>0.707</td>
<td></td>
</tr>
<tr>
<td>Time constant 1 $\tau_1$</td>
<td>0.0117</td>
<td>s</td>
</tr>
<tr>
<td>Time constant 2 $\tau_2$</td>
<td>0.0450</td>
<td>s</td>
</tr>
<tr>
<td>Proportional gain $K_P$</td>
<td>3.86</td>
<td></td>
</tr>
<tr>
<td>Integral gain $K_I$</td>
<td>85.8</td>
<td></td>
</tr>
<tr>
<td>Setting $K_{Pup}$</td>
<td>116</td>
<td></td>
</tr>
<tr>
<td>Setting $K_{Pdown}$</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>Setting $K_{Iup}$</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Setting $K_{Idown}$</td>
<td>113</td>
<td></td>
</tr>
</tbody>
</table>

### Table D.4: Controller parameters for GSC control system.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
<th>Fractional gain $k$</th>
<th>$m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulator gain coefficient $k_{MOD}$</td>
<td>$2/\sqrt{3}$</td>
<td>V/Q</td>
<td>85</td>
<td>50</td>
</tr>
<tr>
<td>Line voltage feed-forward gain $k_{FF}$</td>
<td>1.7</td>
<td>u</td>
<td>8</td>
<td>50</td>
</tr>
<tr>
<td>Cross axis decoupling gain $k_{DEC}$</td>
<td>0.16</td>
<td>u</td>
<td>25</td>
<td>50</td>
</tr>
<tr>
<td>Control mixing gain $k_{MIX}$</td>
<td>0.5</td>
<td>u</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Current control proportional gain $K_{IP}$</td>
<td>1.5</td>
<td>u</td>
<td>20</td>
<td>1</td>
</tr>
<tr>
<td>Current control integral gain $K_{II}$</td>
<td>3700</td>
<td>/s</td>
<td>60</td>
<td>79</td>
</tr>
<tr>
<td>DC link control proportional gain $K_{VP}$</td>
<td>20</td>
<td>u</td>
<td>20</td>
<td>1</td>
</tr>
<tr>
<td>DC link control integral gain $K_{VI}$</td>
<td>488</td>
<td>/s</td>
<td>1</td>
<td>10</td>
</tr>
</tbody>
</table>
Appendix E

Parameter Listings for Control of Rotor Side Converter

This appendix lists the parameters of the RSC and its control system. Table E.1 lists the electrical parameters of the RSC, and Tables E.2 to E.5 list the parameters of the Bit-Stream control system.

Table E.1: Rotor side converter parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter module</td>
<td>Semikron Semiteach</td>
<td></td>
</tr>
<tr>
<td>IGBT module</td>
<td>SKM50GB123D</td>
<td></td>
</tr>
<tr>
<td>IGBT voltage rating</td>
<td>1200</td>
<td>V</td>
</tr>
<tr>
<td>IGBT current rating</td>
<td>50</td>
<td>A</td>
</tr>
<tr>
<td>DC link capacitance</td>
<td>2200</td>
<td>µF</td>
</tr>
<tr>
<td>Heat sink thermal resistance</td>
<td>0.13</td>
<td>K/W</td>
</tr>
<tr>
<td>Gate drive dead time (T_D)</td>
<td>4.4</td>
<td>µs</td>
</tr>
</tbody>
</table>

Table E.2: Bit-Stream parameters for the RSC’s control system.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling rate (F_B)</td>
<td>1.25</td>
<td>MHz</td>
</tr>
<tr>
<td>Resolution (R)</td>
<td>8</td>
<td>bits</td>
</tr>
<tr>
<td>Voltage measurement gain (k_{VM})</td>
<td>0.25</td>
<td>Q/V</td>
</tr>
<tr>
<td>Current measurement gain (k_{IM})</td>
<td>8</td>
<td>Q/A</td>
</tr>
<tr>
<td>Modulator and inverter gain (k_{INV})</td>
<td>2.34</td>
<td>V/Q</td>
</tr>
<tr>
<td>Inherent integrator gain (k'_I)</td>
<td>4883</td>
<td>per second</td>
</tr>
</tbody>
</table>

Table E.3: Stator flux estimator parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>(k)</th>
<th>(m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stator resistance compensation (k_{RS})</td>
<td>0.0431</td>
<td>5</td>
<td>116</td>
</tr>
<tr>
<td>Filter gain (k_1)</td>
<td>0.0643</td>
<td>7</td>
<td>109</td>
</tr>
<tr>
<td>Filter gain (k_2)</td>
<td>488.3</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>Filter gain (k_3)</td>
<td>488.3</td>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>Filter gain (k_4)</td>
<td>1</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>
Table E.4: Slip Angle Calculation Parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Encoder resolution $N_L$</td>
<td>500</td>
<td>lines</td>
</tr>
<tr>
<td>Accumulator reset value</td>
<td>2000</td>
<td>counts</td>
</tr>
<tr>
<td>Angle scale factor</td>
<td>0.7676</td>
<td></td>
</tr>
<tr>
<td>Speed scale factor $N_S$</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Speed sensor gain $k_\omega$</td>
<td>1.278</td>
<td>rad/s/Q</td>
</tr>
</tbody>
</table>

Table E.5: Controller parameters for RSC.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
<th>Fractional gain $k$</th>
<th>$m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current control proportional gain $K_{RP}$</td>
<td>1</td>
<td>u</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Current control integral gain $K_{RI}$</td>
<td>38.4</td>
<td>/s</td>
<td>1</td>
<td>127</td>
</tr>
<tr>
<td>Control mixing gain $k_r$</td>
<td>0.25</td>
<td>u</td>
<td>1</td>
<td>4</td>
</tr>
</tbody>
</table>
Appendix F

Schematics

Figure F.1: Clock sources and supervisory control system.
Figure F.2: DC link control system.
Figure F.3: Measurement system for GSC.
Figure F.4: Current control system for GSC.
Figure F.5: Modulator for GSC.
Figure F.6: Stator voltage and current measurements.
Figure F.7: Slip angle calculation system.
Figure F.8: Rotor current measurements.
Figure F.9: Rotor current control system.

Figure F.10: Modulator for RSC.

Figure F.11: Excitation control system.
Speed Control System

Over / under speed protection

OSP @ 1380 RPM

USP @ 660 RPM

Speed Controller

Speed Reference

Manual torque reference

Figure F.12: Speed control system.
References


