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Design and Control of Modular Multilevel Converters

Baljit Singh Riar

Abstract

An increasing awareness of energy efficiency has led to the development of several improved semiconductor devices, power converter topologies and control schemes within the field of power electronics. Recent advances in multilevel converters, especially Modular Multilevel Converters (M2LCs), have improved upon existing power conversion technology in several aspects, including efficiency, power quality, modularity and reliability. There are, however, several challenges associated with the M2LC topology, which include capacitor voltage variations, voltage balancing, circulating currents and increased complexity of the overall control scheme. This thesis contributes to the ongoing research on the M2LC topology by proposing the following solutions to the aforementioned challenges.

Typically, schemes with cascaded control loops have been used to control M2LCs and these schemes could affect the performance of the converter. Model Predictive Direct Current Control (MPDCC), which has a single loop, is proposed to keep load currents within tight bounds, while minimising both capacitor voltage variations and circulating currents. Moreover, the width of the current bounds sets the level of Total Harmonic Distortion (THD) of the currents. Simulated and experimental results for a 860-VA prototype M2LC are presented to demonstrate the effectiveness of the MPDCC scheme.

A modified M2LC topology that employs a full-bridge module in each arm is proposed to minimise both circulating currents and capacitor voltage variations. The modified topology allows for decoupled control of the load and circulating currents, where the load and circulating currents are controlled by the half-bridge and full-bridge modules, respectively. A comparative investigation with respect to a conventional topology, using theoretical as well as experimental results for a 800-VA prototype converter, reveals that the modified topology offers superior performance.

Capacitor voltage variations are difficult to control within the conventional M2LC, because the variations are coupled to arm currents and load currents. An alternative M2LC topology that uses Inductive Power Transfer (IPT) technology is proposed to simplify the control of the capacitor voltages. The IPT system keeps the voltage variations within bounds irrespective of the operating conditions of the converter. The feasibility of the concept and improvements achieved with the alternative topology are demonstrated using simulations of a 800-VA converter.
To my family.
Acknowledgements

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Baljit Singh Riar
25 February, 2015
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Symbols and Acronyms

Mathematical notation

- $e^x$: Exponent of the variable $x$
- $\min$: Minimum
- $\mathbb{N}_0$: Non-negative integers
- $\in$: Is element of (belongs to)
- $\subset$: Subset
- $\mathbb{R}^n$: Space of $n$-dimensional real vectors
- $\mathbb{R}^{n \times m}$: Space of $n$ by $m$ real matrices
- $\top$: Transpose
- $x$: Column vector
- $x^\top$: Row vector
- $X$: Matrix
- $\frac{dx}{dt}$: Time derivative of the variable $x$
- $||x||_1$: 1-norm of vector $x$ (sum of the absolute elements)
- $||x||_2$: 2-norm of vector $x$ (Euclidean norm)

Symbols

- $C$: Module capacitance
- $C_{vcm}$: VCM capacitance
- $C_{si}$: IPT pickup compensation capacitance
- $f$: Grid frequency
- $f_T$: IPT track current frequency
- $f_{sw}$: Average switching frequency
- $i_r$: Phase current, $r \in \{a, b, c\}$
- $i_{ref,r}$: Phase current reference, $r \in \{a, b, c\}$
- $i_{cir,r}$: Circulating current, $r \in \{a, b, c\}$
- $i_{rq}$: Arm current, $r \in \{a, b, c\}$, $q \in \{T, B\}$
- $i_{DC}$: DC-link current
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</tr>
<tr>
<td>$i_{sc}$</td>
<td>Short circuit current of pickup inductor</td>
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<td>$J$</td>
<td>Set of indices</td>
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<td>$j$</td>
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<td>$\delta$</td>
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<td>AC</td>
<td>Alternating Current</td>
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<tr>
<td>A/D, ADC</td>
<td>Analogue to Digital Converter</td>
</tr>
<tr>
<td>CHC</td>
<td>Cascaded H-Bridge Converter</td>
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<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DCC</td>
<td>Diode Clamped Converter</td>
</tr>
<tr>
<td>DSC</td>
<td>Digital Signal Controller</td>
</tr>
<tr>
<td>FCC</td>
<td>Flying Capacitor Converter</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
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<tr>
<td>HVDC</td>
<td>High Voltage Direct Current</td>
</tr>
<tr>
<td>IPT</td>
<td>Inductive Power Transfer</td>
</tr>
<tr>
<td>LS</td>
<td>Level-Shifted</td>
</tr>
<tr>
<td>LCC</td>
<td>Line-Commutated Converter</td>
</tr>
<tr>
<td>M2LC</td>
<td>Modular Multilevel Converter</td>
</tr>
<tr>
<td>M2LC-IPT</td>
<td>Modular Multilevel Converter with Inductive Power Transfer</td>
</tr>
<tr>
<td>M2LC-VCM</td>
<td>Modular Multilevel Converter with Voltage Correcting Modules</td>
</tr>
<tr>
<td>MIMO</td>
<td>Multi-Input Multi-Output</td>
</tr>
<tr>
<td>MPC</td>
<td>Model Predictive Control</td>
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<tr>
<td>MPDCC</td>
<td>Model Predictive Direct Current Control</td>
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<tr>
<td>NPC</td>
<td>Neutral Point Clamped</td>
</tr>
<tr>
<td>OPP</td>
<td>Optimised Pulse Pattern</td>
</tr>
<tr>
<td>PD</td>
<td>Phase Disposition</td>
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<td>PI</td>
<td>Proportional-Integral</td>
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<td>PS</td>
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<td>SISO</td>
<td>Single-Input Single-Output</td>
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<td>SHE</td>
<td>Selective Harmonic Elimination</td>
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<td>Total Harmonic Distortion</td>
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<td>Volt-Amp</td>
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<td>VCM</td>
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<td>VOC</td>
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<td>Voltage Source Converter</td>
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Chapters 3 and 4 are based on the journal paper "Model Predictive Direct Current Control of Modular Multilevel Converters: Modelling, Analysis and Experimental Evaluation", which is published in IEEE Transactions on Power Electronics, 2014.

### Co-AUTHORS

<table>
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<tr>
<td>Tobias Geyer</td>
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<tr>
<td>Udaya Madawala</td>
<td>Provided direction on the scope and structure of the analysis, and proofread the manuscript.</td>
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**Certification by Co-Authors**

The undersigned hereby certify that:

- the above statement correctly reflects the nature and extent of the PhD candidate’s contribution to this work, and the nature of the contribution of each of the co-authors; and
- in cases where the PhD candidate was the lead author of the work that the candidate wrote the text.

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<tr>
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Chapters 5 and 6 are based on the journal paper "Decoupled control of Modular Multilevel Converters using Voltage Correcting Modules", which is published in IEEE Transactions on Power Electronics, 2014.

| Nature of contribution by PhD candidate | Proposed M2LC-VCM concept, modelled the converter, performed the experiments, interpreted the results and wrote the manuscript. |
| Extent of contribution by PhD candidate (%) | 70 |

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<tr>
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Chapter 1

Introduction

1.1 Background

The green economy, which promotes the efficient generation and consumption of energy with minimum environmental impact, is a key part of sustainable living [1]. Coordinated measures are needed to realise the green economy, and one such measure is to adopt renewable energy systems. Power electronic converters, which are used in a wide range of applications such as energy conversion, machine drives and renewable energy systems, have become vital components within electrical power networks. The increasing demand for highly efficient, reliable and compact power converters means that a number of converter topologies have evolved with improved efficiency, reliability and power-to-weight ratio [2].

Line-Commutated Converters (LCCs) and Current-Source Converters (CSCs) have been used in the past in various high-power industrial applications [3]. Although these converters feature low maintenance costs, high efficiencies and simple topologies, their applications are decreasing, because of their dependence on reactive power for proper operation [4]. The advent of self-commutated devices such as the Insulated-Gate Bipolar Transistor (IGBT), Gate-Turn-Off (GTO) thyristor and Gate-Commutated Thyristor (GCT) has triggered the development of Voltage-Source Converters (VSCs) [5], [6]. In modern systems, VSCs have become more popular than LCCs and CSCs, because they feature fast dynamic response times, control of both real and reactive output power, and the capability to supply power to weak electrical networks [7].

For high-power applications, VSCs can be categorised as two-level VSCs and multi-level (i.e. more than two levels) VSCs [8]. Two-level VSCs have a simple topology, with a series- and parallel-connection of switches being used to achieve the desired voltage- and current-ratings. Moreover, additional components are required to ensure that the voltage stress on series connected devices is equal. State-of-the-art control schemes and
modulation strategies can easily be used to control a two-level VSC. However, the two-level converter requires large filters, which are bulky, to achieve output current waveforms of acceptable quality. Multilevel VSCs yield output waveforms with lower harmonic distortion and, therefore, can operate with smaller filters. Both the topology and required control schemes of multilevel VSCs, however, are more complex than those of two-level VSCs. Nonetheless, in high-power applications, the advantages of multilevel VSCs outweigh their disadvantages and, as a result, these converters have become more popular than two-level VSCs. Consequently, multilevel converters can be found in a number of applications such as grid-connected systems, machine drives, renewable energy systems and transportation systems [2].

Various multilevel VSC topologies have been developed, but only a few, such as the Diode Clamped Converter (DCC), Flying Capacitor Converter (FCC), Cascaded H-Bridge Converter (CHC) and Modular Multilevel Converter (M2LC), have become popular in high-power applications.

The DCC topology uses an arrangement of diodes with cascaded capacitors to synthesise an AC voltage waveform, using multiple levels of voltages [9]. With the DCC topology, the capacitor voltages need to be kept balanced so as to prevent uneven voltage variations across the switches [10], [11]. The reverse blocking voltage of the clamping diodes becomes uneven as the number of levels increases. Therefore, series-connected diodes along with some external circuitry are used to maintain an equal voltage stress across each diode [12]. The clamping diodes can also be replaced with switches that control the neutral current and, consequently, improve the power loss distribution across the switches [13], [14]. Although the DCC can be configured to produce any number of voltage levels, only the three-level DCC, which is commonly known as the Neutral-Point-Clamped (NPC) converter, has widely been used in industrial applications, because of the difficulties relating to capacitor voltage balancing and uneven blocking voltages.

The FCC uses an arrangement of capacitors to synthesise an AC voltage waveform, using multiple voltage levels. The topology of the FCC is similar to that of the DCC and uses capacitors for voltage clamping. Therefore, the topology is also known as the capacitor clamped converter. The topology allows redundant switching operations, which enable the same output voltage level to be realised with a number of switching combinations. These redundant combinations are used to balance the capacitor voltages within the FCC. Although the FCC has a modular structure, it is only found in a limited number of high-power industrial applications, because both the switching frequency and the complexity of the capacitor voltage balancing increase with the number of voltage levels [12].

The CHC uses a series connection of H-bridge modules to synthesise an output voltage waveform with multiple levels. A CHC with $n$ H-bridge modules can produce $2n + 1$
1.2 Research Objectives

In order to alleviate the aforementioned disadvantages, this thesis proposes a Model Predictive Direct Current Control (MPDCC) scheme and topological changes to M2LCs. This thesis demonstrates that by employing MPDCC, a single control loop can be used
to minimise both circulating currents and voltage variations, while also controlling the load currents. The proposed MPDCC scheme is also shown to improve the dynamic performance of the M2LC.

Additionally, this thesis proposes a modified M2LC topology that employs full-bridge modules to minimise both circulating currents and voltage variations. The thesis also demonstrates that the modified topology with full-bridge modules allows for simple and decoupled control of the load and circulating currents without compromising the performance of the M2LC.

Furthermore, another modified M2LC topology is proposed that employs Inductive Power Transfer (IPT) technology to maintain capacitor voltage variations within bounds. The thesis presents the concept of a modified topology with IPT and validates that the topology decouples the control of the load current and capacitor voltages.

Several case studies are used to evaluate the performance of proposed solutions, and the results are presented in detail with accompanying discussion. Both of the modified M2LC topologies that are proposed have not been reported prior to the research undertaken in this thesis. Moreover, these proposed methods simplify the control scheme of M2LCs.

### 1.3 Thesis Organisation

The subsequent chapters of this thesis are arranged as follows:

**Chapter 2 - Modular Multilevel Converters.** This chapter presents an overview of the operation of M2LCs, followed by a description of circulating currents, which are unique to the M2LC topology. A survey of publications on the control of capacitor voltages, circulating and load currents is then presented. The modulation strategies that have been used to generate pulse patterns for M2LC switches are also discussed. Advantages and disadvantages of the control schemes and modulation strategies are discussed. Moreover, a review of the modelling methods and design process for M2LCs is given. Finally, current research trends and applications of M2LCs are presented. This chapter presents previous work in the area and demonstrates the need for the proposed solutions.

**Chapter 3 - Model Predictive Direct Current Control of Modular Multilevel Converters: Concept.** A MPDCC scheme for M2LCs is proposed in this chapter. Both continuous- and discrete-time models of a M2LC are derived to predict the behaviour of the capacitor voltages, load- and circulating-currents over time. The MPDCC algorithm, which is used to keep the load currents within prescribed bounds and to minimise both the voltage variations and circulating currents, is explained. In addition, a mathematical function of the load current THD is derived to reveal that the THD is a linear function of the current bound width.
Chapter 4 - Model Predictive Direct Current Control of Modular Multilevel Converters: Performance Analysis. This chapter evaluates the performance of the MPDCC scheme using simulations of a three-phase M2LC and compares the performance with that of a Voltage-Oriented Control (VOC) scheme, which is a popular scheme for grid-connected multilevel converters. Results are presented to demonstrate that the MPDCC scheme provides a very fast current response during transient conditions, such as a sudden change in reference values. Detailed simulation and experimental results for a 860-VA M2LC are provided to validate practical feasibility of the proposed MPDCC scheme. Since the MPDCC algorithm is computationally expensive, a simple approach is discussed to reduce the computational time.

Chapter 5 - Modular Multilevel Converter with Voltage Correcting Modules: Concept. A modified M2LC topology is proposed in order to minimise circulating currents and variations in capacitor voltages. The proposed topology incorporates a full-bridge module, referred to as Voltage Correcting Module (VCM), into each arm of the converter to compensate for the voltage difference in the phase-leg. The solution simplifies and decouples the control of the circulating currents from that of the load currents. Two controllers are developed to control the VCMs, in order to minimise the circulating currents. Detailed and lumped models of the topology are also derived to predict the behaviour of capacitor voltages and arm currents.

Chapter 6 - Modular Multilevel Converter with Voltage Correcting Modules: Performance Analysis. This chapter analyses the improvement in performance that is achieved with VCMs in terms of reduction in circulating currents and capacitor voltage variations. Simulation and experimental results for an 800-VA M2LC are provided to validate the proposed concept and models. The models are also used to investigate the effectiveness of the VCMs for a range of circuit parameters.

Chapter 7 - A Modular Multilevel Converter based on Inductive Power Transfer Technology. This chapter proposes a modified topology that employs IPT technology to maintain the capacitor voltages within bounds. The operating principles of the modified topology, which also allows for wireless power transfer between modules, is presented. Simulated results for an 800-VA M2LC with IPT are presented to demonstrate the feasibility of the proposed concept. A comparative investigation with respect to the M2LC-VCM topology reveals that the M2LC-IPT topology offers superior performance in certain aspects, such as improved reliability and the ability to control voltage variations.

Chapter 8 - Conclusions. This chapter concludes the research, summarises the contributions of the thesis and briefly discusses directions for future research.
Chapter 2

Modular Multilevel Converters

2.1 Introduction

Recently, M2LC topology, which features modularity, scalability, reduced voltage rating of switches and redundant switching operations, has become popular in medium to high voltage applications [15], [16]. The M2LC has been used in various applications such as High-Voltage Direct Current (HVDC) transmission [4], [18], machine drives [19], [20], traction motors [21], [22] and STATic synchronous COMpensators (STATCOMs) [23]. Both the academic and industrial power electronics communities have acknowledged the importance of the M2LC in high-power medium- to high-voltage applications, and several control schemes and modulation strategies have been proposed to improve the performance of the converter [24]–[27]. Moreover, various modelling techniques have also been proposed to accurately predict the behaviour of the converter.

The primary feature of the M2LC, as shown in Fig. 2.1, is a series connection of a large number of identical modules, where the module is typically configured as a two-level voltage source converter. The modular structure of the M2LC offers a number of advantages, with a few of these listed as follows:

1. The number of output voltage levels can be increased easily by adding more modules to the arm of a converter. The Total Harmonic Distortion (THD) of the output voltage decreases with the increased number of levels, thus improving the quality of the voltage waveform. With the reduced THD, the M2LC can be operated without output filters, which are usually bulky.

2. For a fixed DC-link voltage, the voltage across each module is inversely proportional to the number of modules. Therefore, in high-voltage applications, semiconductor devices with low- to medium-voltage ratings, which are readily available, can be used in M2LCs with a large number of modules.
3. A DC-link capacitor is replaced with a number of module capacitors, where the voltage across each capacitor is lower than that of the total DC-link voltage. Moreover, the topology does not require any complex transformer setup, as in the case of Cascaded H-Bridge Converters (CHCs), for supplying power to the capacitors.

4. Unlike Diode Clamped Converters (DCCs), the currents in each phase-leg are continuous and generate very low Electromagnetic Interferences (EMIs). The voltage supply of the M2LC therefore does not need expensive cables/bars with low inductance.

5. The topology features redundant switching combinations for certain output voltages. Thus, there are several module combinations that generate certain output voltage levels, and the redundancy can be exploited for the balancing of the capacitor voltages.

2.2 Fundamentals

A typical M2LC is shown in Fig. 2.1, where each phase-leg of the converter is divided into two halves, called arms. Each arm consists of $N$ modules, which are represented as
$M_{rn}, r \in \{a, b, c\}, n \in \{1, 2, \ldots, 2N\}$, a resistor, $R$, which models conduction losses, and an arm inductor, $L$. The number of modules connected in each arm is varied sinusoidally in order to produce an output voltage with multiple levels [21], [28].

### 2.2.1 Operating Principles

Fig. 2.2 shows the topology of a single-phase leg of a three-level M2LC. The operation of the M2LC is described by considering half-bridge modules, where the module capacitors are assumed to be charged to a voltage of $V_{DC}/2$. The converter under consideration produces three voltage levels, $V_{DC}/2$, 0 and $-V_{DC}/2$. In order to produce an output voltage, $v_a$, of $V_{DC}/2$, all of the modules in the top arm are bypassed whereas the modules in the bottom arm are connected\(^1\). To produce an output voltage of $-V_{DC}/2$, all of the modules in the top arm are connected and the modules in the bottom arm are bypassed. By connecting one module in each arm, the converter produces an output voltage of 0. The switching states of the modules of the three-level M2LC are summarised in Table 2.1.

![Figure 2.2: Three-level modular multilevel converter.](image)

It can be observed from Table 2.1 that the voltage level 0 can be obtained by four module combinations. Thus, there are four redundant states. For $N$ modules, the maximum number of output voltage levels can be found as $N + 1$. Table 2.2 shows the maximum

\(^1\)A module is considered to be bypassed when the voltage inserted by the module is zero. A module is considered to be connected when it inserts a voltage that is equal to the capacitor voltage.
number of combinations, \( \binom{N}{g}^2 = \left( \frac{N!}{(N-g)!g!} \right)^2 \), or the redundant states that result in the same output voltage level, where the levels are numbered as \( l \in \{1, 2, 3, \ldots, N+1\} \). For a large \( N \), the capacitor voltages can be better balanced by utilising the large number of redundant states without affecting the output voltage. The output voltage, \( v_r \), that corresponds to the level number is given by

\[
v_r = V_{DC} \left( \frac{1}{2} - \frac{l - 1}{N} \right), \quad l \in \{1, 2, 3, \ldots, N+1\}
\]

### Table 2.2: Module combinations of a \( N \)-level M2LC.

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>Number of Combinations</th>
<th>Level Number ( l )</th>
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<tbody>
<tr>
<td>( \frac{V_{DC}}{2} )</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>( V_{DC} \left( \frac{1}{2} - \frac{1}{N} \right) )</td>
<td>( \binom{N}{1}^2 )</td>
<td>2</td>
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<tr>
<td>( V_{DC} \left( \frac{1}{2} - \frac{2}{N} \right) )</td>
<td>( \binom{N}{2}^2 )</td>
<td>3</td>
</tr>
<tr>
<td>( V_{DC} \left( \frac{1}{2} - \frac{3}{N} \right) )</td>
<td>( \binom{N}{3}^2 )</td>
<td>4</td>
</tr>
<tr>
<td>( \vdots )</td>
<td>( \vdots )</td>
<td>( \vdots )</td>
</tr>
<tr>
<td>( -\frac{V_{DC}}{2} )</td>
<td>1</td>
<td>( N+1 )</td>
</tr>
</tbody>
</table>

### 2.2.2 Module Configuration

A typical module, as shown in Fig. 2.3, is configured as a half-bridge converter with a capacitor, \( C \), connected to its terminals. The half-bridge module has two switching states \( u_{rn} \in \{0, 1\} \), where 1 means that the capacitor is connected to the circuit, i.e. the switch \( S_{rn,1} \) is turned on. The turn-on operations of the switches in a module are complementary to one another. Since the voltage inserted by a half-bridge module, \( v_{rn} \), is always positive, these modules can only be used with an M2LC connected to a DC-link. The modules can
also be configured as full-bridge converters which allows for the M2LC to be connected to both a DC- or an AC-link. The number of switches of the full-bridge module, however, is double that of the half-bridge module.

![Diagram of M2LC module configurations](image)

Figure 2.3: M2LC module configurations.

For a given number of modules, the number of output voltage levels can be increased by changing the module configuration to NPC or FCC converter, as shown in Fig. 2.3, [29]. However, the complexity of the control scheme increases with such configurations. In [30], two half-bridge modules are connected in such a way as to limit the arm current during faults. Each configuration has its own advantages and disadvantages, and the selection of the particular configuration depends on the design objectives.

## 2.3 Circulating Currents

The circulating currents, which are labelled as $i_{\text{cir},a}$ in Fig. 2.2, are inherent to the M2LC topology. These currents do not affect the load current, but circulate within the converter as common-mode currents. The arm currents, $i_{rq}$, $r \in \{a, b, c\}$, $q \in \{T, B\}$, comprise load and circulating currents. For a balanced system, the relationship between the arm current, $i_{rq}$, circulating current, $i_{\text{cir},r}$, and load current, $i_r$, can be defined for a given
phase-leg as

\[ i_{rT} = i_{cir,r} + \frac{i_r}{2} \quad (2.2) \]
\[ i_{rB} = i_{cir,r} - \frac{i_r}{2}. \quad (2.3) \]

The circulating current in a phase-leg is the average of two arm currents

\[ i_{cir,r} = \frac{i_{rT} + i_{rB}}{2} = \overline{i_{cir,r}} + \sum_{h=1}^{\infty} i_{h,r} \quad (2.4) \]

The circulating current in each phase-leg consists of a DC/average component, \( \overline{i_{cir,r}} \), and harmonic component, \( i_{h,r} \), [17]. The harmonic currents manifest from the variations in the capacitor voltages [17], [28]. The DC component of the current is proportional to the power delivered, or the load current. For a three-phase lossless system, the input power, \( P_{in} \), and output power, \( P_{out} \), are related as follows:

\[ P_{in} = P_{out} \quad (2.5) \]
\[ V_{DC}I_{DC} = 3VI \cos(\phi) \quad (2.6) \]

where \( V_{DC} \) and \( I_{DC} \) are the average DC-link voltage and current, and \( V \) and \( I \) are the RMS phase voltage and current, respectively. The angle \( \phi \) denotes the relative phase angle between phase-voltage, \( v_r \), and phase-current, \( i_r \). If the circuit parameters of the three phase-legs are symmetrical and power flow between them is uniform, then the average value of the circulating current in a phase-leg is given by:

\[ \overline{i_{cir,r}} = \frac{I_{DC}}{3} = \frac{VI \cos(\phi)}{V_{DC}}. \quad (2.7) \]

The relationship between the circulating current, modulation scheme and capacitor voltages, \( v_{c,rn} \), can be represented as

\[ 2L \frac{di_{cir,r}}{dt} + 2Ri_{cir,r} = V_{DC} - \sum_{n=1}^{N} u_{rn}v_{c,rn} - \sum_{n=N+1}^{2N} u_{rn}v_{c,rn} \quad (2.8) \]

where \( \sum_{n=1}^{N} u_{rn}v_{c,rn} \) and \( \sum_{n=N+1}^{2N} u_{rn}v_{c,rn} \) are the voltages inserted by the modules in the top and bottom arms, respectively. In a three-phase converter, the circulating currents are in negative sequence with respect to the load current, with the dominant frequency of the circulating current being twice that of the load current [17], [31]. The circulating current, modulation scheme (switching function) and capacitor voltages are coupled to
2.4 Control

The primary objective of the control schemes that are employed for the M2LC is to control either the load current or the output voltage of the converter. This objective is fulfilled by regulating the number of modules that are connected in each arm. Since each arm comprises a large number of modules, the capacitor voltages of the modules need to be maintained close to their nominal values to ensure that the operation of the converter is stable. The importance of balancing capacitor voltages around their nominal values has been well recognised [32]–[35], and capacitor voltage balancing can be regarded as one of the secondary objectives of the control scheme. Additionally, the circulating currents need to be minimised for the reasons detailed previously, and circulating current control is another secondary objective of the control scheme.

2.4.1 Cascaded Control

Several control schemes, mostly cascaded, have been proposed to fulfil the aforementioned objectives [20], [35]–[37]. These schemes employ two control loops. The upper loop uses a current controller in conjunction with a modulator to control the load currents. The lower loop utilises the redundancy of the converter switching states to balance the capacitor voltages. In addition, the circulating currents are minimised by adding an appropriate component to the modulating signal of either each arm, or each module, of the M2LC. The block diagram of a typical cascaded control scheme is shown in Fig. 2.4.

![Figure 2.4: Block diagram of a cascaded control scheme for an M2LC.](image-url)
Chapter 2. Modular Multilevel Converters

2.4.1.1 Load Current Control

A number of state-of-the-art control schemes that have been developed for controlling the load/phase current of conventional VSCs can also be used for M2LCs [25]–[27]. The common approach with these schemes is to transform the load currents from the $abc$ frame into rotating $dq$ quantities, followed by comparison with their reference values, and use Proportional-Integral (PI) controllers for generating $dq$-frame voltage references. The $dq$ references are then transformed back to $abc$ frame for generating voltage reference, $M \cos(\omega t + \phi_r)$, for each phase [38]. The voltage reference is then used to control the voltage of each arm, thus driving the arm currents. The reference of each arm, $m_{rq}$, can be defined as

$$m_{rT} = \frac{1 - M \cos(\omega t + \phi_r)}{2} \quad (2.9a)$$

$$m_{rB} = \frac{1 + M \cos(\omega t + \phi_r)}{2} \quad (2.9b)$$

The voltage references are then compared with triangular carriers to generate the pulse pattern for the modules [20], [39]–[43]. The reference of each arm voltage is proportional to the number of modules that are connected in the arm. Since the voltage reference of the two arms has a phase shift of 180°, the total number of modules that are connected in a phase-leg remains equal to $N$. Therefore, if $N_1$ modules are connected in the top arm, then $N - N_1$ modules are connected in the bottom arm, and vice versa.

In [44], the energy stored in each arm is calculated by measuring the capacitor voltages and is used to generate the voltage reference for each arm. These reference signals are then compared against triangular carriers to determine the required arm voltage for controlling the load current. This scheme controls the energy that is stored in the converter and balances the energy of the top and bottom arms. Another variation of this control scheme is presented in [45], where the energy in each arm is estimated using the load current and the DC-link voltage. An optimal control scheme, the Linear Quadratic Regulator (LQR), has also been used to control an M2LC [46]. In another approach, arm current control is the primary objective of the scheme, with the load currents being controlled implicitly [47].

2.4.1.2 Capacitor Voltage Balancing

The DC value of the circulating currents, given in (2.7), determines the average value of the capacitor voltages. In a practical system, the power losses need to be compensated in order to maintain the capacitor voltages at their average values [48]. Typically, a sorting algorithm is used for balancing the capacitor voltages and the algorithm is implemented in the post modulation stage as shown in Fig. 2.4.
With the sorting algorithm, all of the capacitor voltage measurements are sorted in either ascending or descending order of their voltage magnitudes, and each capacitor is selected to be connected or bypassed [21], [41], [49]. For example, if two modules need to be connected in an arm, then the two capacitors with the lowest voltage are selected for a positive arm current and, conversely, the capacitors with the highest voltage are selected for a negative arm current.

The modulation signal or duty cycle for each module can also be modified for balancing the capacitor voltages [36]. Along with the balancing of the voltages, the capacitor voltage variations can be reduced by generating the appropriate harmonic circulating currents [33], [37], [50], [51]. In another approach, a half-bridge module is used to connect both arms of a phase-leg and to generate high frequency circulating currents to minimise voltage variations [52]. However, the inclusion of harmonic components increases the RMS arm currents and, therefore, the power losses of the converter.

### 2.4.1.3 Circulating Current Control

Various methods, both hardware and control based, have been proposed to minimise the circulating currents. The circulating currents, which are driven by a small voltage difference between the top and bottom arms of a phase-leg, can be reduced by increasing the size of the passive components, such as the arm inductance and/or resistance, or the capacitance of the power-modules [53]–[55]. Increasing the arm resistance, however, will reduce the efficiency of the converter. Increasing the capacitance, where the voltage rating of the capacitor is equal to the step size of the output voltage, could increase the monetary cost and footprint of the converter. Similarly, inductors, which are designed to operate in the low frequency range, are bulky and increase the footprint of the converter.

In [56], each phase-leg incorporates a filter that is tuned to block the second harmonic of the circulating current. In situations where the number of modules is increased without changing the number of voltage levels, the active redundancies of the modules have been used to reduce the capacitor voltage variations and circulating currents [57]. Circulating currents have also been minimised by employing cascaded control loops, with which the modulation function of each arm or module is modified [35], [48], [58]–[60]. With these control schemes, a compensation term, $M_{\text{cir},r}$, is added to the reference of the arm voltage (2.9), which modifies the reference of each arm as shown:

\begin{align}
    m_{rT} &= \frac{1 - M \cos(\omega t + \phi_r)}{2} + M_{\text{cir},r} \\
    m_{rB} &= \frac{1 + M \cos(\omega t + \phi_r)}{2} + M_{\text{cir},r}.
\end{align}

The currents can also be minimised by adding a common-mode voltage term to the
references of the arm voltages [44], [61]. Proportional-Resonant (PR) based controllers have also been used to minimise the circulating currents [35], [62]. The performance of the M2LC with the aforementioned schemes, in general, has been demonstrated to improve when the modules are switching at high frequencies. However, in high-power applications the switching frequency of the modules is always kept low to minimise power losses. A Selective Harmonic Elimination (SHE) based method that calculates the switching angles of the modules offline and reduces the switching frequency to the fundamental frequency of the load current while minimising the circulating currents is presented in [63].

2.4.2 Predictive Control

The M2LC, being a Multi-Input Multi-Output (MIMO) system, has in general been controlled with schemes that were designed for Single-Input Single-Output (SISO) systems. One such commonly used scheme is PI control in combination with carrier-based Pulse Width Modulation (PWM). Multiple PI loops, which are commonly used to control the M2LC, are difficult to tune, and if not properly designed could negatively affect the performance of the converter. Model Predictive Control (MPC) is suitable for controlling MIMO systems in a comprehensive manner [64]. With the MPC algorithm, a model of the converter is used to predict the response of output variables over several time-steps known as prediction horizon, \( N_p \). The control input that yields a desirable response is applied to the converter and the algorithm is repeated at the next sampling instant.

Historically, MPC was used in the petrochemical industries and power plants for several decades [65]. Since dynamics of such systems were slow, performance of the system was not affected by the long sampling intervals, which were needed to compute MPC algorithms. The development of fast processors, however, has reduced the computational time of MPC algorithms. Consequently, MPC has been used in several other applications such as automotive and aerospace industries, and recently in power electronics applications [66]–[68]. Some of the advantages of the MPC are simple design, ease of handling constraints, robustness, and ease of modelling non-linearities and time delays.

Because of the advantages of MPC over the traditional control schemes, it is becoming a popular approach for controlling M2LCs [69]–[72]. These MPC schemes use a single control loop to control the load currents, where the control objective is to minimise the error between reference, \( y_{ref}(k+1) \), and predicted currents, \( y(k+1) \). Variations in capacitor voltages, circulating currents and the load current error are all part of a cost function that is evaluated for all switch positions. The switch position, \( u(k) \), with the minimum cost is applied to the converter and a receding horizon policy is implemented by evaluating the cost function at each sampling instant. Fig. 2.5 shows the block diagram of MPC for an M2LC.
2.5 Modulation

In the context of multilevel converters, various modulation strategies have been proposed to generate gate signals for the converter, with each one having its own advantages and disadvantages [8], [73], [74]. Multicarrier modulation strategies such as Phase-Shifted (PS) and Level-Shifted (LS) modulation have commonly been adopted for the M2LC, and these strategies are discussed in the following sections.

2.5.1 Phase-Shifted Multicarrier Modulation

The Phase-Shifted (PS) modulation strategy is based on the comparison of a modulating reference signal with triangular carrier waveforms to generate a pulse pattern for the modules. For a converter with \( N + 1 \) voltage levels, \( N \) triangular carriers are required. With this approach, all of the carriers have the same amplitude and frequency, but adjacent carrier waveforms are phase shifted by \( 360^\circ / N \). The carrier arrangements using \( N = 4 \), and the output voltage of one of the modules are shown in Fig. 2.6.

Since an individual carrier waveform is associated with each module, the modules can be controlled independently, with the switching frequency of a module being equal to the frequency of the carrier waveform [23], [36]. Because of the PS carrier arrangement, the switching frequency appearing at the output terminal of the converter is \( N \) times the carrier frequency. Therefore, a higher switching frequency of the output voltage improves the THD of the load current [75].
Another variant of the PS modulation strategy is demonstrated in [36], [76], where the carrier waveforms of the bottom arm are phase shifted by 180° from those of the top arm. This variant results in an output waveform with $2N + 1$ voltage levels. With this approach, the number of modules connected in a phase-leg varies between $N$, $N - 1$ and $N + 1$. The increased number of voltage levels improves the harmonic performance of the load current, but results in increased variation in the circulating currents. Moreover, the complexity of the modulation strategy increases with the large number of modules, because each module requires a separate modulating signal [42], making implementation more difficult.

### 2.5.2 Level-Shifted Multicarrier Modulation

With Level-Shifted (LS) modulation, the pulse pattern for the modules is generated by comparing the modulating signal of the arm voltage with $N$ carrier waveforms with the same frequency and amplitude. The arrangement of carrier waveforms using $N = 4$ is shown in Fig. 2.7. This modulation strategy generates a reference for the number of modules to be connected in each arm. Therefore, there is flexibility in selecting the exact modules to connect [41], [77], [78]. In general, the modules are selected in accordance with the aforementioned sorting algorithm. Due to the sorting process, the switching frequency of the individual modules oscillates around its average value.

A modified modulation strategy that shifts the harmonics of the output voltage to twice the switching frequency has also been proposed [79]. Consequently, the switching frequency can be reduced without compromising the quality of the output voltage. Moreover, the LS modulation approach can also synthesise an output voltage waveform with $2N + 1$ levels by interleaving the carrier waveforms of the top and bottom arms [48]. The
circulating currents, however, have a significant amount of switching harmonics, requiring the arm inductance to be increased so as to reduce the effect of these harmonics on the arm current.

$$\theta = \omega t$$

$$V_{\text{nom}}$$

$0^\circ$ $90^\circ$ $180^\circ$ $270^\circ$ $360^\circ$

(a) Carrier arrangements

Figure 2.7: Level-shifted modulation strategy.

2.5.3 Space Vector Modulation

Space Vector Modulation (SVM), which offers several benefits over carrier based modulation, such as better utilisation of the DC-link voltage and improved harmonic characteristics, has also been adopted for M2LCs [21]. With this strategy, the switching states of the converter are represented by vectors. For a two-level three-phase converter, there

$$\beta$$

$$\omega$$

$$V_{\text{ref}}$$

Sector 2 $\mathbf{V}_2$

Sector 1 $\mathbf{V}_1$

Sector 3 $\mathbf{V}_3$

Sector 4 $\mathbf{V}_4$

Sector 5 $\mathbf{V}_5$

Sector 6 $\mathbf{V}_6$

Figure 2.8: Space vector diagram for a two-level converter.
are six active vectors $\vec{V}_1$ to $\vec{V}_6$ and a zero vector, $\vec{V}_0$. These vectors form a hexagon with six sectors as shown in Fig. 2.8. The reference voltage, $V_{\text{ref}}$, can be synthesised by the three vectors in the current sector. The SVM algorithm therefore determines the active sector that encloses $V_{\text{ref}}$, and calculates the on-time of the corresponding vectors during each sampling period. The complexity of SVM, however, increases with the number of levels, because a large number of calculations is required for finding and selecting the appropriate switching vector.

### 2.5.4 Reduced Switching Frequency Modulation

Because of the large number of modules, the carrier-based PWM and SVM strategies can be replaced with a staircase modulation strategy to reduce the switching frequency of the modules. Selective Harmonic Elimination (SHE) is one such strategy that reduces the switching frequency and eliminates certain low-order harmonics from the output voltage [2], [74]. With this strategy, the pulse-pattern or switching angles, as shown in Fig. 2.9, are calculated off-line by solving the appropriate equations, which are a function of the modulation index of the load current, and the harmonics of the output voltage waveform.

![Figure 2.9: Staircase modulation.](image)

A method of computing Optimised Pulse Patterns (OPP) for the minimisation of the THD of the output voltage is presented in [80], [81]. The number of equations increases with the number of voltage levels and, consequently, the process of finding an appropriate switching pattern becomes more complex as $N$ increases.

Nearest Level Control (NLC) is another strategy that reduces the switching frequency, and also has lower complexity than SHE. With this strategy, the voltage level that is closest to the reference waveform is determined and the switching combination yielding the voltage level is applied [82], [83]. Since switching harmonics are not specifically
targeted as a part of the scheme, this strategy cannot be used to eliminate the low-order harmonics of the voltage waveform. Nonetheless, NLC can be used for M2LCs with a large number of modules/levels, because the low frequency harmonics reduce with the increased levels.

With the NLC strategy, a small error exists between the selected level and its reference. To better approximate the nearest level, a combination of the NLC and PWM strategies has been proposed for the M2LC [40]. With this combination, PWM is used for a single module to minimise the error between the nearest level and the reference waveform.

2.6 Modelling

A model of the M2LC is required in order to analyse the behaviour of the converter. Moreover, the model can be regarded as a tool that facilitates both the proper controller design and physical design of the converter. The complexity of detailed models of the M2LC increases with the number of modules and, consequently, the computational time associated with the simulations also increases. A number of approaches have been described to simplify the model while adequately predicting the behaviour of the converter.

The Thevenin equivalent circuit of the converter, which reduces the number of state variables and thus computational time, is used to derive the mathematical model in [84], [85]. Another approach, as described in [86], reduces the computational burden and complexity of the model by representing each arm as a voltage source, as shown in Fig. 2.10. In another approach [87], each arm is modelled as a controlled voltage and current source, as shown in Fig. 2.11, in order to simplify the analysis of the converter.

![Figure 2.10: M2LC model using voltage sources.](image-url)
A state-space model, where the switching inputs are interpreted as continuous variables in the range of 0 to 1, is described to predict the behaviour of the converter in [88]. Because switching harmonics are ignored, the model is able to accurately describe the behaviour of lower order harmonics of the arm currents. In [89], a capacitor is used in each arm to model the combined behaviour of all the modules in the arm. Therefore, the model does not characterise the behaviour of individual modules, but predicts the average behaviour of the modules in each arm.

Simple models, which are easier and faster to simulate, are mainly used to predict the average behaviour of the converter. In contrast, detailed models, which are slower to simulate, can predict the behaviour with higher accuracy than the simple models. Detailed models can also investigate the effect of each module on the output quantities, such as the load and circulating currents. The choice of a suitable model for predicting the behaviour of the M2LC therefore depends on the objectives to be addressed.

2.7 Design

The process of designing an M2LC, which includes selecting the number of modules, the capacitance of the modules, and the arm inductance, can be started by considering the application of the M2LC. The control scheme for the M2LC can also be a part of the design process. The selection of the DC-link voltage or the output voltage of the converter, which depends on the application of the converter, forms the basis for the design of the M2LC. The voltage rating of both the module switches and the capacitors, which is an important aspect of the design, reduces in proportion to the number of modules. The THD of the output voltage also decreases by increasing the number of modules, but at the expense
of increased cost and component count. Each module can be configured as one of several arrangements depending on the application of the converter, as explained in Section 2.2.

The average voltage across the module capacitor depends on the number of modules in each arm. The voltage variations of the module capacitor, however, depend upon the capacitance. For a given capacitance, the corresponding voltage variations have been analysed in [33], [34], [50], [90], [91], and for a given operating condition, the capacitance which results in an acceptable level of voltage variation can be selected [92]. The footprint of the module is mainly governed by the capacitor. A relationship between the power transfer capability to the energy that is stored in the converter has also been developed, so as to optimise the capacitor size and the footprint of each module [93].

The purpose of arm inductors is to attenuate the switching harmonics of the arm currents and to reduce low-order harmonic currents, where the latter are referred to as circulating currents [94]. The design of a coupled inductor, which replaces the two inductors in a phase-leg, has been proposed to minimise the circulating currents [36]. In the case of the M2LC, the arm inductor and the module capacitors form a series resonant circuit, which can increase circulating currents if the proper circuit parameters are not selected. Therefore, the parameters that reduce the circulating currents or the effect of the resonance on the arm currents have been selected in [53]. In addition, the rate of change of the arm current during faults for a range of arm inductances has been investigated [55]. The rate of change of the current can be monitored and appropriate procedures can be initiated during fault conditions.

Once the parameters are selected, the complete system has to be simulated in order to optimise the performance of the converter. Software tools such as Matlab/Simulink can be used to build either detailed or simple dynamic models of the converter. Control schemes that meet desired performance specifications during steady-state and transient operating conditions can be compared and selected for controlling the M2LC [43], [44].

The design of a proper heat sink and the examination of the thermal behaviour of the switches are important for optimizing the efficiency of the converter [40], [95]. From an efficiency perspective, the choice of IGBT or Integrated Gate-Commutated Thyristor (IGCT) as a switch depends on the power rating of the converter, as investigated in [96]. Moreover, the acoustic noise that results from high frequency harmonics can also be considered during the design stage. Control schemes that reduce the switching frequency are appropriate for reducing the acoustic noise [26].
2.8 Applications

2.8.1 HVDC Transmission

Conventional transmission-scale converters have historically been based on the two-level VSC, with series connected semiconductor devices used to achieve the desired voltage ratings [97]. These conventional converters, however, are less efficient than the M2LC, because of their high switching frequency [18], [98], [99]. Along with high efficiency, the salient features of the M2LC topology, such as modular structure, low output voltage THD, and low switching frequency, have made the M2LC the preferred converter for HVDC transmission [16], [18], [43], [100]. Siemens has already implemented the M2LC technology for an HVDC transmission system, which is capable of delivering 400 MW over a distance of 88 km [101].

Several disadvantages of using a traditional High Voltage Alternating Current (HVAC) system for connecting offshore wind farms can be overcome with M2LC based HVDC systems [102], [103]. An offshore wind farm in Nanhui, China is using such a system to transfer 8 MW power over a distance of 8 km [104]. A multi-terminal HVDC grid which is based on M2LC technology is also proposed for connecting various energy sources [105], [106]. The multi-terminal grid improves the reliability of the complete power system by providing an additional means of power transmission along with the existing HVAC system.

2.8.2 Motor Drives

Substantial developments in the field of multilevel converter topologies have increased their use in various motor drive applications, such as industrial pumps, conveyors, fans and transportation [2]. The M2LC is also a part of these developments, and has been proposed for motor drives [19], [107]. However, the variation in the capacitor voltages of the M2LC increases when the motor operates at low speeds [20]. The common mode phase voltages can be used to reduce the voltage variations [51].

The viability of the M2LC over the full speed range of a motor has been demonstrated in [108]. A M2LC system has also been configured for AC/AC direct power conversion, and AC/DC/AC indirect power conversion, to interconnect the industrial grid at 50 Hz with the European rail grid at 16.7 Hz [22]. In another approach, a medium frequency transformer is used as an intermediate coupler between the rail power supply and the traction converters that are used for driving the motors [109]. Curtiss-Wright is using the M2LC technology for medium-voltage variable frequency drives [110].


2.8.3 Power Conditioners

The M2LC can be connected to the grid to improve power quality [23], [111], [112]. The star and delta configurations of the M2LC when used as a STATCOM are shown in Fig. 2.12 and Fig. 2.13, respectively. Because the star configuration does not have a path for circulating currents, it can only be used for controlling the positive-sequence reactive power [24]. In contrast, the delta configuration, which has a path for the circulating currents, can control both negative- and positive-sequence reactive power. Siemens has commercialised an M2LC based STATCOM system, and it has been implemented in a number of countries [113], [114].

The M2LC has also been used as an energy storage system to improve the reliability of a power distribution system [115]. A battery energy storage system has been integrated with the M2LC, allowing energy to be stored and released as required [24], [116].

2.9 Variants

A number of topological variations of the M2LC have also been proposed, to either improve the performance of the converter, or to extend the application range of the converter. The M2LC topology with half-bridge modules cannot block current during a DC fault. Therefore, a hybrid topology that integrates a switch in series with the full-bridge modules is used to block the fault current in [117]. The M2LC is configured as a multilevel matrix converter, as shown in Fig. 2.14, which allows for AC-AC direct power conversion in [118]–
In another variation, the arms of the converter are arranged to form a hexagonal M2LC, as shown Fig. 2.15, thus reducing the number of arms for AC-AC conversion [121].

2.10 Disadvantages of the M2LC

Even though the M2LC has several advantages over two-level and other multilevel VSCs, there are some disadvantages associated with the M2LC topology. The quality of the out-
put waveform can be improved by increasing the number of modules, but the complexity of the control scheme also increases. Since various voltage and current measurements are required to control the converter, the number of communication channels also increases with the number of modules. Moreover, sampling a large number of measurements can compromise the stability of the controller if processors with limited computing power are used. In addition, the voltage variations of the module capacitors are proportional to the phase current magnitude and inversely proportional to the frequency of the phase current. Hence, a large capacitor is required to limit the variations.

2.11 Summary

The M2LC, which features modularity, redundancy, easy scalability to any number of voltage levels and improved efficiency, has become popular in both medium- and high-voltage applications. Several control schemes, modulation strategies and modelling approaches have been proposed to improve both the performance and design of the converter. Since the M2LC employs floating capacitors to produce a number of output voltage levels, the control of the capacitor voltages is essential to ensure that the operation of the converter is stable. Moreover, both the academic and industrial communities have acknowledged the importance of controlling the circulating currents, which are generated by variations in the capacitor voltages. The control of the capacitor voltages and circulating currents is an ongoing area of research.

Although the M2LC has mostly been employed in HVDC and STATCOM applica-
tions, its usage in medium- to high-voltage drives is also increasing. The variation in the capacitor voltage, however, increases when running at low output frequencies. As such, improved control schemes and new variants of the M2LC topology will be the main area of research that will promote the widespread adoption of the M2LCs.
Chapter 3

Model Predictive Direct Current Control of Modular Multilevel Converters: Concept

3.1 Introduction

M2LCs have typically been controlled with hierarchical control schemes, which require at least two control loops: one to control the load currents, and another to control the circulating currents. With these schemes, multiple Proportional-Integral (PI) controllers are required to address the control objectives of the M2LC. In general, the tuning of multiple PI loops is difficult when appropriate performance of the converter is desired during both steady-state and transient operating conditions. Moreover, the tuning becomes even more challenging when certain constraints are imposed on the control objectives [122]. As detailed in Section 2.4.2, several Model Predictive Control (MPC) schemes have been proposed for controlling M2LCs, and these schemes promise to overcome the drawbacks of the typical control strategies. However, these MPC schemes have a short prediction horizon of one time-step. In general, however, a long prediction horizon is desired, as it improves the stability and performance of the converter [123].

The aim of this chapter is to present a Model Predictive Direct Current Control (MPDCC) scheme, which has a single control loop, for controlling M2LCs. The MPDCC scheme extrapolates the predicted trajectories of the load currents to yield long prediction horizons. The scheme also keeps the load currents within tight bounds around their sinusoidal references, and minimises both the capacitor voltage variations and circulating currents. A state-space model, which is generalised for N modules per arm of the M2LC, is also presented to investigate the dynamic behaviour of the arm currents and capacitor voltages. The model is used to predict and minimise the number of switching transitions...
for a given current ripple at steady-state, while providing a fast current response during transient conditions. In addition, a mathematical relationship between Total Harmonic Distortion (THD) and the bound width, \(2\delta\), as shown in Fig. 3.5, of the load currents is presented to demonstrate that the THD is a linear function of the bound width.

### 3.2 Model Predictive Control

For a typical MPC, the behaviour of the variables of concern is predicted over a number of time-steps, the length of which is referred to as the prediction horizon, \(N_p\). The controller determines the optimal control input based on the objectives and constraints of the converter. To visualise the concept of MPC, consider a system with three possible switch positions, \(u_1\), \(u_2\), and \(u_3\), shown in Fig. 3.1. The control objective is to find a suitable switch position that minimises the predicted error between the load current, \(i_o\), and its reference, \(i_{\text{ref}}\). In Fig. 3.1, the actual trajectory of the current is shown as a thick-solid line, whereas predicted trajectories are shown as thin solid lines, for all three switch positions. In this example, the trajectories are predicted for two steps, thus the length of the prediction horizon is two. Moreover, the switch positions are kept fixed over the length of \(N_p\). At time-step \(k + 2\), the error is predicted to be minimised with the switch position \(u_2\). Hence, the position \(u_2\) is the optimal input, and can be applied at time-step \(k\).

![Figure 3.1: Current predictions for various switch positions.](image)

If the \(N_p\) was one, the trajectories would be predicted for one time-step and, therefore, the switch position \(u_3\), with the minimum error at \(k + 1\) would be the optimal input. With
the application of $u_3$ at $k$, a new switch position might need to be applied at $k+1$ in order to minimise the error at $k + 2$. Therefore, the switch position that is applied depends on the length of the prediction horizon. In general, MPC with short horizons has the tendency to switch often while minimising the current error. In contrast, MPC with long horizons reduces the switching frequency of the converter, but also increases the current ripple and, therefore, THD of the current. In the case of M2LCs, the prediction horizon of the MPC schemes cannot be significantly increased unless proper control actions are taken to regulate the THD.

### 3.3 Model Predictive Direct Current Control

MPDCC, which has its roots in constrained optimal control, has previously been introduced for multilevel converters [66], [68], [124], [125]. With MPDCC, the load currents are kept within the allocated bounds, where the bound width, $2\delta$, regulates the THD of the current, as proven in the later sections of the chapter. The load current trajectories are predicted at time-step $k$, and the trajectories that can be kept within the bounds are extrapolated until they violate the bounds. The extrapolation yields horizons that are significantly longer than one sampling period. Other objectives of M2LCs, such as minimising the circulating currents and balancing the capacitor voltages are all part of the cost function that is evaluated over the length of $N_p$. The switch position with the minimum cost is applied to the converter. Moreover, the MPDCC controller sets the converter switch positions without a modulator, and therefore delays associated with the modulator are avoided, resulting in an improved transient response of the converter. The prediction model, constraints, cost optimisation and receding horizon policy are the key elements of the MPDCC scheme, and are discussed in the following sections.

#### 3.3.1 Prediction Model

MPDCC employs a discrete-time state-space model to predict the behaviour of the system. The accuracy of the predictions is governed by the accuracy of the model. In a practical system, the MPDCC algorithm is implemented on a digital signal processor, which sends the control inputs to the converter at discrete time instants. The model of the system can be written in the general form for a nonlinear time-invariant system as

$$ x(k + 1) = g(x(k), u(k)) \tag{3.1a} $$

$$ y(k) = h(x(k)) \tag{3.1b} $$
Chapter 3. MPDCC of M2LCs: Concept

and for a linear time-invariant system as

\[
\begin{align*}
  x(k+1) &= Ax(k) + Bu(k) \quad (3.2a) \\
  y(k) &=Cx(k) \quad (3.2b)
\end{align*}
\]

where \( k \in \mathbb{N}_0 \) is the discrete time-step, and \( x \in \mathbb{R}^n \), \( u \in \mathbb{R}^m \) and \( y \in \mathbb{R}^p \) are the state, input and output vectors, respectively. Moreover, \( A \in \mathbb{R}^{n \times n} \), \( B \in \mathbb{R}^{n \times m} \) and \( C \in \mathbb{R}^{p \times n} \) are the state, input and output matrices, respectively. Equations (3.1) and (3.2) are based on the assumption that the control inputs do not have a direct effect on the system output.

3.3.2 Constraints and Cost Optimisation

MPDCC allows the system to be driven closer its limits without violating them. The MPDCC algorithm finds the control inputs for which the constraints or limits are not violated. The constraints on system states, control inputs and system outputs can be defined in the following form

\[
\begin{align*}
  x(k) &\in \mathcal{X}(k) \subset \mathbb{R}^n \quad (3.3) \\
  u(k) &\in \mathcal{U}(k) \subset \mathbb{R}^m \quad (3.4) \\
  y(k) &\in \mathcal{Y}(k) \subset \mathbb{R}^p \quad (3.5)
\end{align*}
\]

where \( \mathcal{X}(k) \), \( \mathcal{U}(k) \) and \( \mathcal{Y}(k) \) are the sets of permitted states, inputs and outputs at time-step \( k \).

The problem to be solved is generally formulated as an optimisation problem with the aim being to find an appropriate sequence of control inputs, \( U \). The optimisation problem can be solved by evaluating a cost function, which is a measure of the chosen performance indicators, and can be expressed as

\[
J^*(k) = \min f(x(k), U(k))
\]

where \( J^*(k) \) is the minimum of the cost function \( f(x, U) \) that is based on the system states at time-step \( k \) and the sequence of control inputs. At each time-step, the cost function is subjected to the aforementioned constraints and evaluated to determine the optimal sequence of control inputs.
3.3.3 Receding Horizon Policy

At each sampling instant, the system states are measured and the behaviour of the system is predicted over the length of the prediction horizon. The control problem is solved to compute the present and future control inputs of the system, \( U(k) = [u(k), \ u(k + 1), \ u(k + 2), \ldots, \ u(k + N_p - 1)]^\top \), with the objective being to bring the system output closer to its reference. This concept is exemplified in Fig. 3.2(a). At time instant \( k \), only the first element of the sequence \( U(k) \) is applied to the system. At the next sampling instant \( k + 1 \), the control problem is solved again with the new set of measurements to determine a new optimal sequence of control inputs, as shown in Fig. 3.2(b). Only the first element of the sequence is applied at \( k + 1 \) and the process is repeated at the subsequent steps. This method of computing the control law is referred to as the receding horizon policy.

![Figure 3.2: Receding horizon policy.](image)
### 3.4 Modelling the M2LC

A typical M2LC, where the load is connected in the star-configuration, is shown in Fig. 3.3. Each phase-leg of the converter is divided into two halves, called arms. Each arm consists of \( N \) half-bridge modules, \( M_{rn}, r \in \{a, b, c\}, n \in \{1, 2, \ldots, 2N\} \), a resistor, \( R \), and an arm inductor, \( L \). The output terminals are connected to the load, which consists of an inductor, \( L_1 \), in series with a resistor, \( R_1 \), and a grid voltage, \( v_{g,r} \).

\[
\begin{align*}
V_{DC} & \quad \frac{V_{DC}}{2} & \quad \frac{V_{DC}}{2} \\
\text{A} & \quad M_{a1} & \quad M_{a2} & \quad \text{B} & \quad M_{bN} & \quad M_{b2N} \\
\text{C} & \quad M_{cN} & \quad M_{c2N} & \quad \text{D} & \quad M_{aN} & \quad M_{b(N+1)} \\
\text{E} & \quad R & \quad L & \quad R & \quad L & \quad R \\
\text{F} & \quad v_{a} & \quad v_{b} & \quad v_{c} & \quad v_{g,a} & \quad v_{g,b} & \quad v_{g,c} \\
\text{Load} & \quad \text{Grid} & \quad \text{Converter} & \quad \text{Power-Modules} & \quad \text{Input} & \quad \text{Output} \\
\end{align*}
\]

Figure 3.3: Modular multilevel converter.

The converter under consideration produces \( N + 1 \) output voltage levels, because \( N \) modules are always connected in a phase-leg. It is also possible to produce \( 2N + 1 \) voltage levels by varying the number of connected modules between \( N, N - 1 \) and \( N + 1 \) in accordance with the explanation given in Chapter 2. The increased number of voltage levels improves the harmonic performance of the load current at the expense of increased variation in the circulating currents. Although the MPDCC concept introduced in this chapter is based on the generation of \( N + 1 \) voltage levels, it can easily be extended to \( 2N + 1 \) voltage levels by modifying the constraints on switching states.

Since each power-module is configured as a half-bridge converter, the voltage, \( v_{rn} \), inserted by the module in an arm can be related to the capacitor voltage of the module, \( v_{c,rn} \), as

\[
v_{rn} = u_{rn}v_{c,rn} \tag{3.7}
\]
where \( u_{rn} \in \{0, 1\} \) is the switching state of the module. The switching states 0 and 1 correspond to a bypass and connection of a module capacitor, respectively.

The module capacitor, \( C \), charges or discharges depending on the switching state of the module and the arm current, \( i_{rq}, q \in \{T, B\} \). The capacitor voltage can be related to the switching state and arm current as

\[
C \frac{dv_{c,rn}}{dt} = \frac{v_{c,rn}}{R_{\text{cap}}} = i_{rT}u_{rn} \quad n \in \{1, N\}, r \in \{a, b, c\} \quad (3.8a)
\]

\[
C \frac{dv_{c,rn}}{dt} = \frac{v_{c,rn}}{R_{\text{cap}}} = i_{rB}u_{rn} \quad n \in \{N + 1, 2N\}, r \in \{a, b, c\} \quad (3.8b)
\]

where \( R_{\text{cap}} \) models the losses associated with the module. Although \( R_{\text{cap}} \) is not shown in Fig. 3.3, it is considered to be connected in parallel with the module capacitor, \( C \).

There are five independent currents associated with the star-configured load and these currents describe the state of the converter. The arm currents in phases \( a \) and \( b \), \( i_{aT}, i_{aB}, i_{bT}, i_{bB} \), and the DC-link current, \( i_{\text{DC}} \), are chosen to be the independent variables. The relationship between these currents, grid voltage and voltage inserted by the modules is given below, using Kirchhoff’s voltage law around the five circuit loops

Loop EABE

\[
L \frac{di_{aT}}{dt} + L \frac{di_{aB}}{dt} = -Ri_{aT} - Ri_{aB} - v_{a1} - v_{a2} \ldots - v_{a2N} + V_{\text{DC}} \quad (3.9a)
\]

Loop EACE

\[
L \frac{di_{bT}}{dt} + L \frac{di_{bB}}{dt} = -Ri_{bT} - Ri_{bB} - v_{b1} - v_{b2} \ldots - v_{b2N} + V_{\text{DC}} \quad (3.9b)
\]

Loop EADE

\[
-L \frac{di_{aT}}{dt} - L \frac{di_{aB}}{dt} - L \frac{di_{bT}}{dt} - L \frac{di_{bB}}{dt} + 2L \frac{di_{\text{DC}}}{dt} = Ri_{aT} + Ri_{aB} + Ri_{bT} + Ri_{bB} - 2Ri_{\text{DC}}
\]

\[
- v_{c1} - v_{c2} \ldots - v_{c2N} + V_{\text{DC}} \quad (3.9c)
\]

Loop EBFCE

\[
-L \frac{di_{aT}}{dt} + (L + L_i) \frac{di_{aB}}{dt} + L_i \frac{di_{bT}}{dt} - (L + L_i) \frac{di_{bB}}{dt} = Ri_{aT} - (R + R_i)i_{aB} - Ri_{bT} + v_{g,a}
\]

\[
- v_{a(N+1)} \ldots - v_{a2N} + v_{b(N+1)} \ldots + v_{b2N} + (R + R_i)i_{bB} - v_{g,b} \quad (3.9d)
\]
Loop EBFDE

\[
2L_i \frac{di_{aT}}{dt} - 2(L + L_i) \frac{di_{aB}}{dt} + L_i \frac{di_{bT}}{dt} - (L + L_i) \frac{di_{bB}}{dt} + L \frac{di_{DC}}{dt} = -2R_l i_{aT} + 2(R + R_l) i_{aB} \\
- R_l i_{bT} + (R + R_l) i_{bB} - R_l i_{DC} + v_{a(N+1)} \ldots + v_{a2N} - v_{g,a} + v_{g,c} - v_{c(N+1)} \ldots - v_{c2N} \tag{3.9e}
\]

where \( R_l \) and \( L_i \) are the load resistance and inductance, respectively.

The states of the arm currents and capacitor voltages are modelled using two linear state-space equations, termed as the first and second model, respectively. The state variables of the first model are the independent currents and the grid voltages in the \( \alpha \beta \) coordinate system. The state vector of the model is defined as

\[
x_i = [i_{aT} \ i_{aB} \ i_{bT} \ i_{bB} \ i_{DC} \ v_{g,\alpha} \ v_{g,\beta}]^T \tag{3.10}
\]

and the input vector is formed by the switching states of the modules

\[
u = [u_{a1} \ u_{a2} \ u_{a3} \ \ldots \ u_{c2N}]^T \in \{0, 1\}^{6N}. \tag{3.11}\]

The continuous-time state equation of the first model can be defined as

\[
T \frac{dx_i}{dt} = F_i x_i + G_i u + V_{DC}. \tag{3.12}
\]

The definitions of the system matrices \( T, F_i, G_i \) and \( V_{DC} \) are given in Appendix A.1. In the case of the first model, the capacitor voltages are treated as fixed parameters over the length of the prediction horizon. Such an assumption does not compromise the performance of the proposed scheme, because there is a very small change in the magnitude of the capacitor voltages over the length of prediction horizon, \( N_p \).

The state variables of the second model are the capacitor voltages, and its state vector is defined as

\[
x_c = [v_{c,a1} \ v_{c,a2} \ v_{c,a3} \ \ldots \ v_{c,c2N}]^T. \tag{3.13}\]

With the input vector defined in (3.11), the continuous-time state equation of the model is defined as

\[
\frac{dx_c}{dt} = F_c x_c + G_c u \tag{3.14}
\]

The system matrices \( F_c \) and \( G_c \) are presented in Appendix A.2. In the case of the second model, the arm currents are treated as parameters within the prediction horizon, because a small change in the arm currents, as given by the first model, has a negligible effect on the capacitor voltages.
The output equations for the load currents in phases $a$, $b$ and $c$ are as follows:

\[
\begin{align*}
    i_a &= i_{aT} - i_{aB} \\
    i_b &= i_{bT} - i_{bB} \\
    i_c &= -i_{aT} + i_{aB} - i_{bT} + i_{bB}.
\end{align*}
\]  

The circulating current in a phase-leg is given by

\[
i_{\text{cir},r} = \frac{i_{rT} + i_{rB}}{2}
\]

### 3.5 Internal Prediction Model

Since the MPDCC algorithm is implemented on a Digital Signal Controller (DSC), two discrete-time models of the converter are derived to predict the trajectories of the capacitor voltages and the arm currents. The first model predicts the arm currents and, as a result, the load- and circulating-currents. The output vector of this model is

\[
y_1 = [i_a \ i_b \ i_c \ i_{\text{cir},a} \ i_{\text{cir},b} \ i_{\text{cir},c}]^T.
\]

The second model predicts the behaviour of the capacitor voltages and, therefore, the voltages are the output vector of this model, $y_c = x_c$. Using the continuous-time state equations (3.10)–(3.16) and exact discretisation, presented in Appendix A.3, the following discrete-time models are derived.

\[
\begin{align*}
x_i(k+1) &= A_i x_i(k) + B_i u(k) + V_i \\
y_i(k+1) &= C_i x_i(k+1) \\
x_c(k+1) &= A_c x_c(k) + B_c u(k) \\
y_c(k+1) &= C_c x_c(k+1)
\end{align*}
\]

The definitions of the system matrices $A_i$, $B_i$, $V_i$, $C_i$, $A_c$, $B_c$ and $C_c$ are presented in Appendix A.3.

As described in Section 2.2.1, a voltage level can be produced by a number of module combinations. These combinations are enumerated in accordance with the Table 2.2 to form a look-up table of permitted combinations. Each row of the look-up table contains a possible switch position $u$ that is used by the discrete-time models of the converter.
3.6 Control Problem

The primary objective of MPDCC is to keep the load currents within symmetrical bounds around their sinusoidal references. The current reference determines the amount of power transferred to the load and can either be set directly by a user or by an external power controller. The load currents can be kept within the allocated bounds as long as the value of the violation function, \( \nu_r \), with an applied switch position, is zero over the length of prediction horizon, \( N_p \).

\[
\nu_r(k) = |i_r(k) - i_{\text{ref},r}(k) - \delta_u| + |i_r(k) - i_{\text{ref},r}(k) + \delta_l| - (\delta_l + \delta_u) \quad (3.22)
\]

where \( \delta_u = \delta_l = \delta \) is one half of the bound width that is set around the reference current, \( i_{\text{ref},r} \).

An inherent characteristic of the M2LC topology is that the voltage across the capacitors is a fraction of the DC-link voltage. The control scheme has to balance the capacitor voltages around their nominal value, \( V_{c,\text{nom}} \), or minimise the voltage variations, \( v_{c,\text{var}} \), derived as

\[
v_{c,\text{var}}(k) = \begin{bmatrix}
v_{c,a1}(k) - V_{c,\text{nom}} \\
v_{c,a2}(k) - V_{c,\text{nom}} \\
\vdots \\
v_{c,c2N}(k) - V_{c,\text{nom}}
\end{bmatrix}. \quad (3.23)
\]

As explained in Section 2.3, variations in the capacitor voltages generate circulating currents, which need to be minimised for the reasons mentioned in previous chapters. Therefore, MPDCC has to determine a switch position that minimises the circulating currents

\[
i_{\text{cir}}(k) = \begin{bmatrix}
i_{\text{cir},a}(k) \\
i_{\text{cir},b}(k) \\
i_{\text{cir},c}(k)
\end{bmatrix}. \quad (3.24)
\]

At the same time, the average switching frequency, \( f_{sw} \), which is an indirect measure of the switching losses, needs to be minimised as well.

\[
f_{sw} = \lim_{N_p \to \infty} \frac{1}{N_p T_s} \sum_{l=k}^{k+N_p-1} ||u(l) - u(l-1)||_1 \quad (3.25)
\]

where || \cdot ||_1 is the 1-norm and \( T_s \) is the sampling interval.

The key strength of a MPDCC is the ability to handle constraints for a multivariable system. The primary objective of the control problem, which is to keep the load currents within their bounds, can be extended by imposing constraints on the arm currents and...
3.7 Cost Function

The control problem, presented in Section 3.6, is solved by minimising the following cost function

\[ J_j = \frac{||u_j(k) - u(k-1)||_1}{N_j} + \lambda_1 ||i_{cir}(k + N_j)||_2^2 + \lambda_2 ||v_{c, var}(k + N_j)||_2^2, \quad j \in J \]  

(3.26)

where \( J \) is an index set, \( j \) is the index of a particular input, \( \lambda_1 \) and \( \lambda_2 \) are weighting coefficients and \( ||\cdot||_2 \) is the 2-norm. The first term in the cost function penalises the number of switching transitions and, therefore, minimises the average switching frequency. The first term is evaluated by dividing the number of switching transitions by the length of the extrapolated trajectory, \( N_j \). The other two terms, as described in Section 3.6, are used to minimise the circulating currents and the capacitor voltage variations. The function is only evaluated for the set of switch positions that keeps the load currents within the bounds. The algorithm to find such a set is described in Section 3.8.

At first glance, the cost function (3.26) seems to have redundant terms, because it has terms for both the voltage variations and circulating currents and these terms are related by (2.8). Even though the third term in (3.26) seems sufficient to minimise both the voltage variations and the circulating currents, its usage without the second term results in increased circulating currents. This is because of the redundant switching states of the converter, which can have a severe effect on the circulating currents. It is possible that a switching state might result in a minimum voltage variation while the same state results in an increased voltage difference and, as a result, increased circulating current in a phase-leg of the converter. Therefore, these states need to be used in such a manner that both the circulating currents and the voltage variations are minimised.

For example, consider a M2LC with four capacitors per phase-leg and capacitor volt-
ages that need to be balanced around half of the DC-link voltage of 400 V. The objective of the control scheme is to connect two capacitors that will reduce the voltage variations and the circulating currents. The capacitor voltages are predicted to be 202 V, 199 V, 205 V and 195 V in this hypothetical scenario. From the capacitor balancing perspective, the first two capacitors will be connected, because their selection is predicted to result in the minimum voltage variation around 200 V. On the other hand, the voltage difference in a phase-leg will be zero \((400 - 205 - 195 = 0)\) with the connection of the last two capacitors and their selection is thus more appropriate for minimising the circulating currents. Selection of sub-optimal states over time increases the voltage difference in a phase-leg, or the circulating currents. Therefore, both terms are needed in the cost function.

To achieve a strict control of the capacitor voltage variations, the cost function (3.26) can be augmented as

\[
J_j = \frac{||u_j(k) - u(k - 1)||}{N_j} + \lambda_1||i_{\text{cir}}(k + N_j)||^2 + \lambda_2||v_{\text{c, var}}(k + N_j)||_2^2 + \lambda_3||v_{\text{diff}}(k + N_j)||_2^2 \quad j \in J
\]

(3.27)

where,

\[
v_{\text{diff}}(k) = \begin{bmatrix}
v_{c,a1}(k) + v_{c,a2}(k) + \ldots v_{c,aN}(k) - v_{c,a(N+1)}(k) - v_{c,a(N+2)}(k) - \ldots v_{c,a2N}(k) \\
v_{c,b1}(k) + v_{c,b2}(k) + \ldots v_{c,bN}(k) - v_{c,b(N+1)}(k) - v_{c,b(N+2)}(k) - \ldots v_{c,b2N}(k) \\
v_{c,c1}(k) + v_{c,c2}(k) + \ldots v_{c,cN}(k) - v_{c,c(N+1)}(k) - v_{c,c(N+2)}(k) - \ldots v_{c,c2N}(k)
\end{bmatrix}
\]

The first, second and third terms in the cost function are the same as presented in (3.26). The fourth term minimises the difference in the average value of the capacitor voltages in the top and the bottom arm.

The cost function (3.26) is easier to implement and has fewer penalties. However, the voltage variations can be slightly higher than with (3.27). On the contrary, the cost function (3.27) has more penalties and, therefore, the tuning of the weighting coefficients could become more difficult. The cost function can thus be selected according to the specified performance objectives.

Control of the DC-link current, if required, can also be incorporated into the MPDCC scheme. The DC-link current can be a part of the cost function, where the term evaluating the current error (DC-link current minus its reference) will be minimised. The error will be evaluated at each sampling instant and weighting coefficients define its importance/cost in relation to the other quantities listed in the cost function.
3.8 Control Algorithm

The Switch and Extrapolate (SE) switching scheme is adopted, as described in [124], [126], to predict the states of M2LC. This scheme employs a single control loop to control the load- and circulating-currents, and to balance the capacitor voltages. In addition, minimisation of the switching frequency is a part of the same loop. The block diagram of the scheme is presented in Fig. 3.4.

![Model Predictive Direct Current Control Scheme](image)

Figure 3.4: Model predictive direct current control scheme.

The operating principle of the SE scheme is explained below:

1. Given the previously applied switch position \( u(k-1) \) and the present states, the arm currents and, as a result, the load currents are predicted at time-step \( k+1 \), using (3.18) and (3.19) for all possible switch positions. This implements the first part, S, of the SE scheme. For example, the predicted trajectories of the load currents, in phases a and b, for three switch positions are shown in Fig. 3.5. Here, \( \delta \) is one half of the allowed ripple around the reference currents.

2. The main objective of MPDCC, as mentioned in Section 3.6, is to keep the load currents within their bounds or to keep the value of the violation function (3.22) at zero. This is achieved by imposing a constraint on the switch positions, and this constrained set of positions is called the candidate switch positions. In other words,
the candidate positions are those switch positions which keep the load current trajectories within the bounds. During steady-state operating conditions, the value of the violation function (3.22) can easily be kept at zero by applying the candidate switch positions. However, during transient operating conditions, such as a sudden change of reference currents, the current trajectories may violate the bounds, because of the limited response time of the physical system. Therefore, the positions for which the absolute violation value, $\nu_r$, decreases with time are also included in the candidate positions.

In the next step, the candidate switch positions with indices $j$, where $j \in J$ and $J$ is an index set, are determined. Moreover, the switch positions for which a load current violates bounds at $k + 1$ are rejected. For example, consider Fig. 3.5, in which the switch position 1 is not a candidate position because the load current is predicted to violate the upper bound, for both phases $a$ and $b$, at time-step $k + 1$. On the other hand, the load current at $k + 1$ is predicted to be within the bounds when selecting the third switch position, making it a candidate position. For the second position, the current at $k + 1$ will remain outside of its bound for phase $a$, but its violation decreases from $k$ to $k + 1$, making it also a candidate position.

![Figure 3.5](image-url)

Figure 3.5: Trajectories of the load currents. Actual, predicted and extrapolated trajectories are shown as thick-solid, solid and dashed lines, respectively.

3. The candidate trajectories are then linearly extrapolated from time-step $k + 1$ onwards until they violate the predefined band [127]. This implements the second part, $E$, of the SE scheme. This extrapolated length, $N_j$, is represented in multiples of the sampling interval, $T_s$. For position 2 at time-step $k$, the load current trajectories can be kept within the bounds for a length of $N_2 = \min(N_{a2}, N_{b2}, N_{c2})$, before requiring a new switching transition at time-step $k + N_2$. 
4. At the next stage, the capacitor voltages are predicted, using (3.20) and (3.21), for all the predetermined candidate positions (step 2). These voltages are then linearly extrapolated for the number of time-steps determined in step 3. The capacitor voltages at time-step $k + N_j$, $j \in J$ are denoted as terminal capacitor voltages, $v_{c,rn}(k + N_j)$. Similarly, the trajectories of the circulating currents are predicted and extrapolated, using (3.19), for all the candidate positions.

5. The candidate positions satisfy the constraints imposed on the load currents and the remaining objectives of the M2LC, as stated in Section 3.6, and the cost function (3.26) is evaluated for the candidate positions.

6. The candidate switch position with the minimum cost is determined and applied at time-step $k$.

A receding horizon policy is implemented by repeating these above steps at the next sampling instant. The prediction horizon can be further extended by using more complicated switching schemes, such as SSE or SESE. Increasing the prediction horizon improves the performance of the system, as detailed in [68], [124], [128], and such an improvement in performance could also be expected with the M2LC.

### 3.9 Bounds of the Load Current

With MPDCC, symmetrical bounds are imposed around the load currents to keep the currents within the bounds. The bound width sets the trade-off between the level of current THD and the length of prediction horizon and, consequently, the average switching frequency. As explained in the following sections, a smaller bound width reduces the THD of the current at the expense of increased switching frequency.

#### 3.9.1 Total Harmonic Distortion

The load current is distorted due to the steps in the output voltage. Along with the fundamental frequency component, the current contains harmonics of the switching frequency at integer multiples of the fundamental frequency [74], [129]. These harmonic components are used to measure the THD and can be calculated by using Fourier series. The load current waveform $i_{r}(t)$ can be expressed in terms of Fourier coefficients as

$$
    i_{r}(t) = \frac{a_0}{2} + \sum_{h=1}^{\infty} A_h \cos \left( \frac{2\pi h t}{T} \right) + \sum_{h=1}^{\infty} B_h \sin \left( \frac{2\pi h t}{T} \right) \quad (3.28)
$$
where $T$ is the interval over which $i_r(t)$ is periodic. The coefficients $a_0$, $A_h$ and $B_h$ can be evaluated as

$$a_0 = \frac{2}{T} \int_0^T i_r(t)dt \quad (3.29)$$

$$A_h = \frac{2}{T} \int_0^T i_r(t)\cos\left(\frac{2\pi ht}{T}\right)dt \quad (3.30)$$

$$B_h = \frac{2}{T} \int_0^T i_r(t)\sin\left(\frac{2\pi ht}{T}\right)dt \quad (3.31)$$

The value of $a_0$ is zero, because the load current controller ensures that there is no DC component in $i_r(t)$. Therefore, the load current can be expressed as the sum of fundamental and harmonic current components as

$$i_r(t) = i_{r1}(t) + \sum_{h=2}^{\infty} i_{rh}(t) \quad (3.32)$$

where $i_{r1}(t)$ is the fundamental component and $i_{rh}(t)$ is the component at the $h^{th}$ harmonic frequency. The load current ripple, $i_{\text{rip, r}}$, can be determined by subtracting the fundamental component from the load current. To visualise this, the waveform of the current ripple is shown in Fig. 3.6, where $2\delta$ is the width of the current bounds and $T_r$ is the time period of the repetitive ripple waveform. In a real system, however, the time period of the two adjacent ripples will be different, because the slope of the load current changes over the fundamental period of the current. Nonetheless, the effect of such differences can be ignored for smaller bound widths, because the magnitude of the harmonic currents decreases with the bound width.

![Figure 3.6: Load current ripple.](image-url)
The Fourier coefficients of $i_{rip,r}$ are calculated using (3.29) – (3.31) to be

\[ a_0 = 0 \]  \hspace{1cm} (3.33) \\
\[ A_{rip,h} = \frac{\delta T_r^2 \left( \cos \left( \frac{2\pi h T_1}{T_r} \right) - 1 \right)}{\pi^2 h^2 T_1 (T_r - T_1)} \]  \hspace{1cm} (3.34) \\
\[ B_{rip,h} = \frac{\delta T_r^2 \sin \left( \frac{2\pi h T_1}{T_r} \right)}{\pi^2 h^2 T_1 (T_r - T_1)} \]  \hspace{1cm} (3.35)

The RMS magnitude of the each harmonic component of $i_{rip,r}$ is

\[ AB_{rip,h} = \sqrt{A_{rip,h}^2 + B_{rip,h}^2} \]  \hspace{1cm} (3.36)

This magnitude can be expressed in terms of the bound width using (3.34) – (3.35) as

\[ AB_{rip,h} = \frac{\delta T_r^2}{\sqrt{2} \pi^2 h^2 T_1(T_r - T_1)} \left[ \cos \left( \frac{2\pi h T_1}{T_r} \right) - 1 \right]^2 + \left[ \sin \left( \frac{2\pi h T_1}{T_r} \right) \right]^2 \]  \hspace{1cm} (3.37)

Although (3.37) is calculated over the time period $T_r$, its value remains the same over the entire fundamental period of the load current and, therefore, does not have any impact on the THD calculations. The THD of the load current is given by

\[ \text{THD}_i = \sqrt{\sum_{h=1}^{\infty} \frac{AB_{rip,h}^2}{I_{r1}^2}} \]  \hspace{1cm} (3.38)

where $I_{r1}$ is the RMS value of the fundamental component of the load current. Unlike the standard definition of THD, the lower limit of the summation in (3.38) is one, because the Fourier coefficients (3.33) – (3.35) are based on the ripple current instead of the load current waveform.

The THD can be expressed in terms of bound width, by using (3.37), as

\[ \text{THD}_i = \frac{\delta T_r^2}{\sqrt{2} I_{r1} \pi^2 T_1 (T_r - T_1)} \sqrt{\sum_{h=1}^{\infty} \frac{\left( \cos \left( \frac{2\pi h T_1}{T_r} \right) - 1 \right)^2 + \left( \sin \left( \frac{2\pi h T_1}{T_r} \right) \right)^2}{h^4}} \]  \hspace{1cm} (3.39)

It is evident from (3.39) that the THD of the load current is a linear function of the bound width. Therefore, the value of $\delta$ sets the level of THD of the currents. Although the level of THD can be affected by under-utilisation of the bounds, the MPDCC algorithm
usually selects an optimal switch position with which the bounds are well utilised.

### 3.9.2 Length of the Prediction Horizon

At each sampling instant, the MPDCC algorithm determines the switch position with the minimum cost over the length of the prediction horizon. The length of the prediction horizon is not fixed, as the extrapolation part of the MPDCC yields a dynamic horizon that is often significantly longer than one time-step. The length of the prediction horizon depends on the bound width, the sampling frequency and the time constant of the load inductor.

The slope of the load current changes over the fundamental period and has an important role in the calculations of the prediction horizon. The change in slope can be evaluated from the voltage across the load inductor, and can be found from

$$L_1 \frac{di_r(t)}{dt} = v_r(t) - v_{g,r}(t) - R_l i_r(t)$$  \hspace{1cm} (3.40)

where $v_r(t)$ is the output voltage of the converter, and $R_l$ and $L_1$ are the load resistance and inductance, respectively.

The slope of the load current can be derived by applying forward-Euler discretisation as

$$\frac{i_r(k+1) - i_r(k)}{T_s} = \frac{v_r(k) - v_{g,r}(k) - R_l i_r(k)}{L_1}$$  \hspace{1cm} (3.41)

where $T_s$ is the sampling interval. At time instant $k$, the length of the prediction horizon is evaluated by using the ripple current, $i_{rip,r}(k) = i_r(k) - i_{ref}(k)$, and slope of the load current via

$$N_{p,r}(k) = \frac{\delta - i_{rip,r}(k)}{i_{rip,r}(k+1) - i_{rip,r}(k)}, \quad \text{when} \ (3.41) \geq 0 \hspace{1cm} (3.42a)$$

$$N_{p,r}(k) = \frac{-\delta - i_{rip,r}(k)}{i_{rip,r}(k+1) - i_{rip,r}(k)}, \quad \text{otherwise} \hspace{1cm} (3.42b)$$

For a given ripple current, $i_{rip,r}(k)$, and predicted ripple current, $i_{rip,r}(k+1)$, the average length of the prediction horizon given in (3.42) is proportional to the bound width. Because the value of the current ripple changes over the fundamental period, the length of the prediction horizon is dynamic.

The MPDCC algorithm applies a new switch position once the trajectories are close to the bound width. Therefore, a larger bound width increases the time for which the chosen position can be applied and, consequently, reduces the switching frequency of the converter.
3.10 Summary

In this chapter, an MPDCC scheme, with long prediction horizons, has been proposed for M2LCs. The proposed MPDCC employs a single control loop to maintain the load current within prescribed bounds around sinusoidal references, and minimises the capacitor voltage variations and circulating currents. With the MPDCC scheme, the extrapolation of the predicted trajectories yields prediction horizons that can be significantly longer than one time-step. The trajectories of the load currents are predicted for all the switch positions and the positions for which the currents can be kept within the allocated bounds are regarded as possible candidate positions. The cost function, which is a measure of the voltage variations, circulating current and switching frequency, is evaluated for all the possible positions and the position with the minimum cost is applied to the converter. The formulation of an appropriate cost function has also been presented in this chapter.

A state-space model, which is generalised for $N$ modules per arm of the M2LC, has been derived to investigate the dynamic behaviour of the arm currents and capacitor voltages. In addition, a mathematical function of the load current THD has been derived to reveal that the THD is a linear function of the current bound width. The THD can be reduced by decreasing the bound width at the expense of a reduced prediction horizon and, as a result, increased switching frequency.
Chapter 4

Model Predictive Direct Current Control of Modular Multilevel Converters: Performance Analysis

4.1 Introduction

This chapter evaluates the performance of the MPDCC scheme that was proposed in Chapter 3 for M2LCs. The performance of the MPDCC scheme is benchmarked against the Voltage-Oriented Control (VOC) scheme that is extensively used for controlling grid-connected multilevel converters, through simulations of a three-phase M2LC. These two schemes are compared for a fixed average switching frequency. Under steady-state conditions, the key performance indicators are the THD of the load current, the magnitude of the circulating currents and the voltage variations of the capacitors.

The practical feasibility of the scheme is validated using experimental results for a single-phase three-level 860-VA M2LC prototype. In general, the MPDCC algorithm is computationally expensive and, therefore, in order to reduce the computational burden of the MPDCC algorithm, most of the calculations are computed offline. In addition, a simple yet effective approach is discussed to further reduce the computational time. The simulated performance of the converter, under various operating conditions, is presented in comparison to the measured performance to demonstrate the successful implementation of the proposed MPDCC scheme.

4.2 Simulation Results

The performance of the MPDCC scheme was investigated using PLECS/SIMULINK simulations for a 2-MVA three-level M2LC. The simulations were used to establish the ideal
response of the control scheme ignoring the non-ideal behaviour such as sampling delays. All simulations were performed assuming that the DC supply is free of oscillations. The circuit parameters used for the simulations are summarised in Table 4.1. The cost function weighting coefficients $\lambda_1 = 1.11 \times 10^{-5}$ and $\lambda_2 = 1.67 \times 10^{-4}$ were used for MPDCC in the simulations, and heuristic approach was followed to select their values. These coefficients were tuned such that an appropriate performance of the M2LC was achieved during steady-state and transient operations.

Table 4.1: System parameters of a three-phase M2LC.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output frequency</td>
<td>$f_o$</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>$V_{DC}$</td>
</tr>
<tr>
<td>Grid RMS voltage</td>
<td>$V_{\text{ll}}$</td>
</tr>
<tr>
<td>Load RMS current</td>
<td>$I_r$</td>
</tr>
<tr>
<td>Capacitance current</td>
<td>$C_{rn}$</td>
</tr>
<tr>
<td>Load resistance</td>
<td>$R_l$</td>
</tr>
<tr>
<td>Load inductance</td>
<td>$L_1$</td>
</tr>
<tr>
<td>Arm inductance</td>
<td>$L$</td>
</tr>
<tr>
<td>VA rating</td>
<td>2 MVA</td>
</tr>
</tbody>
</table>

VOC was used to benchmark the performance of the MPDCC scheme. With the VOC scheme, the load currents in the $abc$ frame were transformed into $dq$ quantities, followed by comparison with their reference values and, finally, Proportional-Integral (PI) controllers were employed to generate $dq$-frame voltage references. The $dq$ voltage references were then transformed to the $abc$ domain and compared against carrier waveforms in Phase Disposition (PD) to generate the gating signals for the modules. The PI gains were tuned such that rise time of the load current with the VOC scheme is similar to that with the MPDCC scheme. The inputs to the PI controller were the normalised three-phase load currents. The output of the PI controller was limited to $\pm 1.155$ and the integrator was stopped when the output exceeds the set limits, thereby implementing an anti-windup scheme. Moreover, a third harmonic was injected in the reference signals using a min-max approach, which achieves the same switching sequences as space vector modulation [130]. The frequency of the carrier waveform was 750 Hz. The capacitor voltages were balanced by using the sorting algorithm as presented in Chapter 2, and the algorithm was based on the polarity of the arm currents.
4.2 Simulation Results

4.2.1 Steady-State Performance

The waveforms of the load current with the MPDCC and VOC schemes, shown in Fig. 4.1, are similar in trend and value. In the case of MPDCC, the currents have been maintained within the bounds, where the bound width, $\delta$, of the load currents was tuned to 25 A. The THD of the load current was 3.39% and 4.11% with the MPDCC and VOC schemes, respectively. THD was calculated by using PLECS software, which has a block to compare the amplitude of the current harmonics to the fundamental current level.

![Figure 4.1: Simulated load current waveforms for one fundamental period.](image)

Fig. 4.2 shows the harmonic spectrum of the load current for both schemes. Because the VOC scheme employs a modulator, the spectral components of the current are limited to non-triplen odd integer multiples of the fundamental frequency. In contrast, the spectrum for the MPDCC scheme is spread over the frequency range because of the variable switching frequency.

![Figure 4.2: Harmonic spectrum of the load current.](image)

The waveforms of the arm currents in phase-$a$, which are shown in Fig. 4.3, are similar in shape with both the schemes. In order to enhance the clarity of the figures, the
waveforms of the currents in other two phase-legs, which are phase shifted with respect to phase-leg $a$, are omitted. Both schemes result in the same RMS arm current of 229 A. Therefore, the magnitude of the circulating currents, which is defined in (3.16), is also same with both the schemes.

![Figure 4.3: Simulated waveforms of the arm currents in phase-leg $a$ for one period.](image)

The output voltage produced in the middle of any phase-leg of the converter, $v_r$, was measured with respect to the mid-point of the DC-link, which was used as a reference voltage. In a physical system, the mid-point might not be accessible, but was used in simulations to demonstrate that the converter produces $N + 1 = 3$ voltage levels, as shown in Fig. 4.4. The pulse pattern of the output voltage waveforms is uniformly

![Figure 4.4: Simulated output voltage waveforms.](image)
distributed over the fundamental period of the load current. In the case of VOC, which used carriers in PD, the switching frequency was expected to be $750/N = 750/2 = 375$ Hz. However, the sorting algorithm increased the number of switching transitions and, hence, the frequency was 400 Hz. The frequency was calculated by averaging the number of switching transitions over a time period of 200 ms. The MPDCC results in the similar average switching frequency of 396 Hz, but with the lower current distortion.

The capacitor voltages were balanced within 6% of their average value and Fig. 4.5 shows the capacitor voltage waveforms over one fundamental time period. The voltages with both schemes are well balanced.

![Figure 4.5: Simulated capacitor voltage waveforms.](image)

### 4.2.2 Performance during Transients

In order to evaluate the transient performance, the converter was operated at rated load current before the reference of the load currents was changed to zero at time-instant $t = 50$ ms, with this event termed the power-down transient in the forthcoming discussion. At time-instant $t = 250$ ms, the load current reference was changed back to the rated current, with this event termed the power-up transient. The bound width, $\delta = 25$ A, was not changed during the transient operation.

As shown in Fig. 4.6 and Fig. 4.7, MPDCC achieves a very fast current response both at power-down and power-up. The waveforms of the current for one period are shown in Fig. 4.8 and Fig. 4.9. MPDCC takes less than 3 ms to deliver the rated load currents at both power-up and power-down. On the other hand, the VOC scheme provides a slow response and takes approximately two fundamental time periods to track its new reference. With the VOC scheme, the load currents overshoot at power-up before settling at their nominal values, shown in Fig. 4.7. The current response might not be further improved, because increasing PI gains beyond certain values will result in unstable oscillations in the load currents. Because the PI controller works on the basis of the present error and
the integral of previous errors, its response time to track the reference current is slower than the MPDCC, which works on the basis of minimising an error in the future.

![Figure 4.6: Simulated load current waveforms during the power-down transient.](image1)

![Figure 4.7: Simulated load current waveforms during the power-up transient.](image2)

![Figure 4.8: Simulated load current waveforms during the power-down transient for one period.](image3)
4.3 Experimental Results

With the MPDCC scheme, the capacitor voltages, shown in Fig. 4.10 and Fig. 4.11, are well balanced both at power-down and power-up. After power-up, the capacitor voltages settle within 6% of the average voltage value in less than three periods. The response time of the MPDCC is faster while balancing the capacitor voltages. With the VOC, the peak of the voltage is slightly higher than the MPDCC scheme. This peak value can be minimised by controlling the rate of change of the load current, but at the expense of an increased time to track the current references.

4.3.1 M2LC Setup

In order to verify the viability of the proposed MPDCC scheme, a single-phase three-level 860-VA prototype M2LC was constructed. The experimental setup is shown in Fig. 4.12.
The parameters of the system, which are used to verify the performance of the MPDCC scheme through simulations on PLECS/Simulink and experiments, are summarised in Table 4.2. The simulated results are used to benchmark the experimental performance of the MPDCC scheme. The MPDCC algorithm, shown as a flow chart in Fig. 4.13, was implemented on a TMS320F28335 Digital Signal Controller (DSC). The DSC has an on-board Analog to Digital Converter (ADC), which was used to measure all the arm, load and DC-link currents and the DC-link and capacitor voltages. Altera’s DE2 FPGA board was used to generate dead-time for the switching signals of modules and to safely shut down the converter in the unlikely event of a fault. At start-up, a resistor was connected in series with the DC-supply to charge the capacitors and it was bypassed during normal operation of the converter. The weighting coefficients $\lambda_1 = 0.09$ and $\lambda_2 = 0.36$ were used within the cost function (3.26) in the experiments and simulations. The simulations were carried out to tune the weighting coefficients such that an appropriate performance of the M2LC is achieved during steady-state and transient operations.

Table 4.2: System parameters of a single-phase M2LC.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output frequency $f$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Supply voltage $V_{DC}$</td>
<td>400 V</td>
</tr>
<tr>
<td>Load RMS current $I_l$</td>
<td>4.5 A</td>
</tr>
<tr>
<td>Capacitance $C$</td>
<td>1.72 mF</td>
</tr>
<tr>
<td>Load resistance $R_l$</td>
<td>42 Ω</td>
</tr>
<tr>
<td>Load inductance $L_1$</td>
<td>30 mH</td>
</tr>
<tr>
<td>Arm inductance $L$</td>
<td>1.2 mH</td>
</tr>
</tbody>
</table>
4.3 Experimental Results

4.3.2 Optimised DSC Code

The MPDCC algorithm is computationally demanding, because the trajectories of the arm and load currents, and capacitor voltages need to be predicted and extrapolated for the maximum number of switch positions, i.e. 36 positions in the single-phase setup. In order to solve this problem in a reasonable amount of time, most of the multiplications and divisions were computed offline. This reduces the calculations of the predicted trajectories
to simple logical additions, based on the switching states of the modules, of pre-computed values multiplied by the measured state variables.

For example, consider the equation of the predicted load current

\[
i_l(k + 1) = g(k) - k_1 u_{a1} v_{c,a1}(k) - k_1 u_{a2} v_{c,a2}(k) + k_2 u_{a3} v_{c,a3}(k) + k_2 u_{a4} v_{c,a4}(k)
+ k_3 u_{b1} v_{c,b1}(k) + k_3 u_{b2} v_{c,b2}(k) - k_4 u_{b3} v_{c,b3}(k) - k_4 u_{b4} v_{c,b4}(k)
\]

(4.1)

where,

\[
g(k) = k_5 V_{DC} + k_6 i_{aT}(k) + k_7 i_{AB}(k) + k_8 i_l(k)
\]

(4.2)

Constants k_1 to k_8 depend on the system parameters and were computed offline. Equation (4.1) needs to be evaluated, using for-loops, for all the switch positions. However, \(g(k)\) does not depend on the switch positions and was computed once every sampling interval. The computational time associated with the calculation of (4.1) was minimised by replacing multiplicative instructions with a logical addition, which was based on the permitted switch positions. Two such instructions of the logical addition, which were
used for predicting the load current, $i_{l,p}(k+1), p \in \{1,2,\ldots,36\}$, are presented below:

$$
\begin{align*}
  i_{l,1}(k+1) &= \left[g(k)\right] - \left[k_1 v_{c,a1}(k)\right] - \left[k_1 v_{c,a2}(k)\right] + \left[k_2 v_{c,b1}(k)\right] + \left[k_2 v_{c,b2}(k)\right] \\
  i_{l,2}(k+1) &= \left[g(k)\right] - \left[k_1 v_{c,a1}(k)\right] - \left[k_1 v_{c,a2}(k)\right] + \left[k_2 v_{c,b1}(k)\right] - \left[k_3 v_{c,b3}(k)\right]
\end{align*}
$$

The terms within the square brackets were evaluated once per sampling interval and used throughout the implemented code. The remaining variables, such as the arm currents and capacitor voltages, were also predicted using the same method. This procedure reduced the maximum computational time from 172 $\mu$s to 124 $\mu$s. As the division operation is computationally expensive, its usage was limited to two: for evaluating the prediction horizon and imposing the penalty on the number of switching transitions in the cost function. Since the maximum execution time of the MPDCC scheme is 124 $\mu$s, a sampling frequency of 8 kHz was chosen.

### 4.3.3 Delay Compensation

The MPDCC algorithm presented in Section 3.8 is based on the assumption that the execution time of the algorithm is negligible, i.e. the measurement of the state variables and the application of the new switch position occur at the same time-step $k$. In a practical system, however, the new switch position will only be applied once the execution of the algorithm is completed, and at that instant the system states have already evolved in time. This mismatch between the times of the state measurements and switch application degrades the performance of the converter, which for MPDCC would be observed as a violation of the current constraints.

With the implemented algorithm, this delay is fixed to one sampling interval as it simplifies the forthcoming method of delay compensation. The delay was compensated by predicting the current trajectories and finding the candidate positions at $k+2$ instead of $k+1$ [131]. Fig. 4.14 provides a visual example of the delay compensation method. With this method, the previous switch position that was determined at $k-1$ is applied at time instant $k$. The system states are predicted at $k+1$, using the measured states at $k$ and the applied switch position. The MPDCC algorithm is executed from time-step $k+1$, where the trajectories of the load current are explored at time instants $k+2$ and onwards. The suitable switch position is determined at time instant $k$ to be applied at $k+1$, thus compensating the delay.
4.3.4 Steady-State Performance

At each sampling instant a new switch position was determined over the length of the prediction horizon, where the latter depends upon the bound width, sampling frequency and time constant of the load inductor, as explained in Section 3.9.2. For the given system parameters and $\delta$ of 0.64 A, the length of the prediction horizon with both the experiments and the simulations was in the range of 1 to 8 time-steps. The trajectories of the load- and circulating-currents and capacitor voltages were extrapolated for the same length.

Fig. 4.15 shows both the simulated and experimental waveforms of the load current, $i_l$, to demonstrate that the load currents are kept inside the bounds. The waveforms of the output voltage, $v_{ab}$, are shown in Fig. 4.16. The simulated and experimental waveforms are similar and confirm the validity of the implemented scheme. All switching transitions appear to take place near the edge of the specified bounds and, at that instant, a new switch position that is predicted to minimise the voltage variations and circulating currents was selected. There are a few instances where the load current trajectory does not
4.3 Experimental Results

utilise the full bound width. This is because of two reasons: the choice of the weighting coefficients in (3.26) and increased voltage variations and/or circulating current at that time. The cost function presents a trade-off between the switching frequency or, consequently, the utilisation of the full bound width and the increased variations of the capacitor voltages and/or circulating currents.

![Waveforms of the output voltage.](image)

The capacitor voltages were balanced within 4% of their nominal values and Fig. 4.17 shows the waveforms of the capacitor voltages in phase-leg a for five periods. The arm currents and circulating current in phase-leg a are shown in Fig. 4.18. The circulating currents are controlled within 15% of the load currents. The simulated and experimental waveforms are similar.

![Waveforms of the capacitor voltages in phase-leg a.](image)

The THD of the load current and the switching frequency of the modules, for a range of bound widths, is shown in Fig. 4.19. The experimental results were captured on an oscilloscope in a CSV format and then PLECS was used to calculate THD. With the given bound width, THD was also calculated using (3.39), where $T_1 = T_r/2$ and $T_r = 1/(20 \times f)$. 
Because theoretical calculations do not account for the changing slope of the load current explained in (3.40), there is difference in the values of calculated and experimental results. Moreover, increased voltage variations and/or circulating current also restrict the trajectories from utilising the bounds, resulting in a difference in the values. Nonetheless, all the results show a similar trend. Over the range, the THD is a linear function of the bound width. It is evident from Fig. 4.19 that the THD can be lowered by reducing the bound width, but at the expense of increased switching frequency. Here, the switching frequency was calculated by counting the number of switching transitions of all the modules over a time period of 1 s.

Overall, the experimental and simulated results are in good agreement both in magnitude and trend. The discrepancy in the waveforms is due to a number of factors, such as the simulations do not consider delays associated with the ADCs and filters, and measurement noise. Moreover, the resistive elements that were considered in the simulations, as constant losses, were all estimated values, and thus add to the slight discrepancy seen
in the waveforms.

### 4.3.5 Performance During Transients

The performance of the MPDCC scheme during transient operation was evaluated under two conditions. Initially, the converter was operating at rated load current before the current reference was changed to zero, termed as power-down, and after 1 s the load current reference was changed back to the rated current, termed as power-up. The bound width, $\delta = 0.64$ A, of the load current was not changed during transient operation. The experimental waveforms of the load and arm currents and the capacitor voltages during the power-down and power-up transients are shown in Fig. 4.20, Fig. 4.21 and Fig. 4.22, respectively. To enhance the readability of the time-axis in these figures, the power-down and power-up transients are shown to occur at 20 ms and 10 ms in their respective figures.

![Figure 4.20: Experimental waveforms of the load current during transient.](image-url)

![Figure 4.21: Experimental waveforms of the arm currents during transient.](image-url)

The load current, as shown in Fig. 4.20, takes less than 3 ms to track its reference waveform and has been kept within the specified bounds. MPDCC achieves a very fast
current response both at power-down and power-up. During these transients, the arm currents do not overshoot their steady-state peak values and, as a result, the capacitor voltages do not exhibit large oscillations. The capacitor voltages were kept balanced close to their nominal values. In addition, the capacitor voltages were not rapidly discharged to meet the load requirements, which means that the switch positions were manipulated in such a way that the load was supplied by the DC-link.

![CapacitorVoltages](image)

(a) Power-down

(b) Power-up

Figure 4.22: Experimental waveforms of the capacitor voltages in phase-leg a during (a) power-down and (b) power-up transient.

### 4.4 Summary

The performance of the proposed MPDCC scheme for M2LCs has been evaluated in this chapter. It has been shown that the MPDCC scheme requires a single control loop, without a modulator, to control the load currents within tight bounds around their sinusoidal references. Simulated results have been presented to validate the viability of the proposed control technique. Moreover, a comparison with a PWM based VOC scheme has also been carried out to demonstrate the improvements in performance associated with the MPDCC scheme. It has been shown that the MPDCC scheme achieves a very fast current response during transients, such as power-up and power-down. The capacitor voltages have been kept close to their reference values both during transients and steady-state operating conditions.

To validate the feasibility of the proposed concept, the experimental performance of a single-phase three-level 860-VA prototype M2LC has been presented with discussion. It has been demonstrated with experimental results that bounds of the load current determine the THD of the current. Moreover, over a certain range, the THD of the current is a linear function of the bound width. At each sampling instant, the switch position with the minimum cost is applied to the converter, where the cost function is a measure
of the average switching frequency, capacitor voltage variations and circulating currents. As MPDCC is computationally expensive, most of the calculations were computed offline to reduce the computational burden and a simple yet effective approach has also been discussed to further reduce the computational time.
Chapter 5

Modular Multilevel Converter with Voltage Correcting Modules: Concept

5.1 Introduction

The control of circulating currents in M2LCs is an ongoing area of research and several methods, as detailed in Chapter 2, have been proposed to minimise these currents. Typically, these methods are based on cascaded control loops with switching modules operating at high frequency. In the case of a high-power M2LC, however, operation at high switching frequency is not feasible. The MPDCC strategy, described in Chapter 3, has been proposed as a viable alternative to the typical cascaded loops. However, the computational burden associated with the MPDCC algorithm increases exponentially with the number of modules.

This chapter proposes a modified Modular Multilevel Converter topology that employs Voltage Correcting Modules (M2LC-VCM), as shown in Fig. 5.1, for minimising circulating currents and alleviating the disadvantages of the previous methods. One full-bridge module, which has a lower voltage rating than the half-bridge modules, is included in each arm to minimise the voltage discrepancy that produces circulating currents. The proposed topology allows for simple and decoupled control of the load and circulating currents without compromising the performance of the converter. This chapter presents a detailed description of the proposed topology along with two different schemes for controlling the full-bridge modules. Lumped and detailed models of the M2LC-VCM are also derived to accurately predict the behaviour of the capacitor voltages and arm currents. The lumped model, which treats the converter arms as individual entities, simplifies the analysis of the complete system. In contrast, the detailed model predicts the behaviour
of all of the modules and is useful in understanding the behaviour of the complete system with a high level of accuracy.

5.2 Proposed Topology (M2LC-VCM)

5.2.1 Configuration

The structure of the proposed M2LC-VCM topology, shown in Fig. 5.1, is similar to that of the conventional M2LC topology. With the M2LC-VCM, each phase-leg is divided into two symmetrical halves, known as arms. Each arm consists of \( N \) half-bridge modules, \( M_{rn}, \ r \in \{a, b, c\}, \ n \in \{1, 2, \ldots, 2N\} \), one full-bridge module, \( VCM_{rq}, \ q \in \{T, B\} \), an inductor, \( L \), and a resistor, \( R \). Each half-bridge module has two switching states, \( u_{rn} \in \{0, 1\} \), where state 1 corresponds to switch \( S_{rn,1} \) being on, connecting the capacitor \( C \) in the circuit. An appropriate switching pattern of the half-bridge modules produces a multilevel voltage at the output terminals of the converter, and controls the output power.

The full-bridge modules minimise the voltage discrepancy in each phase-leg, and thus
the circulating currents, as explained in the forthcoming sections. The full-bridge module has three switching states, \( u_{\text{vm},rq} \in \{-1, 0, 1\} \), which are associated with the polarity of the voltage injected by the module. Hereafter, the half-bridge modules and full-bridge modules are termed as power-modules and Voltage Correcting Modules (VCMs), respectively.

### 5.2.2 Operating Principles

The circulating current in a phase-leg, as presented in Section 2.3, consists of a DC component, \( i_{\text{cir},r} \), and harmonic component, \( i_{h,r} \), which can be related to the arm current, \( i_{rq} \), as

\[
i_{\text{cir},r} = \frac{i_T}{2} + \frac{i_B}{2} = i_{\text{cir},r} + \sum_{h=1}^{\infty} i_{h,r}. \tag{5.1}
\]

The DC/average component of the current is in proportion to the power delivered, or the load current. For a three-phase lossless system, the input and output power are related as follows

\[
V_{\text{DC}}I_{\text{DC}} = 3VI \cos(\phi) \tag{5.2}
\]

where \( V_{\text{DC}} \) and \( I_{\text{DC}} \) are the average DC-link voltage and current, and \( V \) and \( I \) are the RMS phase voltage and current, respectively. The symbol \( \phi \) denotes the phase angle between the phase-voltage, \( v_r \), and phase-current, \( i_r \). If the circuit parameters of all three phase-legs are symmetrical, then the average value of the circulating current is given by

\[
i_{\text{cir},r} = \frac{I_{\text{DC}}}{3} = \frac{VI \cos(\phi)}{V_{\text{DC}}} \tag{5.3}
\]

The harmonic currents manifest from the variations in the capacitor voltages [17]. The relationship between the circulating currents, the modulation scheme (and therefore switching states) and the capacitor voltages can be derived using the equivalent circuit of the proposed topology, as shown in Fig. 5.2. The power-modules are represented by controllable voltage sources, as expressed by (5.4a) and (5.4b)

\[
v_{rT} = \sum_{n=1}^{N} u_{rn}v_{c,rn} \tag{5.4a}
\]

\[
v_{rB} = \sum_{n=N+1}^{2N} u_{rn}v_{c,rn} \tag{5.4b}
\]

where \( v_{c,rn} \) is the voltage of the power-module capacitor. The VCMs are represented as
follows

\[ v_{CM,rq} = u_{vcm,rq}v_{vcm,rq} \]  

(5.5)

where \( v_{vcm,rq} \) is the voltage of the VCM capacitor.

\[ \frac{V_{DC}}{2} - v_{rT} - v_{CM,rT} - v_r = R_i r_T + L \frac{di_{rT}}{dt} \]  

(5.6a)

\[ \frac{V_{DC}}{2} - v_{rB} - v_{CM,rB} + v_r = R_i r_B + L \frac{di_{rB}}{dt}. \]  

(5.6b)

Adding (5.6a) and (5.6b), and using (5.1), the relationship between the circulating currents and the various voltages in a phase-leg can be established as

\[ 2L \frac{d\bar{i}_{cir,r}}{dt} + 2R\bar{i}_{cir,r} = (V_{DC} - v_{rT} - v_{rB}) - (v_{CM,rT} + v_{CM,rB}). \]  

(5.7)

It is clear from (5.7) that the harmonics of the circulating currents can be controlled through the voltage that is injected by the VCMs, \((v_{CM,rT} + v_{CM,rB})\). Subtracting (5.6a) from (5.6b) the output voltage of the converter can be expressed as

\[ v_r = \frac{v_{rB} - v_{rT}}{2} + \frac{v_{CM,rB} - v_{CM,rT}}{2} + \frac{R}{2} (i_{rB} - i_{rT}) + \frac{L}{2} \left( \frac{di_{rB}}{dt} - \frac{di_{rT}}{dt} \right). \]  

(5.8)
The VCMs have only a minor impact on the output voltage for two reasons. Firstly, the magnitude of the voltage injected by each VCM is smaller than the voltage-step of the output voltage. Secondly, as described in the following section, the VCMs are controlled in such a manner that the inserted voltages are equal in the respective arms. Therefore, the voltage difference in (5.8), \((v_{CM,rB} - v_{CM,rT})/2\), is zero.

### 5.3 Control Philosophy

The control scheme for the power-modules and VCMs is split into two concurrent loops, as shown in Fig. 5.3. The first loop controls the load current and determines the switching pattern to balance the capacitor voltages. Various modulation schemes, such as Stair-Case Modulation (SCM) and Optimised Pulse Patterns (OPPs) [63], [132], are appropriate for reducing the switching frequency for a given load current distortion, and can thus be a part of this loop.

![Figure 5.3: Block diagram of the decoupled control scheme.](image)

The number of power-modules that are connected in an arm controls the load-current, whereas selection of these modules balances the capacitor voltages. Since the control of the load current was already discussed in Chapter 2, it is not repeated here. The capacitor voltages are balanced by using a simple and commonly used sorting algorithm, which is explained in Section 2.4.1.2.

The circulating currents, as given by (5.1), consist of a number of harmonics, which can be minimised by inserting an appropriate voltage in accordance with (5.7). The second
loop controls the circulating currents by controlling the VCMs. Two control schemes are proposed for controlling the VCMs and described in the following sections.

### 5.3.1 Independent Phase-Leg Control

The control scheme for the VCMs in a phase-leg, as shown in Fig. 5.4, regulates the circulating currents and maintains the capacitor voltage of each VCM at its nominal value. With this scheme, the VCMs in each phase-leg are controlled independently of the others.

In each phase-leg, the circulating current is compared with a reference, $i_{\text{cir,ref}}$, and a Proportional (P) controller is used to generate a voltage reference for the VCMs. This voltage reference is divided equally and added to the reference of the top and bottom VCMs in each phase-leg to minimise the effect of the VCMs on the output voltage, see (5.8).

A PI controller is used to regulate the capacitor voltage of the VCMs at their nominal value, $v_{\text{vcm,ref}}$. The output of the PI controller is multiplied with a sign function that is based on the polarity of the arm current. For a positive arm current the sign is positive and vice versa. Although the sign function adds a discontinuity to the voltage reference of the VCMs, it helps in keeping the VCM capacitor voltages at their nominal value.

A PWM switching scheme, where the voltage reference $v_{\text{CMRef,rq}}$ is compared against carrier waveforms, is used to generate the gate signals of switches $S_{1,rq} - S_{4,rq}$. The switches in the two legs of the VCMs (full-bridge) are not switched at the same time in accordance with the unipolar voltage switching [129]. Thus, the unipolar scheme doubles the switching frequency appearing in the harmonic spectrum of the voltage injected by the VCMs.

![Figure 5.4: Independent control of VCMs in a phase-leg.](image-url)
The implementation of the independent phase-leg control is simple as it uses a proportional controller in each phase-leg for minimising the circulating current. However, the proportional controller might not be effective in suppressing all of the harmonics of the circulating currents. Therefore, there is a trade-off between the simple implementation and the effectiveness of the scheme.

### 5.3.2 Synchronous Control

This control scheme utilises the symmetry of the three-phase converter to control the VCMs. The structure of the scheme, as shown in Fig. 5.5, is similar to that of the commonly known Field Oriented Control (FOC) or VOC.

![Figure 5.5: Synchronous control of VCMs.](image)

Typically, the second-order harmonic is the major component of the circulating currents and is in negative-sequence to the load currents [17], [20], [60]. With the synchronous controller, the three-phase circulating currents in the negative-sequence acb (stationary frame) are transformed into dq components (rotating frame) using $\theta = 2\omega t$ as a reference angular position. The dq current components are then compared with their reference values and a PI controller is used to generate the voltage references for the VCMs. The voltage references are then transformed into acb components, equally divided and added to the references of the top and bottom VCMs in each phase-leg, in accordance with the explanation given in Section 5.3.1. The angle $\theta$, shown in Fig. 5.5, is tuned to the major harmonic component of the circulating currents. In the case of multiple major harmonic components, multiple acb to dq transformations are required for minimising the circulating currents.

The synchronous controller maintains the VCM capacitor voltages at the nominal values using PI controllers and its control principle, which is not repeated here, is similar...
to that of the independent phase-leg controller.

5.4 Modelling

The purpose of this section is to derive a mathematical model of the M2LC-VCM. The model needs to predict the behaviour of the load- and circulating-currents, and the capacitor voltages of both the power-modules and the VCMs with sufficient accuracy. The development of a model is also a first step towards analysing the performance of the proposed topology. Moreover, the model can be regarded as a tool that facilitates both the proper controller design and physical design of the M2LC-VCM.

A state-space model represents a system mathematically as a set of inputs, outputs, and state variables that are related to each other by a series of first-order differential equations [133]. Moreover, systems with Multiple-Inputs and Multiple-Outputs (MIMO) can easily be represented in the compact form of the state-space model. Since a state-space model predicts the behaviour of all of the state variables over time, it is appropriate for modelling and understanding the behaviour of the M2LC-VCM, which is also a MIMO system.

Two state-space models, which are generalised for \( N \) power-modules and one VCM per arm of the converter, are presented. The first model is a detailed state-space model, which is derived to predict the behaviour of all the modules. The second model, a lumped state-space model, represents each arm as a controllable voltage source. With the lumped model, the behaviour of a single module, which acts as a controllable voltage source, is predicted, emulating the combined behaviour of all of the modules in an arm.

5.4.1 Properties of the M2LC-VCM

The following important properties of the M2LC-VCM are accounted for in the models in order to accurately characterise the behaviour of the proposed topology.

5.4.1.1 Configuration

The power-modules and VCMs are configured as half-bridge and full-bridge converters, respectively. Both types of module have a capacitor connected to the terminals. The capacitor acts as a voltage source of the corresponding module. The power-module can either bypass or connect its capacitor in the circuit, thus having two switching states, \((0, 1)\). The VCM, in contrast, can either bypass or connect its capacitor in both forward and reverse polarity, thus having three switching states, \((0, 1, -1)\). The switching states
for the power-module and VCM\(^1\) are summarised in Tables 5.1 and 5.2, respectively. Therefore, the models need to have two types of input variables, one for each module.

Table 5.1: Switching states for the Power-Module.

<table>
<thead>
<tr>
<th>Switching State</th>
<th>Power-Module Voltage</th>
<th>Switching Combinations</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(v_{c,rn})</td>
<td>1 0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0 1</td>
</tr>
</tbody>
</table>

Table 5.2: Switching states for the VCM.

<table>
<thead>
<tr>
<th>Switching State</th>
<th>VCM Voltage</th>
<th>Switching Combinations</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(v_{vcm, rq})</td>
<td>1 0 0 1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1 0 1 0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0 1 0 1</td>
</tr>
<tr>
<td>−1</td>
<td>(−v_{vcm, rq})</td>
<td>0 1 1 0</td>
</tr>
</tbody>
</table>

5.4.1.2 Dynamics

The switching frequency of the VCMs is selected to be higher than that of the power-modules so as to suppress higher order circulating currents. Thus, the pulse pattern of the VCM switches is different from that of the power-modules. Consequently, the switching dynamics of the VCMs are different from those of the power-modules.

5.4.1.3 Objectives

The objectives of the power-modules and VCMs are to control the load- and circulating-currents, respectively. The load current controller determines the number of power-modules to be connected in an arm, thus regulating the voltage levels of the synthesised multilevel waveform. The circulating current controller enables the VCMs to minimise the voltage discrepancy in each phase-leg, thus minimising the circulating currents. Nonetheless, the control of the power-modules, as presented in Section 5.3, is decoupled from that of the VCMs. Thus, the model needs to be able to handle two types of switching patterns that are generated by the decoupled control schemes.

\(^1\)With the VCM, there are two switching combinations which produce the same state 0. These combinations can be used for improving the power loss distribution of the switches.
5.5 Detailed Model

A detailed state-space model is derived by using a M2LC-VCM topology with $N$ power-modules and one VCM in each arm, as shown in Fig 5.1.

It is easy to establish, using network analysis, that there are five independent currents in the topology. The arm currents in phases $a$ and $b$, $i_{aT}, i_{AB}, i_{BT}, i_{BB}$ and DC-link current, $i_{DC}$, are chosen to be independent state variables. These variables can be related as follows:

\[ i_{DC} = i_{aT} + i_{bT} + i_{cT} \]  
\[ i_{DC} = i_{aB} + i_{bB} + i_{cB} \] (5.9a)
\[ i_a = i_{aT} - i_{aB} \] (5.9b)
\[ i_b = i_{bT} - i_{bB} \] (5.9c)
\[ i_c = i_{cT} - i_{cB} \]
\[ i_c = -i_{aT} + i_{aB} - i_{bT} + i_{bB}. \] (5.9d)

The relationship between the independent currents, grid voltage, $v_{g,r}$, and output voltage of both the power-modules, $v_{rn}$, and VCMs, $v_{CM,rq}$, using Kirchhoff’s voltage law around the five circuit loops, is given below:

Loop EABE

\[ L \frac{di_{aT}}{dt} + L \frac{di_{aB}}{dt} = -R_i aT - R_i aB - v_a - v_{a1} - v_{a2} \cdots - v_{a2N} - v_{CM,aT} - v_{CM,aB} + V_{DC} \] (5.10a)

Loop EACE

\[ L \frac{di_{bT}}{dt} + L \frac{di_{bB}}{dt} = -R_i bT - R_i bB - v_b - v_{b1} - v_{b2} \cdots - v_{b2N} - v_{CM,bT} - v_{CM,bB} + V_{DC} \] (5.10b)

Loop EADE

\[ -L \frac{di_{aT}}{dt} - L \frac{di_{aB}}{dt} - L \frac{di_{bT}}{dt} - L \frac{di_{bB}}{dt} + 2L \frac{di_{DC}}{dt} = R_i aT + R_i aB + R_i bT + R_i bB - 2R_i DC \]
\[ - v_{c1} - v_{c2} \cdots - v_{c2N} - v_{CM,cT} - v_{CM,cB} + V_{DC} \] (5.10c)

Loop EBFCE

\[ -L_1 \frac{di_{aT}}{dt} + (L_1 + L) \frac{di_{aB}}{dt} + L_1 \frac{di_{bT}}{dt} - (L_1 + L) \frac{di_{bB}}{dt} = R_i aT - (R + R_i) i_{aB} - R_i i_{bT} + v_{g,a} \]
\[ - v_{a(N+1)} \cdots - v_{a2N} - v_{CM,aB} + v_{CM,bB} + v_{b(N+1)} \cdots + v_{b2N} + (R + R_i) i_{bB} - v_{g,b} \] (5.10d)
5.5 Detailed Model

Loop EBFDE

\[
2L_1 \frac{di_aT}{dt} - 2(L + L_1) \frac{di_aB}{dt} + L_1 \frac{di_bT}{dt} - (L + L_1) \frac{di_bB}{dt} + L \frac{di_{DC}}{dt} = -2R_i aT + 2(R + R_i) i_aB \\
- R_i i_B + (R + R_i) i_B - R_i_{DC} + v_{CM,aB} + v_{a(N+1)} \ldots + v_{a2N} - v_{CM,eB} - v_{g,a} + v_{g,c} \\
- v_{c(N+1)} \ldots - v_{c2N}
\]

(5.10e)

where the parameters \( R, R_i, L \) and \( L_1 \) are the arm resistance, load resistance, arm inductance and load inductance, respectively.

The capacitors are charged or discharged depending on the switching states of the modules and the polarity of the arm current. Since a power-module is configured as a half-bridge converter, it has two switching states \( u_{rn} \in \{0, 1\} \), where 0 and 1 correspond to the voltages of 0 and \( v_{c,rn} \), as summarised in Table 5.1. The state equations of the capacitor voltages of the power-modules are

\[
C \frac{dv_{c,rn}}{dt} + \frac{v_{c,rn}}{R_{cap}} = i_rTu_{rn} \quad n \in \{1, 2, \ldots, N\}
\]

(5.11a)

\[
C \frac{dv_{c,rn}}{dt} + \frac{v_{c,rn}}{R_{cap}} = i_rBu_{rn} \quad n \in \{N + 1, N + 2, \ldots, 2N\}
\]

(5.11b)

where the parameter \( R_{cap} \) models the losses associated with the power-module and parameter \( C \) is the capacitance of the power-module.

A VCM, which is configured as a full-bridge converter, has three switching states \( u_{vcm,rq} \in \{-1, 0, 1\} \), where \(-1, 0\) and 1 corresponds to the voltages of \(-v_{vcm,rq}, 0\) and \( v_{vcm,rq} \), as summarised in Table 5.2. The state equation of the VCM capacitor voltage is

\[
C_{vcm} \frac{dv_{vcm,rq}}{dt} + \frac{v_{vcm,rq}}{R_{vcm}} = i_{rq}u_{vcm,rq}
\]

(5.12)

where the parameter \( R_{vcm} \) models the losses associated with the VCM and the parameter \( C_{vcm} \) is the capacitance of the VCM.

The state variables of the model are the arm currents in phases \( a \) and \( b \), the DC-link current, the grid voltages in the \( \alpha\beta \) coordinate system and the capacitor voltages of both the power-modules and the VCMs. The state-vector of the model is thus defined as

\[
\mathbf{x}_d = [i_aT \ i_aB \ i_BT \ i_BB \ i_{DC} \ v_{g,a} \ v_{g,b} \ v_{c,a1} \ v_{c,b1} \ldots v_{c,a2N} \ v_{vcm,aT} \ v_{vcm,aB} \ldots \ v_{vcm,cB}]^T
\]

(5.13)

and the input vector is formed by the switching states of both the power-modules and VCMs

\[
\mathbf{u}_d = [u_{a1} \ u_{a2} \ldots u_{a2N} \ u_{vcm,aT} \ u_{vcm,aB} \ldots u_{vcm,cB}]^T.
\]

(5.14)
The load- and circulating-currents along with the capacitor voltages of both the power-modules and the VCMs constitute the system output vector, which is denoted as

\[ y_d = [i_a \ i_b \ i_c \ i_{\text{cir},a} \ i_{\text{cir},b} \ i_{\text{cir},c} \ v_{c,a1} \ v_{c,a2} \ldots v_{c,2N} \ v_{\text{vcm},a} \ v_{\text{vcm},aB} \ldots v_{\text{vcm},cB}]^T. \] (5.15)

The complete system can be expressed in the standard state-space form as

\[ \frac{dx_d}{dt} = A_d x_d + B_d u_d + V_d \] (5.16a)

\[ y_d = C_d x_d. \] (5.16b)

The definitions of the system matrices \( A_d, B_d, V_d \) and \( C_d \) are given in Appendix B.1.

If all the switching states are evaluated at each sampling instant, then the total number of switching combinations can be evaluated as \( \binom{2N}{N} = \frac{2^N}{N! \times N!} \), as described in Section 2.2.1. It is evident from Fig. 5.6 that the number of combinations and, consequently, the computational burden increases exponentially with the number of modules.

![Switching combinations](image)

**Figure 5.6: Switching combinations.**

## 5.6 Lumped Model

The matrix size of the detailed model increases proportionally with the number of power-modules in each arm, \( N \). Therefore, the complexity of the model and the computational effort required to solve the equations also increases with \( N \), as does the complexity of the simulated control scheme.

For a large \( N \) and the reasonable assumption of a balanced system, the voltages of all the power-modules can be considered identical and the voltage difference among the capacitors of each arm can be considered negligible. Thus, the behaviour of all the modules with discrete dynamics can be modelled with a continuous voltage source in each arm,
5.6 Lumped Model

where the latter forms the basis of the derived lumped model. Various modelling methods such as [17], [88], [89], [134] have considered a substituted power-module, which acts as a continuous voltage source, to investigate the performance of the conventional M2LC topology. The modelling of the converter then becomes relatively easy due to reduced number of state variables.

5.6.1 Characteristics of the Lumped Model

Each arm is represented by a power-module and a VCM, as shown in Fig. 5.7. The capacitance of the power-modules and VCMs is $C_N$ and $C_{vcm}$, respectively. Three important characteristics of the model are presented below:

![Figure 5.7: Lumped model of the M2LC-VCM.](image)

(1) Continuous Dynamics

The switching function or modulation function, $m_{pm,rq}$, of the power-module is varied continuously with the fundamental frequency of the load current. This implies that only the fundamental component of the pulse pattern is considered for investigating the performance of the converter.
The switching function or modulation function, \( m_{\text{vcm,rq}} \), of the VCM, however, is piecewise continuous, where the zero crossing of the arm current triggers a discontinuity in the function.

(2) Controlled Voltage Source

With a conventional arm, the voltage inserted by the modules is varied sinusoidally by changing the number of connected modules over the range 0 to \( N \). To simulate this characteristic of the conventional arm, the power-module inserts a voltage, \( v_{rq} \), that is a function of \( m_{\text{pm,rq}} \) and capacitor voltage, \( \overline{v}_{\text{pm,rq}} \), as given by:

\[
v_{rq} = m_{\text{pm,rq}} \overline{v}_{\text{pm,rq}}, \quad m_{\text{pm,rq}} \in [0, 1]
\]  

(5.17)

Similarly, the voltage inserted by the VCM in an arm, \( v_{\text{CM,rq}} \), is a function of \( m_{\text{vcm,rq}} \) and capacitor voltage, \( \overline{v}_{\text{vcm,rq}} \), as given by:

\[
v_{\text{CM,rq}} = m_{\text{vcm,rq}} \overline{v}_{\text{vcm,rq}}, \quad m_{\text{vcm,rq}} \in [-1, 1].
\]  

(5.18)

(3) Controlled Current Source

With the lumped model, a controlled current source, \( i_{\text{pm,rq}} \), is used to charge and discharge the capacitor of the power-module. The controlled current, modulation function of the power-module, and arm current are related by

\[
i_{\text{pm,rq}} = m_{\text{pm,rq}} i_{rq}.
\]  

(5.19)

Similarly, the controlled current of the VCM, \( i_{\text{vcm,rq}} \), varies with the modulation function of the VCM as

\[
i_{\text{vcm,rq}} = m_{\text{vcm,rq}} i_{rq}.
\]  

(5.20)

5.6.2 Circuit Analysis

The capacitor voltage of the power-modules, \( \overline{v}_{\text{pm,rq}} \), varies with the arm current, \( i_{rq} \), using (5.19), as follows:

\[
\frac{C}{N} \frac{d\overline{v}_{\text{pm,rq},T}}{dt} = \overline{i}_{\text{pm,rq},T} - \frac{\overline{v}_{\text{pm,rq},T}}{R_{\text{pm}}} = m_{\text{pm,rq},T} i_{rq} - \frac{\overline{v}_{\text{pm,rq},T}}{R_{\text{pm}}}
\]  

(5.21a)

\[
\frac{C}{N} \frac{d\overline{v}_{\text{pm,rq},B}}{dt} = \overline{i}_{\text{pm,rq},B} - \frac{\overline{v}_{\text{pm,rq},B}}{R_{\text{pm}}}
\]
where $R_{\text{pm}}$ is used to model the losses in the power-module. In general, $m_{\text{pm},rq}N$ is equivalent to the number of power-modules that are connected in an arm and $v_{\text{pm},rq}$ is equivalent to the summation of all the capacitor voltages of the conventional arm. Similarly, the voltage of the VCM capacitor, $v_{\text{vcm},rq}$, can be related to the arm current, using (5.20), as follows:

$$
C_{\text{vcm}} \frac{d}{dt} v_{\text{vcm},rT} = i_{\text{vcm},rT} - \frac{v_{\text{vcm},rT}}{R_{\text{vcm}}}
$$  (5.22a)

$$
C_{\text{vcm}} \frac{d}{dt} v_{\text{vcm},rB} = i_{\text{vcm},rB} - \frac{v_{\text{vcm},rB}}{R_{\text{vcm}}}
$$  (5.22b)

where $R_{\text{vcm}}$ is used to model the losses in the VCM.

The formulation of the lumped model is similar to that of the detailed model. The five independent currents, i.e. the arm currents in phases $a$ and $b$, and the DC-link current, the grid voltages in the $\alpha\beta$ coordinate system, and the capacitor voltages of both the power-modules and the VCMs are the state variables of the lumped model. The state-vector of the model is defined as

$$
x_\xi = [i_a \ T \ i_B \ i_a \ b \ i_a \ T \ v_{g,a} \ v_{g,b} \ v_{\text{pm},a} \ T \ v_{\text{pm},ab} \ \ldots \ v_{\text{pm},c} \ T \ v_{\text{vcm},a} \ T \ v_{\text{vcm},ab} \ \ldots \ v_{\text{vcm},c} \ T]^T.
$$  (5.23)

The input vector is formed by the modulation functions of both the power-modules and the VCMs as

$$
u_\xi = [m_{\text{pm},aT} \ m_{\text{pm},ab} \ \ldots \ m_{\text{pm},cT} \ m_{\text{vcm},aT} \ m_{\text{vcm},ab} \ \ldots \ m_{\text{vcm},cT}]^T.
$$  (5.24)

The load- and circulating-currents along with the capacitor voltages of both the power-modules and VCMs constitute the system output vector, which is defined as follows:

$$
y_\xi = [i_a \ i_b \ i_c \ i_{\text{cir},a} \ i_{\text{cir},b} \ i_{\text{cir},c} \ \ldots \ v_{\text{pm},aT} \ v_{\text{pm},ab} \ \ldots \ v_{\text{vcm},aT} \ v_{\text{vcm},ab} \ \ldots \ v_{\text{vcm},cT}]^T.
$$  (5.25)

The complete system can be expressed in the standard state-space form as:

$$
\frac{dx_\xi}{dt} = A_\xi x_\xi + B_\xi u_\xi + V_\xi  
$$  (5.26a)

$$
y_\xi = C_\xi x_\xi.
$$  (5.26b)
The definitions of the system matrices $A_\xi$, $B_\xi$, $V_\xi$ and $C_\xi$ are given in Appendix B.2.

In the case of lumped model, the computational burden remains the same, because only the parameter $N$ is changed to account for the increased number of modules.

### 5.6.3 Inputs

The inputs to the model are the modulation functions of both the power-modules and the VCMs. The modulation function of the power-module can be defined as

$$m_{pm,rT} = \frac{1 - M \cos(\omega t + \phi_r)}{2}$$

(5.27a)

$$m_{pm,rB} = \frac{1 + M \cos(\omega t + \phi_r)}{2}$$

(5.27b)

where $M$ is the modulation index of the phase voltage and $\phi_r$ is the angle between the phase-voltage, $v_r$, and phase-current, $i_r$.

The modulation function of the VCMs when controlled by the independent phase-leg controller can be expressed as

$$m_{vcm,rT} = 0.5K(i_{cir,r} - i_{cir,ref}) + sgn(i_{rT})\left[K_p (v_{ref} - \overline{v}_{vcm,rT}) + K_i \int (v_{ref} - \overline{v}_{vcm,rT})\right]$$

(5.28a)

$$m_{vcm,rB} = 0.5K(i_{cir,r} - i_{cir,ref}) + sgn(i_{B})\left[K_p (v_{ref} - \overline{V}_{vcm,rB}) + K_i \int (v_{ref} - \overline{V}_{vcm,rB})\right]$$

(5.28b)

where, $K$, $K_p$ and $K_i$ are the controller gains. The value of the function $sgn(x)$ is one for $x \geq 0$, and otherwise zero. Consequently, the function yields a piecewise continuous modulation function for the VCMs. The modulation function of the VCMs when controlled using the synchronous control can be expressed in a similar manner, but with the minor difference of the implementation of the current control being in the $dq$ reference frame.

### 5.7 Design Aspects

The dimensioning of the VCMs can be performed after selecting the capacitance of the power-modules and the arm inductance, where the latter can be selected using guidelines such as [53], [54]. The voltage rating of the VCM switches is equal to the average maximum voltage of the VCM capacitors and the voltage is primarily governed by the voltage discrepancy in each phase-leg (5.7). This discrepancy, which is a function of the circuit parameters, can be determined using the derived models. In general, the circulating
currents can only be suppressed if the average voltage is sufficient to minimise the voltage discrepancy.

Because the arm current flows through the VCM switches, the current rating of the VCM switches is the same as that of the power-modules. The variation in the VCM capacitor voltages is a function of the VCM capacitance and the arm currents. The capacitance, which yields an appropriate voltage variation, can also be determined using the model.

The switching frequency of the VCM depends on the frequency of the circulating currents to be minimised. Typically, the frequencies of the most dominant harmonics are 100 Hz (second harmonic) and 200 Hz (fourth harmonic) for a fundamental frequency of 50 Hz. Therefore, the switching frequency for which the VCMs yield an appropriate performance can also be selected using the model. In general, the switching frequency of the VCMs should be at-least five times the frequency of the most dominant harmonic currents. Selecting a switching frequency, which is too close to the frequency of the most dominant harmonics, for example 400 Hz, could limit the VCMs’ ability to reduce the circulating currents.

The reliability of the converter can be improved by adding redundant VCMs in each arm. In the case of a fault in a VCM, the redundant VCM continues to operate without any interruption, and the faulty VCM can be replaced at the next scheduled maintenance.

5.8 Summary

This chapter has presented a modified M2LC topology that employs VCMs for minimising the circulating currents. The VCM can be regarded as an active compensator that minimises the voltage-discrepancy in each phase-leg of the converter. The VCMs do not excessively increase the switching losses even when their switching frequency is higher than the power-modules, because of the lower voltage ratings. With the higher switching frequency, the bandwidth of the circulating current control loop can be much larger than the load current control loop. From the control perspective, the modified topology has two main advantages. Firstly, a simple control scheme can be used to control the load current or output voltage. Secondly, the control of the circulating currents is decoupled from the load currents, where the load- and circulating-currents are controlled by the power-modules and VCMs, respectively. Moreover, the number of output voltage levels of the converter is not affected by the presence of the VCMs.

This chapter has also presented detailed and lumped models for investigating the performance of the proposed topology. The detailed model was formulated by using all the independent currents and voltages as state variables of the model. Consequently, the
complexity of the detailed model increases proportionally with the number of modules. In contrast, the lumped model has been developed using an equivalent circuit of the topology, where the discrete dynamics of all the power-module capacitor voltages in an arm are described by a single module with continuous dynamics. The model does not characterise the behaviour of an individual module, but predicts the behaviour of the arm voltages. The single module approach simplifies the modelling of the converter and reduces the computational time for solving the equations and carrying out simulations.
Chapter 6

Modular Multilevel Converter with Voltage Correcting Modules: Performance Analysis

6.1 Introduction

The M2LC-VCM topology was proposed in Chapter 5 as a solution for minimising the circulating currents. This chapter evaluates the performance of the M2LC-VCM. Simulated and experimental results are presented with discussion, in order to demonstrate the improvements in performance associated with the M2LC-VCM.

The performance of the two control schemes for the VCMs, which are described in Section 5.3, have been evaluated and the results are presented in order to demonstrate the effectiveness of both schemes. Theoretical as well as experimental results for a single-phase three-level 800-VA prototype converter are presented to demonstrate the viability of the proposed mathematical models. Moreover, the performance of the M2LC-VCM is investigated for a range of circuit parameters, with the results revealing that the circulating currents have been minimised over the range of values that are considered.

6.2 Simulation Results

The viability of the proposed topology was verified using PLECS/SIMULINK simulations for a 2-MVA M2LC-VCM connected to a three-phase grid. Each arm of the three-phase converter comprises four power-modules and one VCM. The circuit parameters used for the simulations are summarised in Table 6.1. A VOC scheme with PWM, where the carrier waveforms were at 750 Hz in PD, was used to regulate the rated load current at unity power factor. The capacitor voltages were balanced by using the sorting algorithm
that was discussed in Chapter 2. In the following discussion, the performance of the M2LC-VCM is compared against the conventional topology, which was also controlled using the VOC scheme.

Table 6.1: Parameters of the three-phase M2LC-VCM setup.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output frequency ( f )</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Supply voltage ( V_{DC} )</td>
<td>5.2 kV</td>
</tr>
<tr>
<td>Grid RMS voltage ( V_l )</td>
<td>3 kV</td>
</tr>
<tr>
<td>Load RMS current ( I_r )</td>
<td>365 A</td>
</tr>
<tr>
<td>Power-module capacitance ( C )</td>
<td>5 mF</td>
</tr>
<tr>
<td>VCM capacitance ( C_{vcm} )</td>
<td>5 mF</td>
</tr>
<tr>
<td>Load inductance ( L_l )</td>
<td>5.23 mH</td>
</tr>
<tr>
<td>Arm inductance ( L )</td>
<td>1.5 mH</td>
</tr>
</tbody>
</table>

6.2.1 Performance Evaluation

The performance of the conventional topology is used to benchmark the performance of the M2LC-VCM. The conventional topology was controlled using VOC scheme described in Section 4.2. In order to further understand the M2LC-VCM, both an independent phase-leg controller and a synchronous controller were used to control the VCMs and the performance of the M2LC-VCM with these controllers is presented as VCM with control-1 and VCM with control-2, respectively. The switching frequency of the VCMs with both the controllers was 600 Hz.

Fig. 6.1 shows the simulated waveforms of the arm currents in phase-leg \( a \) to demonstrate that the second harmonic of the current is significantly reduced with the proposed topology. Considering the arm currents with the conventional topology as base quantity.
ties, a relative reduction of more than 16% and 17% can be observed with control-1 and control-2, respectively. The waveforms of the currents in the other two phase-legs, which are phase shifted with respect to phase-leg \( a \), are not shown, in order to enhance clarity in the figures.

The arm current spectra and the AC components of the circulating currents are shown in Fig. 6.2 and Fig. 6.3, respectively. In the case of the conventional topology, the second harmonic of the arm current prevails due to the lack of circulating current control. It is evident from Fig. 6.3 that control-2 is most effective in minimising the circulating currents. The proportional controller, as used in control-1, is unable to suppress all the harmonic currents and, therefore, is less effective than the PI controller of control-2. Moreover, the VCMs do not affect the regulation of the load current, as is evident from the unchanged fundamental of 50 Hz and the DC components of the arm currents in Fig. 6.2.

![Arm current spectrum](image)

Figure 6.2: Arm current spectrum.

![Circulating currents](image)

Figure 6.3: Circulating currents.

Fig. 6.4 shows the waveforms of the capacitor voltages, which are balanced around their nominal values. The variation in the capacitor voltages is approximately 9% and
8% of the average value with control-1 and control-2, respectively. The conventional topology, in contrast, does not have the capability to limit the circulating currents and, consequently, the voltage variation is around 18% of the average value.

![Figure 6.4: Capacitor voltages of power-modules in phase-leg a.](image)

The voltages are balanced around the average value, which is 3.85% of the DC-link voltage. The circulating currents have been suppressed by the VCMs, whose voltage rating is lower than that of the power-modules.

![Figure 6.5: Capacitor voltages of VCMs in phase-leg a.](image)

6.3 Experimental Results

The results presented in the previous section show that the circulating currents can significantly be reduced by using a VCM in each arm. However, the simulations do not include any switching losses or other non-linear characteristics, so further experimen-
6.3 Experimental Results

tal verification is required to assess the improvement in performance associated with the M2LC-VCM. Moreover, the viability of the models needs to be verified using experiments.

6.3.1 M2LC-VCM Prototype

In order to investigate the performance of the proposed topology, a single-phase three-level 800-VA prototype M2LC-VCM was constructed. A circuit diagram and photograph of the experimental setup are shown in Fig. 6.6 and the parameters of the system are summarised in Table 6.2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output frequency</td>
<td>$f$</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>$V_{DC}$</td>
</tr>
<tr>
<td>Load RMS current</td>
<td>$I_l$</td>
</tr>
<tr>
<td>Power-module capacitance</td>
<td>$C$</td>
</tr>
<tr>
<td>VCM capacitance</td>
<td>$C_{vcm}$</td>
</tr>
<tr>
<td>Load resistance</td>
<td>$R_l$</td>
</tr>
<tr>
<td>Load inductance</td>
<td>$L_l$</td>
</tr>
<tr>
<td>Arm inductance</td>
<td>$L$</td>
</tr>
<tr>
<td>Number of modules</td>
<td>$N$</td>
</tr>
</tbody>
</table>

Table 6.2: Parameters of the single-phase M2LC-VCM setup.

The DC power supply can only supply a maximum peak current of 6 A. Without the circulating current control, the required maximum value of the DC-link current increases with the output power. In order to ensure that the current rating of the supply was not exceeded, the output power of the converter presented in Chapter 4 was reduced from 860-VA to 800-VA. The control scheme was implemented on a TMS320F28335 DSC. The DSC has an on-board ADC, which was used to measure the arm currents and the capacitor voltages. Altera’s DE2 FPGA board was used to generate dead-time for the switching signals of the modules and to safely shut down the converter in the unlikely event of a fault. An IGBT, IKW20N60H3, and a MOSFET, IRFP250MPBF, were used for the switches in the power-modules and VCMs, respectively.

At start-up, a resistor was connected in series with the DC-supply to charge the capacitors and it was bypassed during normal operation of the converter. The diode, $D$, as shown in Fig. 6.6, is a part of the DC-supply that was used in the experiments. The diode also ensured that the DC-link current was unidirectional, and this feature is congruent with the six-pulse or twelve-pulse diode rectifiers that are commonly used to supply DC-links in power converter applications.
6.3.2 Verification of the Models

This section presents the simulated performance of the models in comparison to measured performance of the single-phase M2LC-VCM prototype, to demonstrate the validity of the models. Both the detailed model (5.16) and lumped model (5.26) were modified to characterise the behaviour of the single-phase M2LC-VCM.

Both the simulations and experiments were carried out using the system parameters
6.3 Experimental Results

The experimental results were captured on an oscilloscope in a CSV format and then plotted in Matlab. For simulations, the control scheme and the model were implemented in Matlab/SIMULINK software. The VCMs were controlled using the independent phase-leg control scheme, which is presented in Section 5.3.1. The pattern of the switch inputs for the power-modules, which was computed offline, was stored in a table and used for controlling the power-modules. The same pattern was used in the experiments and simulations of the detailed model. The inputs to the lumped model were the modulation functions of the power-modules and the VCMs, which were determined by the independent phase-leg scheme as discussed in Section 5.6.3. These modulation functions were controlled to regulate the load current.

Fig. 6.7 shows the waveforms of the arm currents in phase-leg \( a \), which indicate that the results are similar in value and shape. Since continuous variables are used in the case of the lumped model, the switching harmonics are absent in the waveforms of the arm current. The detailed model is able to accurately describe both the lower and higher order harmonics of the arm currents. In contrast, the lumped model is able to accurately describe the lower order harmonics of the arm currents.

![Figure 6.7: Arm currents in phase-leg \( a \) with the experiments and models.](image)

The switching pattern applied to the power-modules determines the variations in the capacitor voltages. Results show that the simulated and experimental waveforms of the capacitor voltages, as shown in Fig. 6.8, are similar. Because the switching frequency of the power-modules with the experiments and detailed model is 380 Hz, there are variations in the peak values of the capacitor voltages. These variations can be decreased by increasing the switching frequency of the converter. The capacitor voltages of the VCMs, shown in Fig. 6.9, are kept balanced around an average value of 6 V, and the analytical and experimental waveforms are similar. Thus, the results validate the accuracy of both the simulated control scheme and the models.

Since the switching harmonics are accounted for in the detailed model, it is more
6.4 Performance Evaluation: Altering Modulation Strategy

The following sections investigate the performance of the M2LC-VCM using two modulation strategies for the power-modules, namely PWM and Stair Case Modulation (SCM).
The VCMs were controlled using the independent phase-leg controller, which does not require any *abc* to *dq* transformations, and can therefore be easily adapted for the single-phase M2LC-VCM.

### 6.4.1 Pulse Width Modulation

The performance of the proposed topology was compared against the conventional topology, where, in the case of the latter, the VCMs were bypassed during the experiments. The pulse patterns of the power-modules were computed offline by comparing a sinusoidal reference with carrier waveforms in Phase Disposition (PD). The resulting PWM based patterns were stored in a look up table and used for controlling the power-modules. In both cases, the system was operated at its rated conditions as given in Table 6.2. The switching frequency of the power-modules and VCMs was 380 Hz and 2 kHz, respectively. The sorting algorithm was used to balance the capacitor voltages of the power-modules.

Fig. 6.10 shows the waveforms of the arm currents in phase-leg *a* to establish that the VCMs reduce the second harmonic component of the arm current. Relative to the conventional topology, the RMS arm current is reduced by 3 % with the proposed topology.

![Waveforms of arm currents in phase-leg *a* using PWM.](image)

The arm current spectra, as shown in Fig. 6.11, further illustrates that the VCMs minimise the second harmonic of the arm current. However, the second harmonic is not fully suppressed, because a proportional controller is used to control the VCMs. The VCMs do not affect the load currents, as is evident from the waveforms of the currents shown in Fig. 6.12. Both waveforms are similar in value and trend.

Fig. 6.13 shows the waveforms of the DC-link current to demonstrate that the ripple in the DC-link current, or the harmonic circulating currents, are significantly reduced with the proposed topology. The magnitude of the current ripple is reduced by 65 % by using VCMs. The distinct feature of the VCMs is the ability to suppress the circulating currents.
even when the switching frequency of the power-modules is low. The benefit of this feature is prominent when the pulse number, which is the ratio of the switching frequency of the power-modules to the output fundamental frequency, is low. The low pulse number, or switching frequency, reduces the switching losses. Although the switching frequency of the VCMs is higher than the power-modules, the total switching-losses in the topology can be kept low due to the low voltage ratings of the VCMs.

Fig. 6.14 shows that the capacitor voltages of the power-modules are balanced around their nominal values. The average of the capacitor voltages is slightly lower than $V_{DC}/2 = 140\text{V}$ because of the voltage drop across the various resistances within the converter. Nonetheless, the waveforms in both cases show a similar trend.

The capacitor voltages of the VCMs, shown in Fig. 6.15, are balanced around an average value of 6 V, which is about 5 % of the voltage across the power-modules.
6.4 Performance Evaluation: Altering Modulation Strategy

![Figure 6.13: DC-link current using PWM.](image)

![Figure 6.14: Capacitor voltages of power-modules in phase-leg a using PWM.](image)

![Figure 6.15: Capacitor voltages of VCMs in phase-leg a.](image)

### 6.4.2 Stair Case Modulation

The SCM strategy was used to further evaluate the performance of the M2LC-VCM when the switching frequency of the power-modules is further reduced. With this strategy, the pulse patterns that eliminate the fifth harmonic of the output voltage waveform were
generated [74] and used to control the power-modules. The experiments were conducted using the circuit parameters listed in Table 6.2. In addition, the DC-link voltage, $V_{DC}$, was reduced to 268 V so that the converter delivered the rated load current with the given pattern. The sorting algorithm was used to balance the capacitor voltages. The switching frequency of the power-modules and VCMs was 50 Hz and 2 kHz, respectively.

The experimental waveforms of the arm and DC-link currents are shown in Fig. 6.16 and Fig. 6.17, respectively. The RMS arm current is reduced by 2 % relative to the conventional topology. In comparison to the conventional topology, the magnitude of the DC-link current ripple, shown in Fig. 6.17, is reduced by 58 %. These results clearly show that the power-modules can be switched at the fundamental frequency of the load current while achieving the appropriate control of the circulating currents.

Fig. 6.16 shows the spectra of the arm currents, which indicate that the second harmonic of the arm currents has been minimised with the proposed topology. Therefore, the
circulating currents can be suppressed even when the switching frequency of the power-modules is very low. Fig. 6.19 shows that the variation in the capacitor voltages is slightly reduced with the proposed topology. In comparison to the PWM strategy, the variations in the capacitor voltages are larger, because the number of switching transitions with the SCM strategy is lower than the PWM strategy.

6.5 Performance Evaluation: Altering Parameters

The circulating currents, which are driven by a small voltage difference in each phase-leg, can be reduced by increasing the size of the passive components, such as the arm inductance or the capacitance of the power-module [53]–[55]. As demonstrated in this chapter, the circulating currents can also be reduced by the VCMs. The VCM is an active compensator and, unlike the passive components, can adapt rapidly to variations in the operating conditions of the converter. Therefore, simulations using both the detailed
and lumped models were carried out for a range of inductor and capacitor values in order to evaluate the performance of the M2LC-VCM. The effects of such values on the arm and circulating currents are analysed under two scenarios. Firstly, the simulations were performed by bypassing the VCMs, meaning that the performance was analysed without the control of the circulating currents. Secondly, the performance was evaluated by connecting the VCMs. The circuit parameters used for the analysis can be found in Table 6.1. In the case of detailed model, the VOC scheme described in Section 4.2 was used to regulate the load current. In the case of lumped model, modulation functions were not compared with carrier waveforms and were used as inputs to the model.

Fig. 6.20 shows the RMS arm current for a range of capacitor and inductor values. The waveforms associated with and without the VCMs are indicated by the solid and dashed lines, respectively. The waveforms associated with the detailed and lumped models are unmarked and marked with a star marker, respectively. Without VCMs, the results clearly show that the RMS arm current can be reduced by increasing the module capacitance or arm inductance. Over the range of values considered, the RMS arm current with the VCMs connected is lower than without the VCMs. Moreover, the current remains the same with the VCMs connected, because the second harmonic component of the arm current remains suppressed and the system does not allow for further reductions.

![Figure 6.20: RMS arm current for a range of power-module capacitor and arm inductor values.](image)

**Fig. 6.21** shows that the RMS circulating current also reduces with increasing values of arm inductance and module capacitance. The RMS current in the case of the lumped model is slightly lower than the detailed model, because the lumped model ignores the higher order switching harmonics.

The improvement in performance can be measured by evaluating the difference between the currents without and with VCMs. The improvement, however, reduces with increasing arm inductance or module capacitance. Increasing the capacitance, where the voltage rating of the capacitor is equal to the step size of the output voltage, could in-
crease the monetary cost and footprint of the converter. Similarly, inductors, which are designed to operate in the low frequency range, are bulky and increase the footprint of the converter. A choice of employing VCMs for minimising the circulating currents depends on the selection of circuit parameters and the improvements associated with such a selection.

### 6.6 Summary

This chapter has demonstrated the viability of the M2LC-VCM for minimising the circulating currents. A simple decoupled control scheme has been used for controlling the converter, where the load and circulating currents are controlled by the power-modules and VCMs, respectively. Various simulations have been carried out to evaluate the performance of the M2LC-VCM and the results were presented with a discussion. The experimental results have shown that the M2LC-VCM achieves the appropriate control of the circulating currents even when the switching frequency of the power-modules is very low. A comparative investigation with respect to a conventional topology reveals that the proposed topology offers superior performance.

The validity of the detailed and lumped models has been demonstrated using simulated results that have been presented in comparison with the experimental results of a single-phase three-level 800-VA prototype M2LC-VCM. The detailed model predicts the behaviour of the converter with higher accuracy than the lumped model, because the switching harmonics are accounted for by the former model. However, the computational burden associated with the detailed model is greater than that of the lumped model. Both models have been used to investigate the effect of circuit parameters on the circulating currents. Simulated results have been presented with a discussion to analyse the improvement in performance associated with the VCM over a range of circuit parameters.
Chapter 7

A Modular Multilevel Converter based on Inductive Power Transfer Technology

7.1 Introduction

As in M2LCs, the DC-link capacitor is replaced with a number of module capacitors, with the voltage across each capacitor being significantly lower than the total DC-link voltage. Because the capacitors carry full load current, the voltage variations of the capacitors increase with the magnitude of the load current. The MPDCC scheme and M2LC-VCM topology, as presented in the previous chapters, have been proposed to minimise both the circulating currents and the capacitor voltage variations. These proposed methods, however, can only reduce voltage variations up to a certain level.

This chapter presents a variant of the M2LC topology, which incorporates Inductive Power Transfer (IPT) technology, to maintain capacitor voltages within tight bounds. With the proposed solution, capacitors whose voltages violate the bounds exchange power with each other in order to control the voltage variations. The IPT system is inductively coupled to the M2LC modules and, therefore, it provides a contactless interface for the capacitors to exchange power. Moreover, the proposed M2LC-IPT topology allows for simple and decoupled control of the load currents and capacitor voltages. Simulated performance of a single-phase three-level 800-VA M2LC-IPT is presented to demonstrate the feasibility of the proposed solution. Comparative investigations with respect to the M2LC-VCM topology are also carried out to analyse improvement in performance with the M2LC-IPT.
7.2 Inductive Power Transfer (IPT)

The concept of wireless/inductive power transfer has been known since 1800s and is based on the fundamental laws of electromagnetism: Ampère’s law and Faraday’s law. Ampère’s law [135] states that line integral of the magnetic field intensity, \( H \), around a closed loop is equal to the total (enclosed) current, \( I \), as expressed by the well-known equation

\[
\oint H \cdot dl = I. \tag{7.1}
\]

Faraday’s law states that voltage is induced across a coil when it is placed in an area with changing magnetic flux, \( \phi \), and the voltage, \( V \), is given by

\[
V = -\frac{d\phi}{dt}. \tag{7.2}
\]

A conductor carrying a time-varying current produces a time-varying magnetic field, which induces voltage in a coil when the coil is placed within the field. Therefore, electrical energy is transferred without any physical contacts between the conductor and the coil. Traditionally, the concept of wireless power has been used for transmitting information-bearing signals for radio/TV and mobile phones, over long distances. In the past decade, IPT systems have demonstrated the feasibility to transfer power in the range of several kWs over short distances [136]–[138]. IPT technology has a number of advantages over traditional wired connections, with some of the advantages being as follows:

1. Electrical isolation, as there are no physical contacts between the power transmitter and receiver sides.

2. Unaffected by water, snow, and dirt and able to operate in harsh environments. Moreover, safety can be improved by enclosing terminals and making airtight enclosures.

3. The wireless interface provides a convenient means of power transfer in certain applications.

4. Clean as there are no carbon brushes and contacts to produce debris in systems with moving parts.

Because of these advantages, IPT technology has been used in many applications, such as factory automation and clean rooms [139], wireless charging of electric vehicles [140], [141], biomedical implants [142], and power management in vehicle-to-grid and grid-to-vehicle systems [138], [143], [144].
A typical IPT system, as shown in Fig. 7.1, has two magnetically coupled sides, namely primary and pickup, which are separated by an air-gap. The operating principle of IPT systems is similar to that of transformers; however, the magnetic core of the transformer is replaced with a large air-gap in the magnetic path. The primary and pickup sides are identical, and consist of an inductor, resonant circuit and a converter.

![IPT System Diagram](image)

**Figure 7.1: IPT system.**

The open circuit voltage and short circuit current of the pickup inductor, \( L_{si} \), are the main attributes of IPT systems. The open circuit voltage, \( v_{OC} \), is the voltage induced in a pickup inductor [136], [137] and is given by

\[
v_{OC} = j\omega_T M i_T\tag{7.3}
\]

where \( M \) is the mutual inductance between primary and pickup inductors. The symbols \( i_T \) and \( \omega_T \) are the magnitude and angular frequency of the primary inductor (track) current, respectively. As per application requirements, the primary inductor can either be a coil or a long piece of wire.

The short circuit current, \( i_{SC} \), is the current of a shorted pickup inductor as given by

\[
i_{SC} = \frac{v_{OC}}{j\omega_T L_{si}} = \frac{M i_T}{L_{si}}.
\]

These two attributes are a measure of uncompensated power, \( S_U \), which reveals the power transfer capability of a pickup. The power is expressed as

\[
S_U = v_{OC} \times i_{SC} = \frac{\omega_T M^2 i_T^2}{L_{si}}.
\]

Typically, the primary and pickup inductors are loosely coupled with a coupling coefficient \( k_c \leq 0.5 \); therefore, IPT systems have a limited capacity to transfer power across the air-gap. To improve the power transfer capability, the pickup and primary inductors are generally compensated with a capacitor to form a resonant circuit. Different com-
Compensation topologies have emerged to compensate for the inductors, with each having its own advantages and disadvantages [145]. The compensating capacitor increases either the voltage or current of the resonant circuit and the increment is measured by a quality factor, $Q$, of the compensated circuit. Consequently, compensation increases the output power of the IPT pickup [146]. A $Q$ value of less than 10 is generally selected so as to minimise the pickup’s sensitivity to component variations.

7.3 M2LC based on IPT (M2LC-IPT)

An IPT system is added to the conventional M2LC topology, as shown in Fig. 7.2, to keep the capacitor voltages within prescribed bounds around their nominal values. With the proposed topology, a track in the form of a wire, or as appropriate, is laid out across the modules. Each module is magnetically coupled to the track, with the track providing a channel for the capacitors of each phase-leg to exchange their energy. The capacitor voltages are maintained within the prescribed bounds by controlling the amount of energy transferred or received by each capacitor. Minimising the capacitor voltage variations also reduces the circulating currents. For the proposed topology, M2LC-IPT, primary and pickup converters are needed to transfer power across the air-gap and, therefore, the

![Proposed M2LC-IPT topology](image_url)
configuration of these converters is discussed in the following sections.

### 7.3.1 Primary Converter

A typical converter that drives the primary side (track) of an IPT system is shown in Fig. 7.3. It comprises a DC voltage source, $V_{\text{in}}$, and H-bridge converter to control the track current, $i_T$. The output power of the pickup, given in (7.5), increases with the track current frequency, $f_T$. However, losses due to switching and the skin effect also increase with frequency and, therefore, the frequency is usually selected in the range of $10 - 80$ kHz for the highest to lowest power converters, respectively. The reactive power (VAr) requirements on the primary side are minimised by using an $L_{\text{pi}}$-$C_T$-$L_T$ arrangement as a resonant circuit [147]–[149]. The resonant circuit confines resonant circulating current within the circuit and compensates for the track inductor. Moreover, the resonant circuit improves the efficiency of the system, because resonant circulating current does not flow through the switches [144], [146], [150], [151].

![Figure 7.3: IPT primary converter.](image)

### 7.3.2 Pickup Converter

The pickup side also has a similar H-bridge converter and a resonant circuit. The pickup inductor is magnetically coupled to the track through the mutual inductance, $M_{rn}$, $r \in \{a, b, c\}$, $n \in \{1, 2, \ldots, 2N\}$. In order to exchange power between module capacitors and the IPT track, an IPT pickup is added to each M2LC module, as shown in Fig. 7.4. Each pickup comprises an H-bridge converter formed by switches $S_{s1,rn} - S_{s4,rn}$ and a resonant circuit formed by $L_{si,rn}$-$C_{si,rn}$-$L_{so,rn}$. The H-bridge converter allows for bidirectional power flow between the track and the module capacitor, $C_{rn}$. The resonant circuit is tuned to the frequency $f_T$ of the track current. The operating principle of the pickup converter is similar to that of the primary converter.
### 7.4 Operating Principles

The voltage, $v_{si, rn}$, induced in the pickup inductor, due to the track current, is given by

$$v_{si, rn} = j \omega_T M_{rn} i_T. \quad (7.6)$$

Because each pickup is magnetically coupled to the track inductor, the voltage, $v_{T, rn}$, is reflected back on to the track current, due to each pickup current, and the voltage can be expressed as

$$v_{T, rn} = -j \omega_T M_{rn} i_{si, rn} \quad (7.7)$$

where $i_{si, rn}$ is the current in the pickup inductor. At steady-state operating conditions, the primary and $n^{th}$ pickup can be represented by a simple model, as shown in Fig. 7.5.

If $L_T = L_{pi}$, $L_{si, rn} = L_{so, rn}$, and LCL circuits on both primary and pickup sides are tuned to the frequency of $\omega_T$, then

$$\omega_T^2 = \frac{1}{L_T C_T} = \frac{1}{L_{pi} C_T} = \frac{1}{L_{si, rn} C_{si, rn}} = \frac{1}{L_{so, rn} C_{si, rn}}. \quad (7.8)$$

Under these conditions, it can easily be shown that the track current is given by [150]

$$i_T = -j \frac{v_{pi}}{\omega_T L_T}. \quad (7.9)$$
It is evident from (7.9) that input voltage, \( v_{\pi i} \), of the resonant circuit controls the track current, where the magnitude of the voltage is controlled by the turn-on times of the switches in the two legs of the H-bridge. Switches \( S_{p1} \) and \( S_{p2} \), and \( S_{p3} \) and \( S_{p4} \), as shown in Fig. 7.3, are operated complementary to one another to prevent shoot through. All of the switches have a duty ratio of 0.5 and the switches in each leg are turned on with a relative phase delay, \( \theta_{\text{delay}} \). The waveform of \( v_{\pi i} \) for a lagging phase delay \( \theta_{\text{delay}} \) is shown in Fig. 7.6. The output voltage of the primary converter is zero for a phase shift of 0° and is maximum for a phase shift of 180°.

![Figure 7.6: Waveforms of gate signals and output voltage of the primary converter.](image)

The fundamental RMS component of the \( v_{\pi i} \) can be obtained using the Fourier series, and is given by [129]

\[
v_{\pi i,1} = \frac{4}{\pi \sqrt{2}} V_{\text{in}} \sin \left( \frac{\theta_{\text{delay}}}{2} \right). \tag{7.10}
\]

Substituting (7.10) into (7.9) and fundamental component of the track current can be related to the \( \theta_{\text{delay}} \) as follows:

\[
i_{T,1} = -j \frac{4V_{\text{in}}}{\pi \sqrt{2} \omega_{\text{T}} L_{\text{T}}} \sin \left( \frac{\theta_{\text{delay}}}{2} \right). \tag{7.11}
\]

Fundamental component of the secondary side output current is given by [150]

\[
i_{so,1} = -j \frac{M_{\text{rn}} v_{\pi i,1}}{L_{so,\text{rn}} \omega_{\text{T}} L_{\text{T}}} \tag{7.12}
\]

If the equivalent AC voltage of the H-bridge converter of the \( n^{\text{th}} \) pickup system is given by \( v_{so,1} \angle -\theta_{\text{diff},1} \), then the real power output, \( P_{\text{rn}} \), or the power exchanged between the pickup and the primary sides at the fundamental frequency of the track current is expressed as

\[
P_{\text{rn}} = \text{Re} \{ v_{so,1}(-i_{so,1})^* \}. \tag{7.13}
\]
Substituting (7.12) into (7.13) and simplifying gives

\[ P_{rn} = -M_{rn} v_{pi,1} |v_{so, rn, 1}| \sin(\theta_{\text{diff}, rn, 1}) \frac{\omega L_{si, rn} L_T}{\omega L_{si, rn} L_T} \] (7.14)

where the angle \( \theta_{\text{diff}, rn, 1} \in \{90^\circ, -90^\circ, 180^\circ\} \) is the phase difference between the pickup voltage, \( v_{so, rn, 1} \), and primary voltage, \( v_{pi,1} \). For a given \( v_{so, rn, 1} \) and \( v_{pi,1} \), the angle \( \theta_{\text{diff}, rn, 1} \) can be varied to control both the magnitude and direction of the power transfer. However, a value of \( \theta_{\text{diff}, rn, 1} \) other than integer multiples of \( \pm 90^\circ \) results in increased VAr requirements on the primary side. Therefore, the angle \( \theta_{\text{diff}, rn, 1} \) is used only to change the direction of power transfer and its value is limited to the aforementioned set of values.

The pickup controller operates with a phase-shifted modulation technique and produces a voltage \( v_{so, rn, 1} \) that either leads or lags by \( 90^\circ \) relative to \( v_{pi,1} \). Here, \( \theta_{\text{diff}, rn, 1} \) of \( 90^\circ \) means that the pickup receives power or the module capacitor charges, and conversely the module capacitor discharges for a \( \theta_{\text{diff}, rn, 1} \) of \( -90^\circ \). To visualise this concept, consider an IPT system with a primary and two pickups: pickup-1 and pickup-2. The output voltage of pickup-1 is phase delayed by \( 90^\circ \) with respect to the primary voltage; therefore, pickup-1 receives power from the primary, shown in Fig. 7.7. In contrast, pickup-2 gives power as its phase is leading the primary voltage by \( 90^\circ \). The amount of power exchanged between the two sides is controlled by the magnitude of the pickup voltage, \( v_{so, rn, 1} \). The magnitude is controlled by the switching instants of the two legs of the H-bridge converter, where the operating principle of the converter is similar to that of the primary converter as detailed in Section 7.5.1.1.

![Figure 7.7: Output voltage of primary, pickup-1 and pickup-2 converters.](image)
7.5 Control Scheme

The control scheme of the proposed topology is split into two concurrent blocks, Block-1 and Block-2, as shown in Fig. 7.8. Block-1 employs an IPT controller to regulate the track current and to maintain the capacitor voltages within their bounds. For a small bound width, the capacitor voltage variations have negligible effect on the output voltage, $v_r$, of the converter. Therefore, each module can be regarded as a near ideal voltage source, thus simplifying the control scheme for the modules. Consequently, the M2LC controller, which is a part of Block-2, has a single objective of controlling the load currents.

![Decoupled control of capacitor voltages and load currents.](image)

Figure 7.8: Decoupled control of capacitor voltages and load currents.

7.5.1 IPT Controller

The IPT system has two sides, primary and pickup, and each side needs its own controller. The control philosophy of the primary and pickup controllers is presented in the following sections.

7.5.1.1 Primary Controller

The power that can be received by each of the pickups is a function of the track current. Therefore, the magnitude of the track current is maintained constant to minimise the effect of current variations on the output power. As shown in Fig. 7.9, a Proportional-Integral (PI) compensator is used to evaluate $\theta_{\text{delay}}$, where the error between the RMS
track current and a reference value are the inputs to the compensator. A triangle wave generator generates the angle \( \theta \in [0, 180^\circ] \) at a frequency of 20 kHz, and the sine of the angle is used to determine the positive and negative halves of the voltage waveform. The top switch \( S_{\text{p}1} \) of the left-leg is turned on for half the period and then turned off. The switches in the right-leg, \( S_{\text{p}3} \) and \( S_{\text{p}4} \), are switched relative to the left-leg such that the current is maintained at its nominal value. Switches \( S_{\text{p}1} \) and \( S_{\text{p}2} \), and \( S_{\text{p}3} \) and \( S_{\text{p}4} \) are operated complementary to one another to prevent shoot through. The PI compensator, which has a pole (i.e. infinite gain) at zero frequency, is suitable for controlling the RMS track current. Nonetheless, the PI compensator can be replaced with a Proportional-Resonant (PR) compensator if the instantaneous value of the track current is used in the controller feedback.

\[
\begin{align*}
\text{Triangle wave generator} & \quad \rightarrow \quad \text{Sine} \\
| & \quad \rightarrow \quad \text{ON, if } \geq 0 \\
& \quad \rightarrow \quad \text{OFF, otherwise} \\
\end{align*}
\]

Figure 7.9: Primary controller.

### 7.5.1.2 Pickup Controller

In order to maintain the capacitor voltage within the bounds, the pickup converter can be operated in three modes, to charge, to discharge or to bypass the module capacitor. During the charging mode, a module capacitor receives power from the primary side, whereas the capacitor gives power to the primary during the discharging mode. In the case of a bypassed capacitor, the IPT system does not exchange power with the capacitor and the capacitor voltage is primarily governed by the arm current, \( i_{rq}, r \in \{a, b, c\}, q \in \{T, B\} \).

With the proposed control scheme, two symmetrical bounds — outer, \( \delta_{oB} \), and inner, \( \delta_{IB} \), are imposed on the capacitor voltages to keep the voltages within the bounds. Each capacitor gives power to the track when its voltage exceeds the nominal voltage by \( \delta_{oB} \). The capacitor continues to supply power until its voltage is lowered closer to the inner bounds and, at that point, the capacitor is bypassed. Fig. 7.10 shows a hypothetical trajectory of a capacitor voltage with the implemented control scheme. At time instant \( t_1 \) the capacitor voltage violates its bound \( \delta_{oB} \) and, thus, \( \theta_{\text{diff},rn} \) as shown in Fig. 7.7 is
changed to $-90^\circ$ until the voltage reaches $\delta_{iB}$. At time instant $t_2$, the pickup is no longer required to control the voltage ripple and, therefore, the $\theta_{\text{diff,rn}}$ is changed back to $180^\circ$ until $t_3$. Between time instants $t_4$ and $t_5$ the pickup does not exchange power with the track as the capacitor voltage is already within the inner bounds. The capacitor receives power at time instant $t_5$ when its voltage drops below the nominal value by $\delta_{oB}$ and the process is repeated as required.

![Figure 7.10: Controlled voltage trajectory of a module capacitor.](image)

### 7.5.2 M2LC Controller

The proposed topology allows for the control of the load currents to be decoupled from the balancing of the capacitor voltages. The M2LC controller therefore has a single objective of controlling the load currents. State-of-the-art control and modulation schemes such as VOC, OPP and SHE, which achieve a low switching frequency for a given load current distortion, can easily be used for controlling the load currents. A significant amount of literature on the schemes exists [2], [8], [12], [130], [152] and, hence, these schemes are not discussed in the thesis.

### 7.6 Features of the M2LC-IPT

1. **Decoupled Control Schemes**

   From the control perspective, the modified topology has two main advantages. Firstly, a simple control scheme can be used to control the load current. This scheme will focus on meeting the load objectives and providing the best possible performance during the
converter’s steady state and transient operating conditions. Secondly, the switching frequency of the M2LC modules can be significantly reduced without increasing the voltage variations of the module capacitors.

(2) Operation at Low Output Frequency

As explained in Chapter 2, the magnitude of the capacitor voltage variations is inversely proportional to the frequency of the load current. These variations can be minimised by generating high frequency circulating currents, but at the expense of increased RMS arm currents and the complexity of the control scheme. With the proposed topology, the capacitor voltages are balanced by the IPT system and, therefore, the voltages can be maintained within the bounds irrespective of the output frequency of the load current.

(3) Capacitor Charging

In the case of the M2LC topology, each capacitor needs to be charged to a nominal voltage before operating the converter. Typically, an auxiliary power supply or a resistor connected in series with a DC-link supply are used to charge these capacitors. The voltage supply and resistor are bypassed once the capacitors are charged to their nominal voltages. For the M2LC-IPT, the LCL resonant circuit of each pickup behaves like a current source [138], [144], which can easily be used as a controlled current source to charge module capacitors. At startup, each pickup charges its module capacitor, while the primary converter regulates the track current. Once all of the capacitors are charged to their nominal values and the M2LC is operational, the pickup converters return to their regular task of keeping the voltages within their bounds.

(4) Improved Reliability

The reliability of the M2LC improves with the integration of an IPT system, because each pickup is an additional power source to the converter. Therefore, the load current can be controlled without any uncertainty, even without a DC-link power supply. Here, the issues related to the increased number of switches are ignored. The IPT system can also be used as an energy storage system. For such a system, batteries will be integrated with the power supply of the primary converter, allowing the M2LCs to store and release an appropriate amount of energy when needed.
7.7 Simulation Results

The performance of the proposed topology is investigated using PLECS/SIMULINK simulations for the single-phase M2LC-IPT system shown in Fig. 7.11. The feasibility of the M2LC-IPT topology could easily be demonstrated using a three-phase M2LC-IPT, but the single-phase converter was selected so as to compare the performance of the M2LC-IPT topology with that of the M2LC-VCM topology presented in Chapter 6. The circuit parameters of the M2LC system are summarised in Table 6.2 and the parameters of the IPT system are summarised in Table 7.1. The frequency of the M2LC load current and IPT track current was 50 Hz and 20 kHz, respectively. In the simulations, the mutual inductance, $M$, between the pickup and track inductors were assumed to be identical. In a practical system however the mutual inductance between each pickup and the track could be different due to variation in the magnetic coupling. Nonetheless, the primary and pickup controllers would then adjust the phase delay of each pickup to compensate for the variations in the mutual inductance.

![Figure 7.11: Single-phase M2LC-IPT topology.](image)

7.7.1 Load Current Controller

The load current was controlled using a basic open-loop control scheme. With this scheme, a voltage reference for each phase-leg was compared with two Phase-Shifted (PS) carrier waveforms to generate the pulse patterns for the M2LC modules. Because each arm has two modules, the carrier waveforms were phase shifted by $180^\circ$ relative to each other. The
frequency of the carrier waveforms and, therefore, the switching frequency was 600 Hz. The PS PWM strategy is known to create equal duty cycle ratios for each of the switches, because it employs carrier waveforms of the same amplitude and frequency. This strategy has been used in the past to balance capacitor voltages without any active control of the voltages [153]. Therefore, the PS PWM strategy was adopted to balance the capacitor voltages without any additional balancing/sorting algorithm.

The arm current consists of a number of harmonic currents that could affect the balancing of the capacitor voltages [17]. Therefore, the carrier waveforms were rotated every fundamental period in order to minimise the effect of these harmonic currents. With carrier rotation, the duty ratio of the switches is swapped among the modules every fundamental period. Therefore, the rotation process balances the capacitor voltages over two fundamental periods. Since each arm has two modules, two carriers, C-1 and C-2, as shown in Fig. 7.12(a), were needed to generate the pulse patterns for the modules. The waveforms were rotated among the modules such that C-2 and C-1 were swapped at the end of every fundamental period, shown in Fig. 7.12(b). Nonetheless, the capacitor voltages with the M2LC-IPT topology were unaffected by the PS modulation strategy as the IPT system controlled the voltages.

The aforementioned control and modulation strategies were also used to control the conventional M2LC topology, the performance of which was benchmarked against that of the M2LC-IPT topology. Furthermore, the simulated performance of a single-phase M2LC-VCM using the previously mentioned control and modulation strategies is presented to investigate the effectiveness of the M2LC-VCM compared to the M2LC-IPT topology.

### 7.7.2 Performance Evaluation

The conventional, M2LC-VCM and M2LC-IPT topologies were operated at the rated conditions, given in Table 6.2. The simulated waveforms of the load current with these
topologies are shown in Fig. 7.13, with the waveforms showing close agreement. Neither of the M2LC-VCM nor M2LC-IPT topologies affect the output voltage of the converter, as is evident from the unaffected waveforms of the load current when compared against that of the conventional topology.

Hereafter, only the waveforms of the capacitor voltages and the arm currents in phase-leg \( a \) are presented, in order to improve the clarity in the figures. The omitted waveforms of both the arm currents and the capacitor voltages are phase shifted by 180° with respect to those of phase-leg \( a \) and their exclusion does not affect the forthcoming discussion.
The M2LC-VCM reduces the circulating current, and this in turn minimises the capacitor voltage variations, as shown in Fig. 7.14. Although the circulating current is suppressed with the M2LC-VCM, the arm current consists of the fundamental component of the load current. Because of the fundamental component, the voltage variations can only be reduced by a certain amount. With the M2LC-IPT, the capacitor voltages have been maintained within specified bounds, thus validating the feasibility of the control algorithm given in Section 7.5.1.2. With the M2LC-IPT, the outer, $\delta_{oB}$, and inner, $\delta_{iB}$, bound widths were tuned to 1.1 V and 0.2 V, respectively.

![Figure 7.14: Capacitor voltage waveforms in phase-leg $a$.](image1)

The simulated waveforms of the arm currents and the arm current spectra are shown in Figs. 7.15 and 7.16, respectively. With the M2LC-VCM, the second harmonic of the arm currents reduces, because the VCMs compensate for the voltage discrepancy in the phase-leg. In the case of M2LC-IPT, the second harmonic component of the arm currents is reduced due to the reduction in the voltage variations. Considering the arm currents of the conventional topology as the base quantity, a relative reduction of more than 12 % and 9 %

![Figure 7.15: Arm currents in phase-leg $a$.](image2)
can be observed with the M2LC-VCM and M2LC-IPT, respectively. Because circulating currents were not directly controlled with the M2LC-IPT, it is less effective than M2LC-VCM in minimising the circulating currents. Therefore, the RMS arm currents with the M2LC-IPT is slightly higher than that of the M2LC-VCM. Nonetheless, these results clearly show the improvements in performance that the M2LC-IPT topology achieves over conventional topology.

The waveforms of the circulating current are shown in Fig. 7.17, where the circulating current is evaluated by adding the currents in the top and bottom arms of the converter. The current variations are highest with the conventional topology, as it does not have the capability to limit the circulating currents. It is evident from Fig. 7.17 that the M2LC-VCM is the most effective in minimising the circulating currents. Although the control of the circulating current is not a part of the proposed control scheme for the M2LC-IPT, the currents reduce in line with the reduction in the capacitor voltage variations.
7.8 Summary

A modified M2LC topology that incorporates IPT technology has been proposed in order to control the capacitor voltages of the modules within tight bounds. Simulated results of an 800-VA M2LC-IPT have been presented to validate the feasibility of the proposed solution. It has been shown that the M2LC-IPT topology decouples the control of the capacitor voltages and the load currents, and alleviates the shortcomings of the conventional topology. Although the circulating currents have not been directly controlled, they have been shown to reduce in line with the voltage variations. Moreover, a comparison with the M2LC-VCM topology has also been carried out to demonstrate the improvements in performance with the M2LC-IPT topology. Investigations reveal that the M2LC-IPT achieves the best control of the capacitor voltages. However, even though the capacitor voltage variations have been controlled within tight bounds, the proposed M2LC-IPT topology is less effective than the M2LC-VCM in minimising the circulating currents.
Chapter 8

Conclusions

This chapter includes concluding remarks, a list of contributions to the field of Modular Multilevel Converters (M2LCs) arising from this thesis, and a discussion on possible directions for future research.

8.1 Conclusions

Renewable energy generation systems, such as solar, wind and fuel cells, require power converters to transfer electrical power to the existing power networks. To date several converter topologies have been developed to transfer power with high efficiency and reliability, as detailed in Chapter 1. The neutral-point clamped, capacitor clamped and cascaded H-bridge topologies have been used for medium to high-voltage applications, but the M2LC is becoming a popular alternative. A detailed review of the M2LC topology was given in Chapter 2. With this topology, identical modules, which are connected in series, were controlled to synthesise a multilevel voltage waveform. Circulating currents, which are an inherent feature of the topology, were related to the arm currents and capacitor voltages. An overview of the control and modulation strategies for the M2LC was given, and issues relevant to these strategies were explained.

With the M2LC topology, the quality of the output voltage waveform can be improved by increasing the number of modules, but at the expense of increased complexity of the control scheme. The need to control the load currents, capacitor voltages and circulating currents further complicates the scheme. The control of the capacitor voltages and circulating currents is an ongoing area of research. The aim of the thesis was to reduce the capacitor voltage variations and circulating currents, while simplifying the control scheme. Therefore, a number of solutions were proposed, as summarised below.

The M2LC, which is a Multi-Input Multi-Output (MIMO) system, was typically controlled by cascaded control schemes, which require at least two control loops: one to
control the load currents and another to control the circulating currents. Model Predictive Direct Current Control (MPDCC) scheme is convenient for MIMO systems, because it replaces cascaded loops with a single loop to control the system. Chapter 3 presented the concept of MPDCC for M2LCs. The control problem was formulated. A state-space model of the M2LC was derived to predict the behaviour of capacitor voltages and arm currents and, as a result, circulating- and load-currents. Symmetrical bounds were imposed around the load current references to keep the currents within the bounds and to yield long prediction horizons. A mathematical function of the current THD was derived to demonstrate that the THD is a linear function of the current bound width. Moreover, it was shown mathematically that THD reduces with the bound width at the expense of increased switching transitions.

In Chapter 4, the performance of the MPDCC scheme was evaluated. Simulations were carried out to measure the THD of the load current, switching frequency, circulating currents and degree of capacitor voltage variations. These measurements were benchmarked against the Voltage-Oriented Control (VOC) scheme, which is a popular control scheme for grid connected multilevel converters. For a given switching frequency, the THD of the load current with the proposed MPDCC scheme was lower than that with the VOC scheme. The MPDCC outperformed the VOC scheme during transient operating conditions as it achieved a very fast current response without any overshoot in the load currents. The improvements with the MPDCC scheme were verified through experimental results carried out on an 860-VA M2LC prototype. Implementation aspects for the MPDCC scheme, such as delay compensation and algorithm simplification for a DSC were discussed. It was demonstrated with experimental results that the bounds of the load current determine the THD of the current and that the THD was a linear function of the bound width. It was also observed that the proposed MPDCC scheme is computationally expensive and is therefore appropriate for M2LCs with a low number of modules.

Chapter 5 presented a modified M2LC topology that employs Voltage Correcting Modules (VCMs) to both minimise circulating currents and simplify the control scheme. A full-bridge module, which was referred to as VCM, was added to each arm of the converter to compensate for the voltage difference in the phase-leg, thus minimising the circulating currents. Two control schemes that decouple the control of the load and circulating currents were also proposed. A detailed model of the modified topology (M2LC-VCM) was derived to predict the behaviour of the capacitor voltages and circulating currents. A lumped model, which represented each arm with a single module, was then derived to simplify the model of the converter.

The performance of the M2LC-VCM topology was evaluated in Chapter 6. The concept of decoupled control was demonstrated using simulations of a three-phase converter,
where the circulating and load currents were controlled by VCMs and half-bridge modules, respectively. Performance of the VCMs was assessed with both the independent phase-leg and synchronous controllers, which were implemented in the $abc$ and $dq$ reference frames, respectively. Since the synchronous controller employed a proportional-integral compensator, its performance was better than the independent phase-leg controller, which employed a proportional compensator. A comparative investigation with respect to a conventional topology revealed that the M2LC-VCM offers superior performance. Theoretical as well as experimental results for a single-phase three-level 800-VA prototype converter were presented with a detailed discussion, demonstrating the viability of both the proposed mathematical models and the modified topology. It was shown with experimental results that the M2LC-VCM reduces the circulating currents, even with a lower switching frequency for the half-bridge modules. Moreover, models have been used to investigate the effect of circuit parameters on the circulating currents and to demonstrate improvement in performance associated with the VCM.

In Chapter 7, Inductive Power Transfer (IPT) technology was integrated with the M2LC to keep the capacitor voltages within bounds. All of the modules were magnetically coupled to the IPT track, which allowed modules to exchange power without any physical contacts. The operating principles of the M2LC with IPT (M2LC-IPT) and control scheme for controlling the voltage variations were discussed. M2LC-IPT allowed for a decoupled control of capacitor voltages and load currents. The feasibility of the M2LC-IPT topology was demonstrated through simulation of a 800-VA converter. The performance with the M2LC-IPT was benchmarked against both the conventional and M2LC-VCM topologies. The M2LC-IPT offered an appropriate control of capacitor voltages. However, M2LC-IPT was unable to completely suppress the circulating currents, because control of these currents was not a part of the proposed control scheme.

8.2 Contributions

The main contributions of this thesis are listed below:

- An MPDCC scheme for M2LCs has been proposed as a viable alternative to the typical cascaded control schemes for minimising circulating currents and capacitor voltage variations. The MPDCC is also able to control the load currents within prescribed bounds. Dynamic state-space model of the M2LC has been developed to predict the behaviour of both the capacitor voltages and arm currents.

- A modified M2LC topology with VCMs has been proposed to minimise both the circulating currents and capacitor voltage variations. The proposed topology allows
for a decoupled control of the load and circulating currents. Two control schemes for the topology have been developed to minimise the circulating currents. Detailed and lumped models have also been developed to predict the behaviour of the proposed topology.

- A modified M2LC topology with IPT technology has been proposed to both decouple and simplify the control of the capacitor voltages and load currents. A decoupled controller has been developed to maintain capacitor voltage variations within prescribed bounds.

The above outlined work has been published in two journals and five conference proceedings, which are listed below:


8.3 Future Work

This thesis has proposed MPDCC, M2LC-VCM and M2LC-IPT as solutions to minimise both the circulating currents and voltage variations. The feasibility of the solutions has been demonstrated using an M2LC connected to a balanced AC grid. The next area of research therefore could involve the investigation and improvement of these methods for an M2LC connected to an unbalanced AC grid.

As presented in Chapters 3 and 4, MPDCC is computationally expensive, because the behaviour of the converter is predicted for all the switching combinations. Therefore, the presented concept is appropriate for M2LCs with a low number of modules. For an M2LC with a large number of modules, MPDCC could be modified to limit the number of switching transitions in the cost function, for example a maximum number of three transitions. Then, the algorithm will be computed only for the switching combinations with transition counts less than three, thus reducing the computational burden. This approach could raise a minor concern that the control solution is suboptimal. However, the effects of the reduced combinations are expected to be minor, because of the receding horizon policy.

The M2LC-VCM concept, which is presented in Chapters 5 and 6, has been employed to reduce both the circulating currents and capacitor voltage variations. Because the concept allows for the decoupled control of the load and circulating currents, a simple control scheme can easily be used to control the M2LC. The circulating currents are a function of the module switching functions and the circuit parameters. The voltage discrepancy and, therefore, circulating currents in a phase-leg could increase with an improper choice of switching function. Consequently, the voltage across the VCM capacitor has to increase so as to minimise the voltage discrepancy. Future research could investigate methods to reduce voltage discrepancy in a phase-leg so that VCMs have to compensate only for the small discrepancy. Future research could also investigate methods to achieve the minimum possible switching frequency using a simple control scheme. Such methods would greatly improve the performance of the converter and facilitate widespread adoption of the M2LC-VCM topology.

Another area of research could be to model the M2LC-IPT, which is presented in Chapter 7, so as to optimise both the design and control of the converter. Model Predictive Control (MPC) could also be used to control each pickup and to make decisions on whether to connect or bypass capacitors. An MPC algorithm is expected to be more complex than the capacitor voltage ripple controller that has been presented, but it would offer superior performance by reducing the switching frequency of each pickup. The computational burden would not significantly increase as long as the control problem is formulated individually for each pickup.
Appendix A

Matrices and Vectors of the M2LC Model

A.1 System Matrices of the First Model

\[ T = \begin{bmatrix}
L & L & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & L & L & 0 & 0 & 0 \\
-2L & -L & -L & -L & 2L & 0 & 0 \\
-2L & -2L & -2L & -2L & 2L & L & L \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix} \]  
(A.1)

\[ F_1 = \begin{bmatrix}
-R & -R & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -R & -R & 0 & 0 & 0 \\
R & R & R & R & -2R & 0 & 0 \\
R_1 & -R - R_1 & -R_1 & R + R_1 & 0 & \frac{3}{2} & -\frac{\sqrt{3}}{2} \\
-2R_1 & 2(R + R_1) & -R_1 & R + R_1 & -R & -\frac{3}{2} & -\frac{\sqrt{3}}{2} \\
0 & 0 & 0 & 0 & 0 & 0 & -\omega \\
0 & 0 & 0 & 0 & 0 & 0 & \omega \\
\end{bmatrix} \]  
(A.2)
\[ G_i = \begin{bmatrix} V_{aT} & V_{aB} & 0 & 0 & 0 & 0 \\ 0 & 0 & V_{bT} & V_{bB} & 0 & 0 \\ 0 & 0 & 0 & 0 & V_{cT} & V_{cB} \\ 0 & V_{aB} & 0 & -V_{bB} & 0 & 0 \\ 0 & -V_{aB} & 0 & 0 & 0 & V_{cB} \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (A.3) \]

\[ V_{rT} = [-v_{c,r1}, -v_{c,r2}, \ldots, -v_{c,rN}] \quad (A.4) \]

\[ V_{rB} = [-v_{c,r(N+1)}, -v_{c,r(N+2)}, \ldots, -v_{c,r2N}] \quad (A.5) \]

\[ V_{DC} = [V_{DC} V_{DC} V_{DC} 0 0 0 0]^\top \quad (A.6) \]

and \( \mathbf{0} \) is a zero vector of length \( N \). The parameters used in the above equations are the inductance and resistance of both the load and arm, \( L_l, L, R_l \) and \( R \), respectively.

### A.2 System Matrices of the Second Model

\[ F_c = -\frac{1}{CR_{\text{cap}}} I_{6N} \quad (A.7) \]

\[ G_c = \frac{1}{C} \text{diag}(i_{aT}I_N, i_{aB}I_N, i_{bT}I_N, i_{bB}I_N, i_{cT}I_N, i_{cB}I_N) \quad (A.8) \]

Here, \( I_{6N} \) and \( I_N \) are \( 6N \times 6N \) and \( N \times N \) identity matrices, respectively. \( R_{\text{cap}} \) is used to model the losses associated with the module capacitors. Moreover, \( \text{diag}(\cdots) \) is a square diagonal matrix with entries inside the brackets at its main diagonal \([ \ \ ]\).

### A.3 Discrete-time Matrices of the Models

\[ A_i = e^{T^{-1}F_i T} \quad (A.9) \]

\[ B_i = F_i^{-1}T(A_i - I_f)T^{-1}G_i \quad (A.10) \]

\[ V_i = F_i^{-1}T(A_i - I_f)T^{-1}V_{DC} \quad (A.11) \]
A.3 Discrete-time Matrices of the Models

\[ C_i = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ -1 & 1 & -1 & 1 & 0 & 0 \\ \frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{2} & \frac{1}{2} & 0 & 0 \\ -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & 1 & 0 \end{bmatrix} \]  

(A.12)

\[ A_c = e^{F_c T_s} \]  

(A.13)

\[ B_c = F_c^{-1}(A_c - I_{6N})G_c \]  

(A.14)

\[ C_c = I_{6N} \]  

(A.15)

Here, \( I_7 \) and \( I_{6N} \) are 7 \( \times \) 7 and 6N \( \times \) 6N identity matrices, respectively and \( T_s \) is the sampling interval.
Appendix B

Matrices and Vectors of the M2LC-VCM Models

B.1 Matrices and Vectors of the Detailed Model

\[ A_d = \begin{bmatrix} T_1 & 0_{7 \times 6N} & 0_{7 \times 6} \\ 0_{6N \times 7} & I_{6N} & 0_{6N \times 6} \\ 0_{6 \times 7} & 0_{6 \times 6N} & I_6 \end{bmatrix}^{-1} \begin{bmatrix} F_1 & 0_{7 \times 6N} & 0_{7 \times 6} \\ 0_{6N \times 7} & F_2 & 0_{6N \times 6} \\ 0_{6 \times 7} & 0_{6 \times 6N} & F_3 \end{bmatrix} \]  
(B.1)

\[ B_d = \begin{bmatrix} T_1 & 0_{7 \times 6N} & 0_{7 \times 6} \\ 0_{6N \times 7} & I_{6N} & 0_{6N \times 6} \\ 0_{6 \times 7} & 0_{6 \times 6N} & I_6 \end{bmatrix}^{-1} \begin{bmatrix} G_{1}(x) & G_2(x) \\ G_3(x) & 0_{6N \times 6} \\ 0_{6 \times 6N} & G_4(x) \end{bmatrix} \]  
(B.2)

\[ V_d = \begin{bmatrix} T_1 & 0_{7 \times 6N} & 0_{7 \times 6} \\ 0_{6N \times 7} & I_{6N} & 0_{6N \times 6} \\ 0_{6 \times 7} & 0_{6 \times 6N} & I_6 \end{bmatrix}^{-1} \begin{bmatrix} V_{DC} \\ V_{DC} \\ V_{DC} \\ 0_{6N+10}^{T} \end{bmatrix} \]  
(B.3)

\[ T_1 = \begin{bmatrix} L & L & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & L & L & 0 & 0 & 0 \\ -L & -L & -L & -L & 2L & 0 & 0 \\ -L_1 & L + L_1 & L_1 & -L - L_1 & 0 & 0 & 0 \\ 2L_1 & -2L - 2L_1 & L_1 & -L - L_1 & L & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \]  
(B.4)
\( F_1 = \begin{bmatrix} -R & -R & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -R & -R & 0 & 0 & 0 \\ R & R & R & R & -2R & 0 & 0 \\ R_l & -R - R_l & -R_l & R + R_l & 0 & \frac{3}{2} - \frac{\sqrt{3}}{2} & \frac{3}{2} - \frac{\sqrt{3}}{2} \\ -2R_l & 2(R + R_l) & -R_l & R + R_l & -R & \frac{3}{2} - \frac{\sqrt{3}}{2} & \frac{3}{2} - \frac{\sqrt{3}}{2} \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega \\ 0 & 0 & 0 & 0 & 0 & 0 & \omega & 0 \end{bmatrix} \) (B.5)

\( F_2 = -\frac{1}{CR_{cap}} I_{6N} \) (B.6)

\( F_3 = -\frac{1}{C_{vcm} R_{vcm}} I_6 \) (B.7)

\( G_1 = \begin{bmatrix} V_{aT} & V_{aB} & 0_N & 0_N & 0_N & 0_N \\ 0_N & 0_N & V_{bT} & V_{bB} & 0_N & 0_N \\ 0_N & 0_N & 0_N & 0_N & V_{cT} & V_{cB} \\ 0_N & V_{aB} & 0_N & -V_{bB} & 0_N & 0_N \\ 0_N & -V_{aB} & 0_N & 0_N & 0_N & V_{cB} \\ 0_N & 0_N & 0_N & 0_N & 0_N & 0_N \end{bmatrix} \) (B.8)

\( V_{rT} = [ -v_{c,r1} \ -v_{c,r2} \ldots \ -v_{c,rN} ] \) (B.9)

\( V_{rB} = [ -v_{c,r(N+1)} \ -v_{c,r(N+2)} \ldots \ -v_{c,r2N} ] \) (B.10)

\( G_2 = \begin{bmatrix} -v_{vcm,aT} & -v_{vcm,aB} & 0 & 0 & 0 & 0 \\ 0 & 0 & -v_{vcm,bT} & -v_{vcm,bB} & 0 & 0 \\ 0 & 0 & 0 & 0 & -v_{vcm,cT} & -v_{vcm,cB} \\ 0 & -v_{vcm,aB} & 0 & v_{vcm,bB} & 0 & 0 \\ 0 & v_{vcm,aB} & 0 & 0 & 0 & -v_{vcm,cB} \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \) (B.11)

\( G_3 = \frac{1}{C} \text{diag}(i_{aT} I_N, i_{aB} I_N, i_{bT} I_N, i_{bB} I_N, i_{cT} I_N, i_{cB} I_N) \) (B.12)

\( G_4 = \frac{1}{C_{vcm}} \text{diag}(i_{aT}, i_{aB}, i_{bT}, i_{bB}, i_{cT}, i_{cB}) \) (B.13)
\[ C_d = \begin{bmatrix} C_1 & 0_{7\times 6N} & 0_{7\times 6} \\
0_{6N\times 7} & I_{6N} & 0_{6N\times 6} \\
0_{6\times 7} & 0_{6\times 6N} & I_6 \end{bmatrix} \]  
(B.14)

\[ C_1 = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & -1 & 0 & 0 \\
-1 & 1 & -1 & 1 & 0 & 0 \\
\frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{2} & \frac{1}{2} & 0 & 0 \\
-\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & 1 & 0 & 0 \end{bmatrix} \]  
(B.15)

where, \(0_y\) is a zero vector of length \(y\), \(0_{p\times q}\) is a \(p\times q\) zero matrix, and \(I_{6N}\) and \(I_N\) are \(6N \times 6N\) and \(N \times N\) identity matrices, respectively. The parameters used in the above equations are the inductance and resistance of both the load and arm, \(L_l\), \(L\), \(R_l\) and \(R\), respectively. Moreover, \(\text{diag}(\cdots)\) is a square diagonal matrix with entries inside the brackets at its main diagonal \([\ \ \ ]\).

**B.2 Matrices and Vectors of the Lumped Model**

\[ A_\xi = \begin{bmatrix} T_2 & 0_{7\times 6} & 0_{7\times 6} \\
0_{6\times 7} & I_6 & 0_{6\times 6} \\
0_{6\times 7} & 0_{6\times 6} & I_6 \end{bmatrix}^{-1} \begin{bmatrix} F_4 & 0_{7\times 6} & 0_{7\times 6} \\
0_{6\times 7} & F_5 & 0_{6\times 6} \\
0_{6\times 7} & 0_{6\times 6} & F_6 \end{bmatrix} \]  
(B.16)

\[ B_\xi = \begin{bmatrix} T_2 & 0_{7\times 6} & 0_{7\times 6} \\
0_{6\times 7} & I_6 & 0_{6\times 6} \\
0_{6\times 7} & 0_{6\times 6} & I_6 \end{bmatrix}^{-1} \begin{bmatrix} G_5(\mathbf{x}) & G_6(\mathbf{x}) \\
G_7(\mathbf{x}) & 0_{6\times 6} \\
0_{6\times 6} & G_8(\mathbf{x}) \end{bmatrix} \]  
(B.17)

\[ V_\xi = \begin{bmatrix} T_2 & 0_{7\times 6} & 0_{7\times 6} \\
0_{6\times 7} & I_6 & 0_{6\times 6} \\
0_{6\times 7} & 0_{6\times 6} & I_6 \end{bmatrix}^{-1} \begin{bmatrix} V_{\text{DC}} & V_{\text{DC}} & V_{\text{DC}} & 0_{16} \end{bmatrix}^T \]  
(B.18)
Appendix B. Matrices and Vectors of the M2LC-VCM Models

\[
T_2 = \begin{bmatrix}
L & L & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & L & L & 0 & 0 & 0 \\
-L & -L & -L & -L & 2L & 0 & 0 \\
-L_1 & L + L_1 & L_1 & -L - L_1 & 0 & 0 & 0 \\
2L_1 & -2L - 2L_1 & L_1 & -L - L_1 & L & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 \\
\end{bmatrix}
\] (B.19)

\[
F_4 = \begin{bmatrix}
-R & -R & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -R & -R & 0 & 0 & 0 \\
R & R & R & R & -2R & 0 & 0 \\
-R_1 & -R - R_1 & -R_1 & R + R_1 & 0 & \frac{3}{2} & -\frac{\sqrt{3}}{2} \\
-2R_1 & 2(R + R_1) & -R_1 & R + R_1 & -R & \frac{3}{2} & -\frac{\sqrt{3}}{2} \\
0 & 0 & 0 & 0 & 0 & 0 & -\omega \\
0 & 0 & 0 & 0 & 0 & \omega & 0 \\
\end{bmatrix}
\] (B.20)

\[
F_5 = -\frac{N}{CR_{pm}}I_6
\] (B.21)

\[
F_6 = -\frac{1}{C_{vcm}R_{vcm}}I_6
\] (B.22)

\[
G_5 = \begin{bmatrix}
-\tau_{pm,aT} & -\tau_{pm,aB} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -\tau_{pm,bT} & -\tau_{pm,bB} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \tau_{pm,eT} & \tau_{pm,eB} & 0 \\
0 & -\tau_{pm,aB} & 0 & \tau_{pm,bB} & 0 & 0 & 0 \\
0 & \tau_{pm,aB} & 0 & 0 & \tau_{pm,eB} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
\end{bmatrix}
\] (B.23)

\[
G_6 = \begin{bmatrix}
-\tau_{vcm,aT} & -\tau_{vcm,aB} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \tau_{vcm,bT} & -\tau_{vcm,bB} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \tau_{vcm,eT} & -\tau_{vcm,eB} & 0 \\
0 & -\tau_{vcm,aB} & 0 & \tau_{vcm,bB} & 0 & 0 & 0 \\
0 & \tau_{vcm,aB} & 0 & \tau_{vcm,bB} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \tau_{vcm,eB} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \tau_{vcm,eB} & 0 \\
\end{bmatrix}
\] (B.24)
\[ G_7 = \frac{N}{C} \text{diag}(i_{aT}, i_{aB}, i_{bT}, i_{bB}, i_{cT}, i_{cB}) \]  
(B.25)

\[ G_8 = \frac{1}{C_{vcm}} \text{diag}(i_{aT}, i_{aB}, i_{bT}, i_{bB}, i_{cT}, i_{cB}) \]  
(B.26)

\[ C_\xi = \begin{bmatrix} C_2 & 0_{7 \times 6} & 0_{7 \times 6} \\ 0_{6 \times 7} & I_6 & 0_{6 \times 6} \\ 0_{6 \times 7} & 0_{6 \times 6} & I_6 \end{bmatrix} \]  
(B.27)

\[ C_2 = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ -1 & 1 & -1 & 1 & 0 & 0 & 0 \\ \frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 \\ -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & 1 & 0 & 0 \end{bmatrix} \]  
(B.28)

where \( 0_{p \times q} \) is a \( p \times q \) zero matrix, and \( I_6 \) is \( 6 \times 6 \) identity matrix.
Bibliography


