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Miniaturising Wireless Power Supplies for Active Implantable Devices

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Supervised by: Dr Daniel McCormick and Associate Professor David Budgett

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Abstract

Active implantable devices have had a large impact on a range of medical conditions. However, their use has remained limited to a small niche of applications. A challenge limiting their prevalence is miniaturising the device to an unobtrusive and implantable size. Active implants could greatly improve the treatment of medical conditions such as Hydrocephalus. This condition occurs when excess fluid is produced within the brain and leads to increased intracranial pressure. An implantable pressure monitor combined with an active pump or valve would be a large improvement over the current treatment as it could evaluate the pressure within the skull and control fluid volume within the brain. Due to the space constraints and power requirements of this application, batteries alone were not a viable method for powering the implant. Consequently, a wireless power supply solution has been proposed. This thesis covers the development of a miniaturised integrated circuit for the implant’s rectification and power flow control features.

Evaluation of secondary pickup topologies resulted in the parallel topology being chosen as it gave practical coil designs with a low number of turns for the required output powers and load impedances. Multiple rectifier topologies were investigated, and an active diode synchronous rectifier was found to be the most efficient option. Shorting control was used for over-voltage protection and power flow control. In combination with a parallel tuned pickup, shorting control resulted in increased efficiency with increased coupling and greater power transfer with decreased coupling. Furthermore, shorting control could effectively protect the circuitry from large couplings without dissipating excessive power.

An integrated circuit 1.29mm by 2.12mm including an active diode synchronous rectifier and shorting control was designed and fabricated. The rectifier had an efficiency greater than 85% from 30mW to 600mW. The wireless power management integrated circuit was included in a prototype biopotential telemeter with similar power requirements to a hydrocephalus monitor. A micropump was included and powered from the integrated circuit.

This research has demonstrated an efficient wireless power transfer system that is robust to variations in coupling, extremely small in size and capable of supplying the required power for a smart shunt.
Acknowledgement

First and foremost, I have to thank Dr Daniel McCormick who initially approached me about the PhD position. He has provided me with the trust and independence to carry out my research freely while offering advice when needed. His guidance and humour have always been appreciated throughout my study.

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# Table of Contents

Abstract .......................................................................................................................... i
Acknowledgement .......................................................................................................... ii
Table of Contents ........................................................................................................... iii
Glossary ........................................................................................................................... viii
List of Figures .................................................................................................................. xi
List of Tables .................................................................................................................. xvii

Chapter 1  Introduction ................................................................................................ 1
  1.1. Active Implantable devices .................................................................................. 1
  1.2. Hydrocephalus ..................................................................................................... 1
    1.2.1. Cause and Symptoms of Hydrocephalus ...................................................... 2
    1.2.2. Treatment ..................................................................................................... 3
    1.2.3. Shunt Complications .................................................................................... 3
  1.3. Monitoring ............................................................................................................ 4
  1.4. The Cost of Hydrocephalus ................................................................................ 5
    1.4.1. Direct Cost ................................................................................................... 5
    1.4.2. Social Cost .................................................................................................. 5
  1.5. A Smart Shunt for Hydrocephalus ..................................................................... 5
    1.5.1. Components of a Smart Shunt .................................................................... 6
    1.5.2. Size Constraints ......................................................................................... 8
    1.5.3. Power Requirements .................................................................................. 9
    1.5.4. Appropriate Methods for Lifetime Power .................................................. 10
  1.6. Previous Research into Wireless Power for Implantable Devices ..................... 12
  1.7. Objective and Scope ........................................................................................... 14

Chapter 2  Structure of the Power Link ....................................................................... 16
  2.1. Inductive Power Transfer Fundamentals ............................................................. 17
    2.1.1. Secondary Resonance ............................................................................... 18
2.1.2. Single-Turn Equivalent Values
2.2. Series and Parallel Pickup Properties
2.2.1. Secondary Gain
2.2.2. Loaded Parallel Coil Resonance
2.2.3. Series vs. Parallel Pickup
2.3. Parallel Pickup Losses and Efficiency
2.4. Rectifier Topologies
2.4.1. Diodes and Switches
2.4.2. Half Wave Rectifier
2.4.3. Full Wave Bridge Rectifier
2.5. Active Diode Synchronous Rectifier
2.5.1. Operation and Load Power
2.5.2. Losses
2.5.3. Efficiency
2.5.4. Current Spikes and Reduction Techniques
2.6. Voltage and Power Flow Control Strategies
2.6.1. Primary Based Power Control
2.6.2. Secondary Based Power Control
2.7. Shorting Control
2.7.1. Shorting Control for Over-voltage protection
2.7.2. Power Losses During Shorting Control
2.7.3. Shorting Control for Improved Secondary Pickup Efficiency
2.7.4. Shorting Control vs Detune Control
2.8. Discrete Implementation vs. Integrated Implementation
2.9. Summary
Chapter 3 Integrated Circuit Design
3.1. Notation Conventions for this Chapter
3.9.  Shorting Controller ........................................................................................................... 96
  3.9.1.  Design ......................................................................................................................... 96
  3.9.2.  Simulations ................................................................................................................ 98
3.10. Voltage and Current Reference ....................................................................................... 100
  3.10.1.  Required Accuracy of the Voltage and Current Reference ...................................... 100
  3.10.2.  Design of the Voltage and Current Reference .......................................................... 102
  3.10.3.  Simulated Performance .............................................................................................. 105
  3.10.4.  Layout ....................................................................................................................... 106
3.11. Start-up Circuit ................................................................................................................ 108
  3.11.1.  Simulations ................................................................................................................ 109
3.12. ADSR Design, Simulation and Layout ............................................................................. 110
  3.12.1.  Design ........................................................................................................................ 110
  3.12.2.  Layout ........................................................................................................................ 113
  3.12.3.  Simulation .................................................................................................................. 115
3.13. Summary ........................................................................................................................ 119
Chapter 4  Measuring the Integrated Circuit Rectifier and Power Link Performance .......... 121
  4.1. Wire Bonding .................................................................................................................. 122
  4.2. Sub-Circuit Measurements .............................................................................................. 123
    4.2.1. Body Diodes .............................................................................................................. 124
    4.2.2. Bridge-Driver Measurements .................................................................................... 126
    4.2.3. Voltage Reference .................................................................................................... 127
    4.2.4. Start-up Circuit Measurement Results ...................................................................... 128
  4.3. Measuring the Power Conversion Efficiency .................................................................. 128
    4.3.1. PCE Test Circuit ....................................................................................................... 128
    4.3.2. Quantification of Measurement Error ........................................................................ 135
    4.3.3. Experimental Results ............................................................................................... 137
  4.4. Multiple Triggering ......................................................................................................... 140
4.5. Measuring Secondary Efficiency with Shorting Control ........................................ 142
4.6. Shorting Control Power Loss .................................................................................. 145
4.7. Comparison with Previous Work ............................................................................ 147
4.8. Summary .................................................................................................................. 148

Chapter 5 Powering a Pressure Monitor and Micropump .......................................... 150
5.1. An Example Telemeter for Hydrocephalus Monitoring ........................................... 150
5.1.1. Adding the ADSR .............................................................................................. 152
5.2. Powering a Piezoelectric Micro Pump .................................................................. 153
5.3. Summary ................................................................................................................ 154

Chapter 6 Conclusions and Future Work ................................................................. 155
6.1. General Conclusions ............................................................................................... 155
6.2. Contributions ......................................................................................................... 157
6.3. Publications ............................................................................................................ 158
6.3.1. Journal Papers .................................................................................................... 158
6.3.2. Conference Papers ............................................................................................. 158
6.3.3. Conference Abstracts ......................................................................................... 158
6.4. Suggestions for Future Work ................................................................................ 159

Appendices .................................................................................................................... 161
References ..................................................................................................................... 166
## Glossary

### Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>ADC</td>
<td>Analogue to Digital Converter</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>ESD</td>
<td>Electro Static Discharge</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
</tr>
<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>IPT</td>
<td>Inductively Power Transfer</td>
</tr>
<tr>
<td>LC</td>
<td>Inductor-Capacitor connection</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>NMA</td>
<td>6V NMOS Transistor</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PCE</td>
<td>Power Conversion Efficiency</td>
</tr>
<tr>
<td>PMA</td>
<td>6V PMOS Transistor</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
</tbody>
</table>

### Fundamental Quantities

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>Capacitor</td>
<td>Farads (F)</td>
</tr>
<tr>
<td>E</td>
<td>Energy</td>
<td>Joules (J)</td>
</tr>
<tr>
<td>f</td>
<td>Frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>i</td>
<td>Instantaneous Current / Envelope of Current</td>
<td>Amperes (A)</td>
</tr>
<tr>
<td>I</td>
<td>Current Magnitude</td>
<td>Amperes (A)</td>
</tr>
<tr>
<td>j</td>
<td>Complex Operator</td>
<td>$\sqrt{-1}$</td>
</tr>
<tr>
<td>k</td>
<td>Magnetic Coupling Coefficient</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>Self-Inductance</td>
<td>Henrys (H)</td>
</tr>
<tr>
<td>M</td>
<td>Mutual Inductance</td>
<td>Henrys (H)</td>
</tr>
<tr>
<td>P</td>
<td>Power</td>
<td>Watts (W)</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>Q</td>
<td>Quality Factor</td>
<td></td>
</tr>
<tr>
<td>R</td>
<td>Resistance</td>
<td>Ohms (Ω)</td>
</tr>
<tr>
<td>s</td>
<td>Laplace Variable</td>
<td></td>
</tr>
<tr>
<td>t</td>
<td>Time</td>
<td>Seconds (S)</td>
</tr>
<tr>
<td>V</td>
<td>Voltage</td>
<td>Volts (V)</td>
</tr>
<tr>
<td>Z</td>
<td>Impedance</td>
<td>Ohms (Ω)</td>
</tr>
<tr>
<td>μ</td>
<td>Permeability</td>
<td>H/m</td>
</tr>
<tr>
<td>ω</td>
<td>Angular Frequency</td>
<td>Radians/s</td>
</tr>
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**Secondary (Pickup) Symbols**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>A′</td>
<td>Secondary Gain</td>
<td>V/V</td>
</tr>
<tr>
<td>C₂</td>
<td>Secondary Tuning Capacitance</td>
<td>F</td>
</tr>
<tr>
<td>I₂</td>
<td>Secondary Current</td>
<td>A_{RMS}</td>
</tr>
<tr>
<td>L₂</td>
<td>Secondary Self-inductance</td>
<td>H</td>
</tr>
<tr>
<td>L₂₀</td>
<td>Single-Turn Equivalent Secondary Self-inductance</td>
<td>H</td>
</tr>
<tr>
<td>N₂</td>
<td>Secondary Turns</td>
<td></td>
</tr>
<tr>
<td>Q₂</td>
<td>Secondary Quality factor</td>
<td></td>
</tr>
<tr>
<td>R₂</td>
<td>Secondary Winding Resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>R₂₀</td>
<td>Single-Turn Equivalent Secondary Winding Resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>R_L</td>
<td>Load Resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>V_OC</td>
<td>Open-Circuit Voltage</td>
<td>V_{RMS}</td>
</tr>
<tr>
<td>η₂</td>
<td>Secondary Efficiency</td>
<td></td>
</tr>
</tbody>
</table>

**Integrated Circuit Symbols**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Gain</td>
<td>V/V</td>
</tr>
<tr>
<td>C_{ox}</td>
<td>Gate Oxide Capacitance</td>
<td>fF/um²</td>
</tr>
<tr>
<td>g_m</td>
<td>FET Transconductance</td>
<td>A/V</td>
</tr>
<tr>
<td>I_s</td>
<td>BJT Saturation Current</td>
<td>A</td>
</tr>
<tr>
<td>k'</td>
<td>FET Gain Factor</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>FET Gate Length</td>
<td>μm</td>
</tr>
<tr>
<td>r_0</td>
<td>Small Signal Output Resistance</td>
<td>Ω</td>
</tr>
<tr>
<td>V_{ov}</td>
<td>FET Overdrive Voltage</td>
<td>V</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>--------------------------------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>$V_t$</td>
<td>FET Threshold Voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_T$</td>
<td>Thermal Voltage</td>
<td>V</td>
</tr>
<tr>
<td>$W$</td>
<td>FET Gate Width</td>
<td>μm</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>Channel Length Modulation Parameter</td>
<td>μm/V</td>
</tr>
<tr>
<td>$\mu_n$</td>
<td>Average Electron Mobility</td>
<td>cm²/V.s</td>
</tr>
<tr>
<td>$\mu_p$</td>
<td>Average Hole Mobility</td>
<td>cm²/V.s</td>
</tr>
<tr>
<td>$\sigma$</td>
<td>Standard Deviation</td>
<td></td>
</tr>
</tbody>
</table>
List of Figures

Figure 1.1: CSF circulation within the brain [17].................................................................2
Figure 2.1: Overview of an inductive power transfer system..................................................16
Figure 2.2: Equivalent two port representation of the coupled inductive power link a) with mutual inductance and b) with dependent current sources [68].................................17
Figure 2.3: Capacitive tuning of the pickup into resonance can be achieved with a) series tuning or b) parallel tuning..............................................................18
Figure 2.4: Two coils of equal cross sectional area, geometry and copper area with different numbers of turns [78]..................................................................................19
Figure 2.5: Series and parallel-tuned pickups with loads.........................................................22
Figure 2.6: Test case coil with 9 turns of three parallel wires around a ferromagnetic core...25
Figure 2.7: Number of turns required to maximise power transfer for series and parallel-tuned coils with a Q factor of 14.45 at 614KHz.................................................................25
Figure 2.8: Parallel-tuned pickup.........................................................................................26
Figure 2.9: Load power and winding losses for a parallel pickup matched with a 100Ω load. The voltage $V_{OC}$ is set to 0.49$V_{rms}$.................................................................................27
Figure 2.10: Secondary efficiency against load resistance for a coil tuned to match a 100Ω load.........................................................................................................................28
Figure 2.11: Parallel-tuned pickup with infinite load and zero load........................................28
Figure 2.12: Diode and MOSFET.........................................................................................29
Figure 2.13: Half wave diode rectifier. $V_{FW}$ shown as 0V..................................................30
Figure 2.14: Full wave diode bridge rectifier. $V_{FW}$ shown as 0V........................................31
Figure 2.15: Active diode rectifier circuit diagram and waveform.........................................33
Figure 2.16: Load power and power loss for an active diode synchronous rectifier with zero offset and hysteresis and a voltage source input as a function of $V_{DD}$ and $V_{I-V_{DD}}$................................................33
Figure 2.17: Active diode synchronous rectifier reverse current due to switching delay........35
Figure 2.18: Efficiency for an active diode synchronous rectifier as a function of $V_{DD}$ and $V_{I-V_{DD}}$. The rectifier has zero offset and hysteresis and has a voltage source input. ..........35
Figure 2.19: Active diode synchronous rectifier efficiency with load power and switch resistance. Switching losses decrease the efficiency at low load powers, and resistive losses decrease the efficiency at higher powers.................................................................36
Figure 2.20: Representation of the periodic current from the pickup capacitor, pickup inductor and total current through rectifier with a) normal transistor turn on and b) soft transistor turn on.

Figure 2.21: Effect of changing the pass transistor turn on rise time on efficiency, peak current and load power.

Figure 2.22: Wireless feedback loop of primary and secondary.

Figure 2.23: Output voltage control through power shunting.

Figure 2.24: Detune control. V_{out} is managed by using a detune capacitor to change the pickup resonance frequency and decrease the input power.

Figure 2.25: Detune control for the test case coil matched to a 100Ω load. The detune capacitance is 0nF, 10nF, 100nF and 1µF. Simulations were run with and without 500mΩ switch resistance. The simulations with switch resistance always have a lower peak than without.

Figure 2.26: A parallel-tuned pickup can be modelled as a current source in parallel with the pickup. Shorting control uses a switch to bypass the current through the switch resistance.

Figure 2.27: Pickup, rectifier, load and shorting control model with coil losses.

Figure 2.28: Load power and winding losses for a parallel pickup tuned to a 100Ω load. The voltage V_{OC} is set to 0.49V_{rms}.

Figure 2.29: Normalised power delivered to a resistor in parallel to the pickup for a 100Ω load (solid line) and 10Ω load (dashed line).

Figure 2.30: a) Effective load impedance as input voltage increases but output voltage remains V_{ave}. b) The efficiency of the secondary including and excluding losses during shorting control. The duty cycle of the rectifier is proportional to the effective load.

Figure 3.1: NMOS and PMOS physical structure in a CMOS process.

Figure 3.2: Fingered devices to increase gate width.

Figure 3.3: Hybrid model for small signal analysis of the MOSFET.

Figure 3.4: Small signal drain output resistance with AC grounded gate.

Figure 3.5: Small signal source input resistance of a FET with AC grounded gate.

Figure 3.6: Simple current mirror. The drain current in N_2 mirrors the drain current though N_1.

Figure 3.7: Source coupled pair.

Figure 3.8: (left) Differential amplifier with differential gain -g_mR_L. (right) Differential amplifier with feedback.
Figure 3.9: Integrated circuit design process flow. Each step in the design flow (blue) has a corresponding software tool (dark grey).

Figure 3.10: Poor resistor layout for device mismatch, and good layout using multiple unit devices, common centroid layout, dummy devices and identical device orientation.

Figure 3.11: Schematic of synchronous rectifier. Circled components are not included in the integrated circuit.

Figure 3.12: Power dissipated in shorting transistors with increasing resistance and open-circuit voltage.

Figure 3.13: Power dissipated in secondary coil with increasing shorting resistance and open-circuit voltage. Shorting resistance has little effect on losses in this range. An open-circuit voltage of 3.736Vpk results in 66.93mW of power dissipation in the coil winding resistance.

Figure 3.14: ADSR efficiency with 100mΩ NMA and 400mΩ PMA.

Figure 3.15: Simulated body current for PMA and NMA body diodes.

Figure 3.16: The bias circuit sets up the bias voltages for the comparator.

Figure 3.17: Comparator schematic. First stage uses a folded cascode input with a cross coupled latch. The second stage utilises a level shifter to boost the comparator voltage to the rails.

Figure 3.18: Half circuit for the comparator.

Figure 3.19: Comparator second stage.

Figure 3.20: Simulated comparator rise and fall times for $V_A$ and $V_{A+}$ respectively.

Figure 3.21: Simulated comparator rise and fall times for $V_{A+}$ and $V_A$ respectively.

Figure 3.22: Voltage divider circuit with over-voltage protection.

Figure 3.23: Bridge-driver circuit with multiplexor for shorting control input. Multiplexor is circled in blue.

Figure 3.24: Bridge-driver test setup.

Figure 3.25: Shorting control circuit with voltage divider.

Figure 3.26: Shorting of the load to ground through the PMA transistors is prevented by the PMA shorting control circuitry.

Figure 3.27: Test setup for shorting control with 1.1V reference voltage and 4uA reference current. Output capacitance C1 and C2 are taken from parasitic extraction of final circuit.

Figure 3.28: Simulation of high and low threshold variation with bias current.
Figure 3.29: HH and LL delay changes due to current bias variation (without layout parasitics). ................................................................. 101
Figure 3.30: Current mirror with minimum supply voltage of $V_t + 2V_{ov}$ and zero systematic gain offset ................................................................. 103
Figure 3.31: Two low input voltage current mirrors are combined making a low supply voltage, high accuracy bandgap voltage reference and current mirror ................................................................. 104
Figure 3.32: Common centroid BJT layout ................................................................. 106
Figure 3.33: Common centroid FET layout of the bias circuit with symmetric current flow and guard bands ................................................................. 107
Figure 3.34: Common centroid resistor layout for the reference circuit ................................. 107
Figure 3.35: Zero static current start-up circuit ................................................................. 108
Figure 3.36: Test setup for the start-up circuits start up voltage and false start delay .................... 109
Figure 3.37: Bridge-driver buffer with rise time control ................................................................. 111
Figure 3.38: Complete FWR circuit. Rectifier control circuitry (red), voltage divider (green) start-up circuitry (brown), shorting control circuitry (orange) rectifier bridge (blue) and reference circuit (purple) ................................................................. 112
Figure 3.39: Layout of the full wave rectifier including NMA transistors (white boxes), PMA transistors (brown boxes), control circuitry (red box) and surrounding bond pads. Top metal layer is not shown ................................................................. 114
Figure 3.40: Christmas tree routing with current flow shown in blue. Current density is maintained relatively constant along the tree’s length ................................................................. 115
Figure 3.41: FWR efficiency test setup ................................................................. 116
Figure 3.42: Simulated and analytical PCE of the ADSR with output power. Analytical PCE is re-plotted with the simulated control losses included (Simulated without parasitics) ................................................................. 116
Figure 3.43: Efficiency and peak current against rise time ................................................................. 117
Figure 3.44: Simulated shorting control transistor losses with $V_{OC}$ from 0.35V to 3.736V ................................................................. 118
Figure 3.45: Simulated shorting control winding losses with $V_{OC}$ from 0.35V to 3.736V for a 500mΩ winding resistance ................................................................. 118
Figure 4.1: Photo of an ADSR die (1.29mm by 2.12mm). Christmas tree structures and metal slotting are visible on the top metal layer. Small metal squares are part of the fill pattern inserted by the foundry to ensure reliable manufacturing ................................................................. 121
Figure 4.2: ADSR die attached to a PCB with gold wire bonds before epoxy is used .......... 123
Figure 4.3: Schematic of synchronous rectifier. Circled components are not included in the integrated circuit. ................................................................. 124

Figure 4.4: Measured $I_B$, $V_{DS}$ curve for NMA and PMA transistors. ........................................ 125

Figure 4.5: Analytical start-up rectifier efficiency as a function of load voltage with measured 1.15V diode forward voltage. ................................................................. 125

Figure 4.6: Measurement setup for PCE and peak current measurements. The sense-resistant and trace have a small parasitic inductance. ................................................................. 129

Figure 4.7: Test PCB with ferrite core test case coil. Parasitic inductance was minimised by keeping key traces as short as possible (top). A large coil was used in the constant current primary to keep the loosely-coupled approximation true (bottom). ........................................ 130

Figure 4.8: (Top) Increase in apparent efficiency due to the influence of $R_{sense}$ at two different output powers. (Bottom) Decrease in output power with approximately 5.6mW output power (Left) and 55mW output power (Right). ........................................ 131

Figure 4.9: Power spectral density of sense-voltage waveform during ADSR operation. .... 132

Figure 4.10: Measurement error in the input power frequency components due to a 3.4nS delay introduced by the amplifier. ................................................................. 133

Figure 4.11: Simulated and measured PCE and peak current through rectifier. The influence of the parasitic inductance has been removed with convolution correction. Simulated: simulated data without using the sense-resistor. Sim from $R_s$: simulated data calculated using the simulated voltage across a sense-resistor with a parasitic inductance. $L_s$ correction: data after using the discrete time deconvolution to remove effect of parasitic inductance........ 138

Figure 4.12: Probe measurement points for PCE measurements........................................ 139

Figure 4.13: Oscilloscope window showing voltage across the sense-resistor (yellow), differential input voltage to the ADSR (blue), floating output voltage (purple) and floating ground (green) for the 150Ω load................................................................. 139

Figure 4.14: Oscilloscope window showing half wave rectifier behaviour of the ADSR for the 680Ω load. Voltage across the sense-resistor (yellow), differential input voltage to the ADSR (blue), floating output voltage (purple) and floating ground (green). ............. 140

Figure 4.15: Rectifier with output pins for shorting control voltage measurement inputs.... 141

Figure 4.16: Test circuit for secondary efficiency with shorting control. ..................... 142

Figure 4.17: Test circuit for measuring the effect of shorting control on secondary pickup efficiency......................................................................................... 143
Figure 4.18: ADSR and shorting control with a 50% duty cycle. Sense-voltage (yellow) and input voltage (blue). ................................................................. 144

Figure 4.19: Efficiency of the secondary and rectifier including and excluding losses during shorting control. The effective load is proportional to the rectifier duty cycle. .................... 145

Figure 4.20: Measured open-circuit voltage calculated from the secondary current through the sense-resistor. The open-circuit voltage amplitude varies from cycle to cycle but average amplitude (Vpeak) is shown. ................................................................. 146

Figure 5.1: Capacitive divider for load matching. ................................................................. 151

Figure 5.2: Carrier PCB (left) and carrier PCB with a bonded-out IC attached to mouse telemeter (right). ................................................................. 152

Figure 5.3: TxM mouse telemeter with integrated circuit. Power leads supply the micropump controller directly from the rectifier output. Ceramic shell is approximately 20mm x 15mm x 8mm ................................................................. 152

Figure 5.4: Air core coil secondary efficiency when tuned to 600KHz. ......................... 154
List of Tables

Table 1.1: Approximate lifetime estimates for a smart shunt powered from batteries or supercapacitors.................................................................12
Table 2.1 Approximate design equations for series-tuned and parallel-tuned secondary pickups modified from [68] and derived (bold).................................................................21
Table 2.2: Summary of derived equations and conditions.........................................................52
Table 3.1: NMOS and PMOS drain current and regions of operation.................................56
Table 3.2: Key devices and options available in XH018 CMOS process ......................66
Table 3.3: Bias circuit calculated dimensions and modified dimensions after simulation. W is width, L is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices. .................................................................80
Table 3.4: Design equations for the comparator’s first stage. .............................................82
Table 3.5: Comparator first stage transistor sizes and design variable summary. W is width, L is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices........................................................................................................................................88
Table 3.6: Transistor sizes calculated for the comparator’s second stage. W is width, L is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices.................................................................88
Table 3.7: Transistor sizes for shorting control multiplexor. W is width, L is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices. ..............................................................................93
Table 3.8: Transistor sizes for shorting control multiplexor. W is width, L is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices. ..............................................................................94
Table 3.9: Simulation result summary for the NMOS Driver. ........................................96
Table 3.10: Summary of SC simulation results with 1.1V reference voltage and 4uA current reference.................................................................99
Table 3.11: Voltage and current reference transistor sizing. W is width, L is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices. ..............................................................................104
Table 3.12: The mean bias voltage and bias current are presented as well as the standard deviation (STD) obtained from a 500 point Monte Carlo simulation.................105
Table 3.13: Start-up circuit test results. .............................................................................109
Table 3.14: Transistor sizes for NMOS bridge transistor turn on rise time control. W is width, L is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices.  

Table 4.1: Measurement results for the bridge driver thresholds with simulated result for comparison. 

Table 4.2: Measurement and simulated results for the bridge driver delay. 

Table 4.3: Voltage bias measurements from five dice. Simulated min and max are ± 2σ. 

Table 4.4: Measured and calculated power loss during shorting control. 

Table 4.5: Comparison of ADSR with previous work.
Chapter 1  Introduction

1.1. Active Implantable devices

Active implantable devices include electronic circuits and use electrical power to deliver their therapeutic function. When the function addresses a lifetime condition, then power management and device size are always going to be important design considerations. This thesis seeks to advance the state-of-the-art relating to managing the use of inductive power transfer to provide power to active implantable devices. It does this by offering improved control of power regulation and miniaturisation through implementation of circuits in an application specific integrated circuit (ASIC).

Some active implantable devices can be made sufficiently efficient to have adequate battery capacity to operate for many years, for example pacemakers tend to be in the region of ten years [1], [2]. Other implantable devices require so much power that no implantable battery is able to provide sufficient energy, for example heart pumps, or left ventricular assist device, will use a percutaneous lead to provide power. However, there are a range of devices where a battery is nearly sufficient, and hence the ability to recharge it while implanted can make the difference for the device being viable. These devices requiring a mid-range power include deep-brain electrical stimulators [3], [4], and potentially new treatments for Parkinsons disease based on optogenetic light stimulation [5], artificial sphincters [6], [7] and hydrocephalous management [8]. Hydrocephalous is the excess of fluid in the brain and both monitoring of pressure and control of drainage offer exciting prospects for new active implantable devices. The condition of hydrocephalus will be used to motivate and provide context to the research and developments presented in this thesis. In many situations relating to power management, the same principle can be used for other mid-power range active implantable devices.

1.2. Hydrocephalus

Hydrocephalus is a neurological condition in which excess cerebrospinal fluid (CSF) accumulates within the brain causing the intracranial pressure (ICP) within the skull to increase. Congenital hydrocephalus is present at birth and occurs at a rate between 0.5 and 4 per 1000 live births [9].
1.2.1. **Cause and Symptoms of Hydrocephalus**

The brain is surrounded by cerebrospinal fluid (CSF) which, among other functions, provides buoyancy to support the weight of the brain and protect the brain from physical damage [10], [11]. Four connected ventricles within the brain produce and contain CSF. As depicted in Figure 1.1, CSF is produced primarily in the ventricular surfaces and choroid plexus, a network of capillaries and specialised cells present in each ventricle. CSF flows through the ventricular system before being reabsorbed into the blood stream in the subarachnoid space via the arachnoid villus, small protrusions from a protective membrane covering the brain [10], [12]. The total rate of CSF production, and absorption is approximately \(20mLH^{-1}\) and normal ICP for adults is between 7mmHg and 15mmHg with some variation due to posture and activity/straining [13], [14]. ICP is pulsatile in nature and varies about the mean value with the heart rate, breathing rate and other physiological factors [12], [15], [16]. Hydrocephalus is the result of a CSF production rate greater than the absorption rate and leads to an increased CSF volume, dilation of the ventricular system and often increased ICP [11]–[13]. Symptoms of increased ICP and hydrocephalus include headache, vomiting, nausea, irritability, coma and death if untreated [13]. There are multiple forms of hydrocephalus such as communicating and non-communicating but these differences are outside the scope of this thesis.

![Figure 1.1: CSF circulation within the brain](image-url)
1.2.2. Treatment

Hydrocephalus is primarily treated with the insertion of a cerebrospinal fluid shunt which drains excess CSF from the brain. Typically, shunts consist of a proximal ventricular catheter, one way valve and distal catheter [18]. The shunt is commonly placed with the proximal catheter inserted into a ventricle and the distal catheter into the peritoneal cavity (in the abdomen) although other insertion points are used [19]. Once ICP reaches a threshold the one way valve opens and allows CSF to drain from the ventricles to the distal catheter insertion point. A variety of more sophisticated valves exist including programmable pressure settings and anti-siphoning mechanisms [18], [20].

1.2.3. Shunt Complications

Shunts became the most common method of treating hydrocephalus throughout the 1950s and 1960s [13], [19]. While shunts are an effective method of managing hydrocephalus, their reliability is low. It has been estimated and commonly cited that within the first 2 years after shunt insertion as many as 40% [21], [22] of shunts fail and 87.5% of paediatric shunts fail by 10 years [23]. A more recent study published in 2014 carried out by Symss and Oi reviewed previous literature on shunt failure. They found reported shunt survival rates at 1 and 2 years were between 50% to 70% and 47% to 53% respectively [24]. Some of the common shunt failure modes are outlined below.

**Obstruction**

Obstruction refers to any blockage of the shunt that impedes CSF flow. Of 177 reoperations required in a study by Kestle et al. obstruction accounted for 74% [25]. Obstruction can occur at any point along the shunt but predominantly at the ventricular catheter tip and the valve [26].

**Mechanical Failure**

Mechanical failure may be due to fracturing of the catheter, disconnecting of the various parts of the shunt, migration of the catheter from its original location or initial misplacement of the catheter.
**Over Drainage**

Over drainage occurs when the shunt drains excess CSF and can result from factors such as siphoning and the “pumping effect” due to the pulsatile nature of ICP [27]. Excess CSF drainage results in a decreased ICP below the normal physiological range. Kestle et al. found 7% of reoperations occur due to over drainage [25]. Various valves have been designed to address the problem of over drainage with some success. These valves include anti-siphoning valves and programmable valves with magnetically programmed variable resistance [9].

**Infection**

Infection is a common cause of shunt failure and accounted for 16% of shunt failures within a two year period in the study by Kestle et al. [25]. The greatest risk of infection is within the first 6 months of shunt placement [9]. Infections typically occur during operation, through the blood stream or via reverse travel from the distal catheter to the proximal [9].

**1.3. Monitoring**

Various innovations in shunts have increased reliability and effectiveness. However, the failure rate is still considered high, and new methods of increasing shunt reliability should be found. One of the key limits of current shunt technology is the lack of rapid, low cost methods for predicting or alerting patients of shunt failure. Symptoms of shunt failure are somewhat ubiquitous and may present as a headache alone [28], [29]. It can be difficult to assess whether symptoms are due to over or under drainage as they present in similar ways [13].

Multiple imaging methods are used to detect shunt failure, the major three being ultrasonography (US), CT and MRI [9]. Ventricular size, shunt location and shunt integrity can be found through CT scans which are the standard method of diagnosis [29]. However, CT scans are not carried out regularly while the patient is healthy. Consequently, the normal ventricular size is not always known making it difficult to detect if changes have occurred. Furthermore, hydrocephalic patients may require multiple CT scans throughout their lives exposing them to multiple doses of radiation.
1.4. The Cost of Hydrocephalus

1.4.1. Direct Cost

Shunt related procedures result in an average length of 8.4 hospitalisation days and an average cost of $35,816 ± $810 USD per patient in the United States [30]. Patwardhan and Nanda estimated hydrocephalus treatment costs the US healthcare system one billion dollars per annum [30]. A more recent estimate predicted paediatric hydrocephalus alone cost the US between $1.4 billion USD and $2 billion USD per year in healthcare expenditures from 1997 to 2003 [31]. Furthermore, Tamara et al. found that paediatric hospital admissions in the US for shunt complications (9600–10,300 admissions) and shunt infection (2200–2400 admissions) were more common than for shunt placement (4400–4700 admissions) [31]. This indicates shunt complications and infections account for a large per cent of the US hydrocephalus related healthcare costs.

1.4.2. Social Cost

Families of children with shunt treated paediatric hydrocephalus experience many costs and stresses not accounted for in hospital expenditures. Rekate and Kranz have stated a headache often results in an emergency room visit for many patients [32]. Frequently these visits result in costly scans, medical intervention and stress that may, in fact, not be justified [32]. A study carried out on a voluntary self-reporting database with 1242 participants provides reports on the presence of severe, disabling headaches in hydrocephalus patients [32]. It was found that 29% of children aged 12 months to 12 years had severe, disabling headaches, and 42% of children aged 13 years to 19 years had frequently experienced severe, disabling headaches. The data was not collected in a randomised study but provides some insight into the additional difficulties and stresses for patients with hydrocephalus and their family members.

1.5. A Smart Shunt for Hydrocephalus

A wireless pressure monitor small enough to be implanted within the brain would allow instantaneous detection of raised ICP. Headaches could be diagnosed as resulting from raised ICP, lowered ICP or normal ICP causing no immediate concern. Over a longer time period, ICP measurements could help clinicians optimise valve choices and valve settings. Ideally, a pressure monitor would provide accurate and stable intracranial pressure measurements for
the life of the patient, or at minimum, the average life of a shunt. In addition to one-off measurements, continuous or semi-continuous monitoring could lead to shunt assessment and early detection of shunt failure. Including active pumps or valves would allow ICP to be regulated more closely and makes the prospect of shunt-clearing or obstruction removal a possibility.

This leads to the idea of a smart shunt where ICP is monitored and controlled in a closed loop system maintaining ICP within the physiological range [11], [13], [27], [33].

1.5.1. Components of a Smart Shunt

The key components of a smart shunt are outlined below. Among other considerations, hermetic sealing, biocompatibility [34] and MRI compatibility are important challenges [35][36].

**Pressure Sensor**

The pressure sensor must be accurate and stable over the lifetime of the implant. Long term sensor offset and sensitivity drift are major concerns for implantable pressure sensors. Drift results from a combination of sources. Factors such as mechanical fatigue and water ingress into the reference pressure cavity are major challenges but can be minimised by design choices and hermetically sealing the sensor. Environmental drift factors such as tissue encapsulation are unavoidable [37].

**Communications**

Two-way wireless communication for transmitting data and commands is required. Many low power wireless communication circuits are now available with very small form factors. The key challenge is keeping the power draw low and the communication link reliable. For implants housed in titanium cans, the antenna design is also difficult as radio signals are attenuated by the metal housing.

**Pumps**

A pump could provide CSF flow control based on ICP measurements. However, constant power would be required for it to operate limiting its practicality. A more reasonable option would be using a pump as a method of back flushing or providing an unblocking routine to
clear obstructions. Research would have to be completed into the effectiveness of pumping as a method of shunt obstruction removal or prevention.

The predominant limitations for pumps are size, power requirements, number of operating cycles and biocompatibility. A review by Laser and Santiago indicates there are multiple micropumps under research that are smaller than 1cm³ providing flow rates above 100µL/min with pressures above 10kPa (75mmHg) [38]. However, power consumption data was not available on many of these devices. Small, low power pumps are also commercially available such as the Bartel mp6 piezoelectric micropump [39]. It can provide flows of 7ml/min, back pressures of 600mbar (50mmHg), requires less than 200mW to operate and is 30x15x3.8mm in size. It is helpful to know the power requirement of such pumps as this assists with determining the requirements of a wireless power supply system.

**Variable Valves**
An electronically variable valve would allow automatic flow control, potentially only requiring power when adjustments are needed. The valve resistance could be adjusted based on ICP providing closed loop control. New Scale Technologies produces a linear actuator which utilises a piezoelectric squiggle motor and can provide 0.20N of force with less than 500mW of power. It is 28x13.2x7.5mm in size and has a 6mm travel range [40]. An actuator similar to this could be used to create a small variable-resistance valve. Biocompatibility, hermetic sealing and component lifetime would have to be ensured for a practical system. Additional research into MEMS-based micro valves for CSF and other applications is being carried out for small on-off and continuously-adjustable valves [41]–[44].

The power requirements in these circumstances are for a large power (e.g. 500mW) but only for the duration to change the value from one setting to another setting. Hence the mean power consumption could be extremely low (or wireless power only applied at the time of value setting adjustment).

**Housing**
Hermetically sealing electronics and mechanical devices from the saturated, wet environment of the body is a significant challenge. Titanium offers excellent impermeability and is often the material of choice for long term implants but prevents electromagnetic radiation from passing through [45]. Ceramics and glasses also offer low permeability to water. They do not
block electromagnetic radiation but can be more difficult to manufacture and are brittle compared with metals. Another important factor for the housing is how it affects MRI images. The most important factor for MRI imaging artefacts from implants is the implant composition [46]. The ideal material or combination of materials depends on the device size, geometry and location.

**Power Supply**

The nature of the power supply will largely depend on how the smart shunt is used. One-off measurements could potentially be supplied for the life of the device from non-rechargeable lithium iodine batteries. Continuous monitor however would likely require re-chargeable batteries. Unfortunately, rechargeable batteries have a limited number of recharge cycles and may be too bulky for an implant on or within the skull. Super capacitors are an appealing alternative to batteries. They can be charged rapidly and have many recharge cycles. The drawback of supercapacitors is their lower energy densities compared to batteries.

Inductive power transfer (IPT), a form of wireless power transfer (WTP), can power an implantable device indefinitely. An inductive pickup coil must be implanted beneath the skin, and an external coil needs to be present to provide power. Important issues for this technology relate to size of components, alignment of external and internal coils (and patient convenience), MR compatibility and management of any heating effects.

**1.5.2. Size Constraints**

Evaluation of an acceptable size for a smart shunt may depend on clinicians’ views of the benefits and risks associated with implantation. An ICP monitor small enough to be placed between the skull and brain would be an ideal solution. It would be protected from physical damage by the skull, but the monitor would need to be extremely slim. The complexity of placing the implant below the skull may also reduce the viability of this approach. Regardless of where the implant is placed, it should be as small and unobtrusive as possible. Some example implants acceptable for placement on or near the skull are outlined below.

Two programmable valves for hydrocephalus from Medtronic, the Starta and Delta valves, are 16x47x7mm and 16.5x40x8mm respectively. They are implanted outside the skull under
Chapter 1  
Introduction

the skin. These devices provide a valuable reference for what is likely to be clinically acceptable.

An ICP monitor, the Raumedic Neurovent P-tel, has CE approval for 90 day implantation within humans (status, March 2016) [33], [49]. It consists of a cylindrical ceramic housing 31.5mm in diameter and 4.3mm in height that rests on the surface of the skull under the skin [49]. A 30mm long, 1.67mm diameter catheter with a pressure sensor at the tip is inserted through a bur-hole in the skull into the brain parenchyma [49].

Neural recorders commonly require device placement on or around the skull. One of the larger neural recorder designs developed for clinical trials was sealed in a hermetic, 50mm diameter, 12.54mm high titanium can [50]. The housing was intended to be placed into a 50mm hole in the skull where bone was removed.

1.5.3. Power Requirements

This thesis is focused on providing power to implantable devices and the management of hydrocephalous helps identify a selection of power needs to provide lifetime management. The power needs depend on how the smart shunt is used, and what type of features are included. Three different use-cases will be developed to illustrate the variety of the power supply requirements: on-demand monitoring, continuous monitoring and active pumping or valve adjustment.

ICP sampling rate and digital resolution also affect the power draw as they determine how often the sensor is active and how much data is wirelessly transmitted. Sampling rates of approximately 100Hz are commonly used for ICP analysis [8], [51]–[53]. The impact of sampling rate on ICP time domain analysis was investigated by Holm and Eide. They found a 50Hz sampling rate was sufficient but recommended interpolating to 100Hz. Many of these results were from studies interested in ICP waveforms, not just the mean value hence lower sampling rates may still provide accurate mean ICP estimates.

Power requirements will be developed for a 100Hz sampling rate to allow for the potential use of ICP dynamics in addition to mean and ensure all important ICP frequency content is
captured. Resolution depends on the pressure measurement range and the number of digital bits representing the data.

**On-Demand Monitoring**

For this use-case, the pump or valve is not adjusted and the pressure monitor is only activated to take a one-off ICP measurement. The expected use is for patients or clinicians to quickly assess the mean ICP and determine if it is within the physiologically expected range. This would allow symptoms such as migraines to be assessed without hospital visits. Pressure measurements would be taken over multiple ICP waveform periods to determine the average. Measuring over 5s to 15s periods is standard for state of the art technology [53]. It is suggested that longer averaging periods are necessary to average across multiple respiratory cycles (6-10s) and some suggest an accurate mean ICP requires averaging over thirty minutes [54]. Despite this, it is expected that averaging over one respiratory period would provide a strong indication of raised, lowered or normal ICP. As such, power requirements for on-demand monitoring will be developed for a 15s window sampled at 100Hz.

**Continuous Monitoring**

ICP can be monitored continuously over a period of time to assess the shunt dynamics in greater detail. This could aid clinicians in adjusting valve settings after shunt implantation or help assess patients experiencing hydrocephalic symptoms with shunts that appear to function correctly.

**Active Pumping and Valve Adjustment**

Automatic valve adjustment and obstruction prevention using active pumps could be carried out when symptoms occur. As an example, a patient has a headache, an ICP measurement is taken and found to be slightly high, the valve is adjusted to increase flow. Obstruction prevention could also be scheduled and carried out regularly, e.g. every night a pump based flushing routine could be run. Power requirements will be developed for a one minute pumping routine every day.

**1.5.4. Appropriate Methods for Lifetime Power**

Lithium based batteries have high energy densities and have been used in pacemakers, neural stimulators, implantable drug pumps and implantable defibrillators [55]. They have relatively
long lifetimes, up to 10 years in some pacemakers [1]. A typical coin cell lithium based non-
rechargeable battery 20mm in diameter and 3.2mm in height can have a capacity in the range
of 190-225mAh [56]. Rechargeable Li-ion batteries the same size have much lower
capacities, normally within the region of 75mAh [57]. Despite a shorter lifetime, they can be
re-charged hundreds of times before losing a significant proportion of their initial capacity.

Supercapacitors are a power storage option that can withstand over 500,000 recharge cycles
[58]. They can be charged much faster than batteries but have significantly lower energy
densities. One commercially available product has a $7.5mF$ capacitance, internal resistances
of $25\Omega$, $2.6V$ maximum voltage and is $3.2x2.5x0.9mm$ in size [59]. Supercapacitors’ small
form factor makes them an appealing option for implantation.

The power requirements of an ICP monitor can be estimated using performance
characteristics from state of the art communication ICs. Ignoring current needed for sensing,
start-up power and regulator losses, the different lifetime estimates of a battery are provided
in Table 1.1 under different use cases. These estimates assume that the majority of power is
consumed by communications and active pumping and that overheads relating to power
management are small. They are similar to the estimates from experimental results obtained
by Gomez, Oller and Paradells in an evaluation of Bluetooth low energy performance. They
estimated a connected device transmitting a 37bit packet at $0dBm$ every 32s would run for
approximately 14 years with a 230mAh battery [60]. The expected lifetime of a $11.25mF$
supercapacitor is also given in Table 1.1 for a $5V$ initial charge and $3V$ minimum voltage. In
practice, leakage current and internal resistance within the capacitors would reduce these
times.

Table 1.1 gives an indication of the duration of operation when using a 20mm diameter
battery – probably at the top end of what might be considered viable for implantation on the
head. For very basic 15 seconds of data per day, the primary battery could last as long as 8
years. When more active data or operations are required, then the limitation of managing a
lifetime condition become more apparent. Using larger batteries is likely infeasible due to
space constraints. In a practical circuit, power losses from regulators, amplifiers, and
particularly the pressure sensor would reduce the lifetime estimates.
Table 1.1: Approximate lifetime estimates for a smart shunt powered from batteries or supercapacitors.

<table>
<thead>
<tr>
<th>Device</th>
<th>NRF512</th>
<th>Bartel mp6 (pump)</th>
<th>Lifetime with 225mAh battery</th>
<th>Lifetime with 75mAh battery</th>
<th>Lifetime with 11.25mF cap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active current</td>
<td>57µA</td>
<td>60mA</td>
<td>≈ 207 days</td>
<td>≈ 69 days</td>
<td>≈ 4.5S</td>
</tr>
<tr>
<td>Active pumping</td>
<td>-</td>
<td>46µA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous sampling</td>
<td>57µA</td>
<td>-</td>
<td>≈ 164 days</td>
<td>≈ 54 days</td>
<td>≈ 6min</td>
</tr>
<tr>
<td>Average Current</td>
<td>3µA</td>
<td>-</td>
<td>≈ 8.6years</td>
<td>≈ 2.8years</td>
<td>≈ 2hours</td>
</tr>
</tbody>
</table>

Inductive power transfer can offer genuine lifetime operation. Applications including cochlear implants [61], neural recording [50], [62], [63], neural stimulation [64], optical nerve stimulation [65] and glucose monitoring [66] have all made use of wireless power transfer. The presence of an external unit to provide power to the implant generally limits its application to implants that do not require continuous power. Combining inductive power transfer with batteries would allow lifetime powering and continuous operation. With advances in supercapacitor technology, it is possible a supercapacitor could be recharged regularly and store the energy required for multiple 15s measurements.

Energy harvesting is an active research area but has not been considered as the power available from such systems is on the order of micro watts [55].

Overall, the power supply should be capable of supplying up to 500mW to power a micropump or valve and should efficiently supply as low as 50mW to maintain low implant heating.

1.6. Previous Research into Wireless Power for Implantable Devices

Efficient wireless power transfer is crucial to minimise heating for an implantable device, particularly for small implants [67]. A larger implant has more surface area by which heat can

---

1 200 bytes/S are needed for 15s of 100Hz sampled 16bit data. Transmit current for 20 byte package every 100mS is 57µA [119] (estimate assumes one package per connection event).
2 The Nordic Semiconductors online calculator was used to estimate current consumption during advertising and transmitting. Advertising every 10.24S (max interval) at 0dB with a 10 byte payload gives an average current of 3µA [119].
dissipate. In contrast, a smaller device has a lower surface area and the implant temperature can rise to unacceptably high levels with lower power dissipations. For the Raumedic Neurovent P-tel with a 31.5mm diameter and 4.3mm height, wireless power can supply the necessary energy for low, 5Hz frequency pressure monitoring. To provide the potential 200-500mW of power for an active pump or valve, a specialised wireless power system is required.

Inductive Power Transfer (IPT) is a form of wireless power transfer that uses a primary coil to transfer power across an air gap or through skin to a secondary coil. An alternating current in the primary coil generates a time varying magnetic field which induces an alternating current in a secondary coil situated within the field. A capacitor in parallel or series with the inductor is used to tune the pickup resonant frequency to the inductive power transfer frequency. The induced current is rectified, filtered and regulated to create a stable DC power supply. In addition to rectification, some form of power flow control is required to ensure the output DC voltage remains constant despite distance and orientation between the coils.

Rectification of the sinusoidal pickup voltage is often achieved with diode rectifiers or synchronous rectifiers. The efficiency of a diode bridge rectifier is approximately \( \eta = \frac{V_{DC}}{V_{DC} + 2V_{FW}} \) where \( V_{DC} \) is the output voltage assuming the ripple is small and \( V_{FW} \) is the diode forward voltage drop [68]. A Schottky diode with a 0.3V forward voltage drop and a DC output voltage of 3.3V would give an efficiency of approximately 85%. To achieve higher efficiencies with low output voltages, research into synchronous rectifiers using switches instead of diodes has led to the development of many integrated circuit rectifiers.

Synchronous rectifiers that use actively driven transistors to replace diodes in a full wave bridge rectifier have proven to be efficient with low output voltages and have been fabricated in standard and HV CMOS [69]–[77]. However, these designs are aimed at applications requiring 10mW-100mW of power at frequencies of 1MHz-13.56MHz or for providing greater than 500mW with IPT pickup configurations less suited to an implantable device. Xing Li has demonstrated a 25mW-450mW output power with the low 1.2V output [25]. Furthermore, these designs either do not include any method of power flow control or use methods unsuitable for the wide range of coupling conditions which must be accounted for in a medical device.
There is a clear need for a wireless power transfer system capable of supplying up to 500mW of power with power flow control that is small enough and efficient enough to be implanted inside or around the skull.

1.7. Objective and Scope

The objective of this research is to develop an inductive power transfer secondary capable of powering an implantable ICP monitor with an active micropump or microvalve. The primary challenges of this research are miniaturising the power transfer circuitry size and maximising the efficiency to reduce heating. Emphasis is placed on reliability for lifetime implantation and robust design to strong magnetic fields. The thesis is organised as follows:

Chapter 2 introduces the structure of the inductive power link. A background into inductive power transfer is given followed by the development of suitable wireless power pickup structures for the desired power supply range. Different rectifier options are discussed and the theoretical performance of a synchronous rectifier is analysed. Challenges related to the practical implementation of a synchronous rectification are addressed. Voltage management and power flow control strategies are introduced, and a suitable method, shorting control, is covered. Lastly, an argument is developed for the design of an integrated circuit rectifier and power flow controller.

In Chapter 3, the development of an integrated circuit synchronous rectifier and power flow controller capable of providing output powers up to 500mW with 90% efficiency is carried out. Firstly, the concept of integrated circuits is introduced followed by the challenges and design procedures specific to ICs. An overview of a synchronous rectifier structure suitable for CMOS integration is described. The design of each sub-circuit in the rectifier and power flow controller is detailed with simulation results. The final electrical and physical design of the IC is presented, and the expected performance is analysed.

Chapter 4 presents the experimental results for a fabricated integrated circuit. The measurement setup and experimental procedure is detailed for the rectifier and power flow controller. Experimental performance is compared with the simulation performance for the IC
sub-circuits and complete rectifier. Power dissipation under maximum expected coupling conditions is also examined.

In Chapter 5, the fabricated IC is included in a bio-potential measurement telemeter with a wireless communications transceiver. A micro pump is powered from the IC to evaluate its performance in a system similar to a smart shunt.

Chapter 6 provides a summary and conclusions of this research. The contributions made in this thesis are outlined, and direction for future work is presented.
Chapter 2  
Structure of the Power Link

Wireless power transfer based on inductive coupling is referred to as inductive power transfer (IPT). A primary coil is used to transfer power across an air gap or through a medium such as skin to a secondary coil. An alternating current driven in the primary coil generates a time varying magnetic field which induces an alternating current in a secondary coil situated within the field as shown in Figure 2.1. A capacitor in parallel or series with the secondary coil is used to tune the resonant frequency to the inductive power transfer frequency. The coil and capacitor create a “pickup”. A rectifier and smoothing capacitor can be used to convert the AC power from the coil into a DC supply to power an implanted electronic device.

![Inductive Power Transfer Diagram](image)

Figure 2.1: Overview of an inductive power transfer system.

An intracranial pressure monitor with active shunt management is constrained by both size and heating. The sensing circuitry, signal conditioning, RF communications and power management circuitry as well as hermetic packaging must fit into a minimal space within the skull. Concentrating all of the circuitry into a small volume increases the risk of tissue damage from heating as the power losses for IPT are concentrated with less surface area from which the heat can dissipate. This chapter analyses the design considerations for the secondary side of the IPT link including the resonant topology of the pickup and the rectifier design. Design of the primary is not considered.
2.1. Inductive Power Transfer Fundamentals

The amount of power delivered to the load depends on the coupling of the coils, strength of the magnetic field and operating frequency. The coupling describes how much magnetic flux generated by the primary passes through the secondary coil. This can be affected by how close the secondary is to the primary, the orientation of the secondary within the primary’s field and the relative size of the coils. The coupling coefficient is a number between zero and one defined as [68],

\[
k = \frac{M}{\sqrt{L_1 L_2}}
\]  

(2-1)

where \(M\) is the mutual inductance between the coils, \(L_1\) is the primary inductance and \(L_2\) is the secondary inductance. A coupling coefficient of one means all of the flux from the primary flows through the secondary. A coupling coefficient of zero means none of the field intersects the secondary coil [68]. The equivalent two port model of Figure 2.2 can be used to analyse the system.

\[
\begin{align*}
V_1 & = (R_1 + j\omega L_1)I_1 + j\omega M I_2 \\
V_2 & = (R_2 + j\omega L_2)I_2 + j\omega M I_1
\end{align*}
\]

(2-2)

\[
\begin{bmatrix}
V_1 \\
V_2
\end{bmatrix}
=
\begin{bmatrix}
R_1 + j\omega L_1 & j\omega M \\
\omega M & R_2 + j\omega L_2
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2
\end{bmatrix}
\]

Figure 2.2: Equivalent two port representation of the coupled inductive power link a) with mutual inductance and b) with dependent current sources [68].

Voltages \(V_1\) and \(V_2\) can be found from Figure 2.2 b):
An implantable device is often characterised by a loosely-coupled link where the equivalent impedance seen by the primary due to the coupled secondary is small [68][78]. In this case \( j \omega M I_2 \ll (R_1 + j \omega L_1)I_1 \) and (2-2) can be approximated to,

\[
\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_1 + j \omega L_1 & 0 \\ j \omega M & R_2 + j \omega L_2 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}
\]  

making \( j \omega M I_1 \) a voltage source that is independent of the secondary. Therefore, for the rest of the chapter, the design of the secondary will assume,

\[
V_2 = V_{OC} + (R_2 + j \omega L_2)I_2.
\]  

where \( V_{OC} = j \omega M I_1 \) with \( I_1 \) independent of the secondary [68][79].

### 2.1.1. Secondary Resonance

A capacitor can be placed in series or in parallel with the secondary pickup coil to achieve resonance. At the resonance frequency, the inductor’s reactance is cancelled by the capacitor’s reactance and the maximum oscillating voltage can be achieved.

![Figure 2.3](image)

**Figure 2.3**: Capacitive tuning of the pickup into resonance\(^3\) can be achieved with a) series tuning or b) parallel tuning.

The impedance of the series-tuned pickup from Figure 2.3 a) is [80][79],

\[
Z_{series} = j \omega L_2 + \frac{1}{j \omega C_2} + R_2 + R_C.
\]  

For the parallel-tuned pickup shown in Figure 2.3 b), the impedance is [80][79],

\[
Z_{parallel} = \frac{R_2 - \omega^2 L_2 C_2 R_C + j \omega (L_2 + C_2 R_C R_2)}{1 - \omega^2 L_2 C_2 + j \omega C_2 (R_C + R_2)}.
\]  

The imaginary part of the impedance can be cancelled at a specific angular frequency by choosing the correct \( C_2 \) value. Under these conditions the secondary draws only real power.

---

\(^3\) Assuming the reflected impedance from the primary is small i.e. the coupling and coil quality factors are low.
from the source. This is known as the Zero Phase Angle (ZPA) frequency and is the most commonly accepted resonant frequency for a damped resonant tank [80][79]. For the series-tuned pickup the ZPA frequency is,

\[ \omega_{ZPA_{\text{series}}} = \omega_0 = \frac{1}{\sqrt{L_2 C_2}} \] (2-7)

and for the parallel tank,

\[ \omega_{ZPA_{\text{parallel}}} = \omega_0 \sqrt{\frac{L_2 - C_2 R_2}{L_2 - C_2 R_C}} \] (2-8)

Provided \( C_2 R_2 \ll L_2 \) and \( C_2 R_C \ll L_2 \) then (2-8) is approximately equal to (2-7). These resonant topologies can be used for both the primary and the secondary tanks.

### 2.1.2. Single-Turn Equivalent Values

Analysis of the pickups can be simplified by using single-turn equivalent values. This is a method used by Lenaerts & Puers in [68] that recognises the quality factors of two coils having the same winding cross sectional area and geometry are independent from the number of turns. Providing the winding cross sectional area and geometry stay constant, both the coil inductance and resistance scale with the square of the number of turns. Under these conditions the coil inductance and resistance can be defined in terms of their single-turn values [68], [78]:

\[ L_0 = \frac{L}{N^2} \] (2-9)

\[ R_o = \frac{R}{N^2} \] (2-10)

The two coils of Figure 2.4 have equal cross sectional areas and turn radii.

![Two coils of equal cross sectional area, geometry and copper area with different numbers of turns](image)
The inductance of the four turn coil will be $16L_0$, and the resistance will be $16R_0$ as the length of wire has increased by a factor of 4 and the cross sectional area of each turn has decreased by a factor of four. Using single-turn equivalent values will allow comparisons between different coil designs with the same geometric and volume limitations. This technique is appropriate for the highly constrained design environment of the skull.

2.2. **Series and Parallel Pickup Properties**

Series and parallel-tuned secondary pickups have different optimal inductor and capacitor values for a given load resistance at a given frequency. The tuned pickup can be designed to provide maximum power transfer, maximum efficiency or a compromise between the two at a particular load. Series and parallel-tuned pickups can have different inductor designs to achieve maximum power transfer at the same load. An important decision in designing the inductive link is which topology to use as this affects the rectifier design. The properties in Table 2.1 modified from [68] can be used in designing a loosely-coupled IPT coil based on the expected secondary load and operating frequency. An assumption in these design parameters is that the coil will be designed to achieve maximum power transfer in the secondary. This is not the same as achieving maximum efficiency in the secondary.

A quantity from Table 2.1 used ubiquitously in coil design is quality factor $Q$. For an inductor $L$, its quality factor is $Q = \omega L / R$ where $R$ is the inductor’s series resistance including winding resistance and any core losses. A high quality factor is desirable in most applications.

2.2.1. **Secondary Gain**

A property commonly used in designing the IPT system is the link gain defined as [68],

$$A = \frac{|V_{RL}|}{|V_{L1}|} \quad (2-11)$$

As the primary is not considered in the secondary design for this application, a new parameter, the secondary gain, will be introduced to describe the voltage gain of the secondary in terms of the open-circuit voltage $V_{OC}$,

$$A' = \frac{|V_{RL}|}{|V_{OC}|} \quad (2-12)$$
Table 2.1 Approximate design equations for series-tuned and parallel-tuned secondary pickups modified from [68] and derived (bold).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Series-tuned</th>
<th>Parallel-tuned</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_2$</td>
<td>$\frac{\omega L_2}{R_2}$</td>
<td>$\frac{\omega L_2}{R_2}$</td>
</tr>
<tr>
<td>$\omega_0$</td>
<td>$\frac{1}{\sqrt{L_2 C_2}}$</td>
<td>$\frac{1}{\sqrt{C_2 L_2}} - \frac{1}{C_2 R_L^2}$</td>
</tr>
<tr>
<td>$C_2$</td>
<td>$\frac{1}{\omega^2 L_2}$</td>
<td>$\frac{1}{2\omega^2 L_2} \left(1 + \sqrt{1 - \frac{4\omega^2 L_2^2}{R_L^2}}\right)$</td>
</tr>
<tr>
<td>$P_{RL}$</td>
<td>$\frac{(I_1 \omega M)^2}{2} \frac{R_L}{(R_2 + R_L)^2}$</td>
<td>$\frac{(I_1 \omega M)^2}{2} \frac{C_2 L_2 R_L}{(C_2 R_2 R_L + L_2)^2}$</td>
</tr>
<tr>
<td>$P_{RL_{max}}$</td>
<td>$\frac{(I_1 \omega M)^2}{2} \frac{1}{4R_2}$</td>
<td>$\frac{(I_1 \omega M)^2}{2} \frac{1}{4R_2}$</td>
</tr>
<tr>
<td>$N_{2p_{max}}$</td>
<td>$\sqrt{\frac{R_L}{R_{20}}}$</td>
<td>$\frac{R_L R_{20}}{\sqrt{R_{20}^2 + \omega^2 L_{20}^2}}$</td>
</tr>
<tr>
<td>$A'$</td>
<td>$\frac{R_L}{R_L + R_2}$</td>
<td>$\frac{R_L}{\sqrt{R_L^2 + (R_L/Q_2 + Q_2 R_L)^2}}$</td>
</tr>
</tbody>
</table>

For the series-tuned pickup in Figure 2.5,

$$V_{RL} = V_{OC} \frac{R_L}{R_L + R_2 + j\omega L_2 - j/\omega C_2}. \quad (2-13)$$

With the tuning capacitance set such that $C_2 = 1/\omega^2 L_2$,

$$A' = \frac{R_L}{R_L + R_2}. \quad (2-14)$$

The secondary gain for a series pickup is always less than one. If $V_{OC}$ is large, this can be an advantage for the series-tuned coil. However often $M$ and hence $V_{OC}$ is low for a loosely-coupled coil. $V_{OC}$ can be increased by making $L_2$ large.

For the parallel-tuned pickup,

$$V_{RL} = V_{OC} \frac{R_L/(1 + j\omega C_2 R_L)}{R_2 + j\omega L_2 + R_L/(1 + j\omega C_2 R_L)}. \quad (2-15)$$

$$|V_{RL}| = V_{OC} \frac{R_L}{\sqrt{(R_2 + R_L - \omega^2 L_2 C_2 R_L)^2 + \omega^2 (C_2 R_2 R_L + L_2)^2}}. \quad (2-16)$$
Assuming \( \omega \approx 1/\sqrt{C_2L_2} \),

\[
|V_{RL}| = V_{OC} \frac{R_L}{\sqrt{R_2^2 + (R_L/Q_2 + Q_2R_2)^2}}. 
\] (2-17)

The secondary gain is,

\[
A' = \frac{R_L}{\sqrt{R_2^2 + (R_L/Q_2 + Q_2R_2)^2}}. 
\] (2-18)

This is valid only if \( Q_2 \) is large and \( R_L \) is large compared to \( R_2 \). The secondary gain for the parallel-tuned pickup can be greater than one giving a voltage boosting effect to the load.

2.2.2. **Loaded Parallel Coil Resonance**

When a load resistor is attached in parallel with the parallel-tuned coil it’s resonance frequency changes to [68],

\[
\omega = \sqrt{\frac{1}{C_2L_2} - \frac{1}{C_2^2R_L^2}} 
\] (2-19)

where \( R_L \) is the load resistance. When \( 1/(C_2L_2) \gg 1/(C_2^2R_L^2) \) and hence,

\[
R_L \gg \sqrt{L_2/C_2} 
\] (2-20)

(2-19) can be approximated to \( \omega \approx 1/\sqrt{L_2C_2} \), the normal condition for parallel resonance. This will become a key simplification for many derivations. It is important to understand the range of coils the assumption \( R_L \gg \sqrt{L_2/C_2} \) is valid over. For a pickup with an inductor matched to the load for maximum power transfer the validity of this approximation can be found as follows,

\[
R_L \gg \sqrt{L_2/C_2} \gg \sqrt{L_2^2\omega^2} \gg L_2\omega. 
\] (2-21)
Rearranging the turns number for maximum power transfer from Table 2.1 and substituting (2-21) gives,

\[ L_{2p_{\text{max}}} = L_{20}N_{2p_{\text{max}}}^2 = \frac{L_{20}R_{20}R_L}{R_{20}^2 + \omega^2 L_{20}^2} \]  \hspace{1cm} (2-22)

\[ \therefore R_L \gg \frac{\omega L_{20}R_{20}R_L}{R_{20}^2 + \omega^2 L_{20}^2} \] \hspace{1cm} (2-23)

Rearranging (2-23) gives a condition that is independent of \( R_L \),

\[ 1 \gg \frac{Q_2}{1 + Q_2^2} \] \hspace{1cm} (2-24)

The assumption \( \omega \approx 1/\sqrt{L_2 C_2} \) is valid for any coil with a high quality factor (approximately greater than 10) providing the coil is designed for maximum power transfer with the load. Loads smaller than the maximum power transfer load can result in a change in pickup resonant frequency.

### 2.2.3. Series vs. Parallel Pickup

It is informative to consider the difference in load power between the two coil topologies. If \( R_L \gg \sqrt{L_2/C_2} \), then \( \omega \approx 1/\sqrt{C_2 L_2} \) for the parallel-tuned pickup. Noting the following,

\[ L_2 = \frac{\omega L_2 R_2}{R_2} = \frac{Q_2 R_2}{\omega} \] \hspace{1cm} (2-25)

\[ C_2 = \frac{1}{\omega^2 L_2} = \frac{1}{\omega Q_2 R_2} \] \hspace{1cm} (2-26)

the equation for parallel-tuned load power from Table 2.1 can be modified by substituting (2-25) and (2-26) to give,

\[ P_{RL} = \frac{(I_1 \omega M)^2}{2} \frac{R_L}{(Q_2 R_2 + R_L/Q_2)^2} = \frac{P_{RL_{\text{series}}}}{(Q_2 R_2 + R_L/Q_2)^2} \] \hspace{1cm} (2-27)

If \( R_L = \alpha R_2 \), (2-27) can be rewritten as,

\[ \frac{P_{RL_{\text{parallel}}}}{P_{RL_{\text{series}}}} = \frac{(R_2 + \alpha R_2)^2}{(Q_2 R_2 + \alpha R_2/Q_2)^2} = \frac{R_2^2(1 + \alpha)^2}{R_2^2(Q_2 + \alpha/Q_2)^2} = \frac{(1 + \alpha)^2}{(Q_2 + \alpha/Q_2)^2} \] \hspace{1cm} (2-28)

For the parallel power to be greater than the series power,

\[ \frac{P_{RL_{\text{parallel}}}}{P_{RL_{\text{series}}}} > 1 \therefore \frac{(1 + \alpha)^2}{(Q_2 + \alpha/Q_2)^2} > 1 \] \hspace{1cm} (2-29)

\[ \therefore (1 + \alpha) > (Q_2 + \alpha/Q_2) \] \hspace{1cm} (2-30)

which can be re-arranged in terms of \( \alpha \) to give the condition for greater power from the parallel-tuned coil,
\[ \alpha > Q_2 \quad (2-31) \]
\[ \therefore R_L > \omega L_2. \quad (2-32) \]

This states that the secondary inductor reactance must be larger than the load for parallel tuning to provide more power than series tuning. If the load is less than this the series-tuned coil will provide more power. Coils with large inductances will tend to suit small loads while coils with small inductances tend to suit large loads.

\( N_{2p_{\text{max}}} \) from Table 2.1 is the number of coil turns needed for maximum power transfer to a given load based on \( R_0 \) and \( L_0 \) [68], [78]. For a series-tuned and parallel-tuned pickup with coils of the same cross sectional area and geometry, a different number of turns is needed to match the pickup with the load. The ratio of the number of turns needed for a series coil to number of turns for a parallel coil is,

\[
\frac{N_{2-\text{series}}}{N_{2-\text{parallel}}} = \sqrt{1 + \frac{\omega^2 L_{20}^2}{R_{20}^2}} = \sqrt{1 + Q_2^2} \quad (2-33)
\]

where \( Q_2 = \omega L_{20}/R_{20} \) is the quality factor of the coil. This can be rearrange to give,

\[
N_{2-\text{series}} = \sqrt{1 + Q_2^2} N_{2-\text{parallel}}. \quad (2-34)
\]

This indicates the number of turns needed to match a series coil to a load will always be larger than the number needed to match a parallel coil to a load. (2-34) also holds true for tightly coupled coils.

For a large load and small \( R_{20} \), a series-tuned pickup will need a large number of turns, thus a parallel-tuned pickup may be more appropriate. For smaller loads, the parallel-tuned pickup may require less than one turn which is impractical to design. In this case a series-tuned pickup may be more appropriate. The test coil shown Figure 2.6 was fabricated to extract practical \( L_0 \) and \( R_0 \) values for an example of a small, implantable sized coil. It uses a ferromagnetic core and has an inductance of \( L_2 = 1.87 \mu H \) and winding resistance of \( R_2 = 0.48 \Omega \). Figure 2.7 shows the relationship between the number of turns \( N_{2p_{\text{max}}} \) and \( R_L \) for both series and parallel-tuned pickups having a Q of 14.5 at 600KHz. For the 20Ω – 100Ω range of load resistances required for pressure monitoring (outline in chapter 1), a parallel-tuned coil is more appropriate. A 100Ω load matched with parallel resonance would require 9 turns. The series-tuned pickup would require a coil with an unwieldy 127 turns. Decreasing \( Q \) would lower the number of turns for maximum power transfer but would also lower \( P_{R_{L_{\text{max}}}} \)
itself. The voltage boost provided by the parallel-tuned secondary along with the more practical coil designs for the loads of interest lead to the parallel-tuned coil being favoured for the design of the pressure monitor.

![Test case coil with 9 turns of three parallel wires around a ferromagnetic core.](image)

**Figure 2.6:** Test case coil with 9 turns of three parallel wires around a ferromagnetic core.

![Number of turns required to maximise power transfer for series and parallel-tuned coils with a Q factor of 14.45 at 614KHz.](image)

**Figure 2.7:** Number of turns required to maximise power transfer for series and parallel-tuned coils with a Q factor of 14.45 at 614KHz.
2.3. Parallel Pickup Losses and Efficiency

The parallel-tuned pickup will power a pressure monitoring telemeter. The telemeter is an active device and, as such, it does not provide a constant load. This section will formulate equations for the load power, winding losses and secondary efficiency as a function of the load. This will give an understanding of how the pickup will perform over a range of conditions. In the following derivations, all of the effects from the primary are separated out and included in the open-circuit voltage $V_{OC}$. As a well-designed coil for IPT will have a high quality factor in general, the following equations will be derived assuming $\omega \approx 1/\sqrt{L_2 C_2}$.

If the pickup is set up such that $C_2 = 1/\omega^2 L_2$, the power dissipated in the load resistance can be calculated from Figure 2.8. The load voltage is,

$$V_{RL} = V_{OC} \frac{(R_L/(1 + j\omega C_2 R_L))}{j\omega L_2 + R_2 + R_L/(1 + j\omega C_2 R_L)}$$

where $V_{OC} = j\omega M I_1$ is the RMS open-circuit voltage and $R_2$ is the winding resistance of the inductor. The load power is shown in Appendix A to be,

$$P_L = V_{OC}^2 \frac{R_L}{R_2^2 + \left(\sqrt{L_2/C_2} + \sqrt{C_2/L_2} R_L R_2\right)^2}. \quad (2-35)$$

The power dissipated in the coil winding resistance can be calculated in a similar way and is,

$$P_{R_2} = V_{OC}^2 \frac{R_2 \left(L_2/C_2 + (R_L + R_2 + R_L^2 R_2 C_2/L_2)^2\right)}{\left(R_2^2 + \left(\sqrt{L_2/C_2} + \sqrt{C_2/L_2} R_L R_2\right)^2\right)^2}. \quad (2-36)$$
The load power and winding losses are plotted in Figure 2.9 for the test case coil from Section 2.2.3 with a Q of 14.5. The coil is matched to a 100Ω load and $V_{oc}$ is set to $0.49V_{rms}$. Figure 2.9 shows the load power decreases as the load resistance decreases below or increases above the matched load. The secondary losses increase with increasing load resistance. It is informative to plot the efficiency of the secondary and see how it behaves as the load resistance is changed. Ignoring rectifier losses, the secondary efficiency is,

$$\eta_2 = \frac{P_L}{P_L + P_{R_2}}. \quad (2-37)$$

Figure 2.9: Load power and winding losses for a parallel pickup matched with a 100Ω load. The voltage $V_{oc}$ is set to $0.49V_{rms}$.

Substituting equations (2-35) and (2-36) into gives the equation for secondary efficiency,

$$\eta_2 = \frac{1}{1 + \frac{R_2}{R_L} \left( \frac{\left( R_L + R_2 + R_2^2 R_2 C_2 / L_2 \right)^2}{R_2^2 + \left( \sqrt{L_2 / C_2} + \sqrt{C_2 / L_2} R_2 R_2 \right)^2} \right)}. \quad (2-38)$$

The efficiency for the test case coil matched to a 100Ω load is shown in Figure 2.10. The maximum efficiency of 88% occurs with a 7Ω load. With a 100Ω load the efficiency is 50%. It is important to note that, although the efficiency is higher, the power delivered to a 7Ω load is approximately 6 times lower than the power delivered to the 100Ω load. In order to get the same power to a 7Ω load, the primary current needs to be tripled, an increase of $\sqrt{6}$.
Figure 2.10: Secondary efficiency against load resistance for a coil tuned to match a 100Ω load.

The efficiency curve can be understood by looking at the two extremes of zero load resistance and infinite load resistance presented in Figure 2.11. With zero load resistance, no power can be dissipated in the load. With infinite load resistance, all current flows through $R_2$ and $C_2$ and no power is dissipated in $R_L$. Under both cases the efficiency is zero.

Figure 2.11: Parallel-tuned pickup with infinite load and zero load.

2.4. Rectifier Topologies

A rectifier converts AC power into DC power. Rectifiers can be designed to convert an AC current into a DC supply or an AC voltage into a DC supply. The parallel-tuned pickup acts as a voltage source and hence only rectifiers working with voltage source inputs are investigated.
2.4.1. Diodes and Switches

Rectification is normally achieved with semiconductor diodes or switches shown in Figure 2.12. Diodes have the advantage of being self-commutating, and a rectifier can easily be implemented using them. They allow current flow in one direction and block reverse flow. All diodes have a forward voltage drop $V_{FW}$ of about 0.7$V$ for P-N junction diodes and 0.45$V$ for Schottky diodes [68]. The anode of the diode must be higher than the cathode by $V_{FW}$ for the diode to start conducting. Diodes also have an internal resistance. Often the $V_{FW}$ is specified at a range of currents to account for the resistance. The main sources of power loss in diodes are the $IV_{FW}$ losses and any $I^2R$ losses. Discharging of the diffusion capacitances within a p-n diode results in a reverse recovery current [68]. Reverse recovery limits the efficiency of the diodes at high frequencies. Schottky diodes do not have reverse recovery currents to the same extent as P-N junction diodes [68].

![Figure 2.12: Diode and MOSFET.](image)

Semiconductor switches prevent current flow while turned off and allow current flow when turned on. Metal oxide semiconductor field effect transistors (MOSFETs) are the most appropriate switch for low voltage, high frequency applications [81]. They do not have the forward voltage drop of diodes but require active circuitry to control them. MOSFETs are controlled with the gate voltage. Losses in semiconductor switches are due to:

1. $I^2R$ losses with the on-resistance of the switch.
2. Switching losses. For MOSFETs, the gate capacitance must be charged and discharged each time the switch is turned on. The power lost from this increases linearly with frequency.
3. Control Power. Some active circuitry (comparators, op-amps etc) is required to control and drive the switches.

A common figure of merit for a MOSFET is the gate charge multiplied by the on-resistance,

$$FOM = R_{DS(on)}Q_G$$

(2-39)

where the gate charge $Q_G = C_G V_{GS}$. FOM gives insight into both resistive and switching losses for a MOSFET at a given gate drive voltage. Most MOSFETs have an internal diode that is intrinsically part of their design.
2.4.2. **Half Wave Rectifier**

The simplest rectifier is the half wave diode rectifier depicted in Figure 2.13. A diode in series with a voltage source allows current to flow in only one direction. When $V_{in}$ is greater than $V_{RL}$ by the diode forward voltage $V_{FW}$, current flows form the source to the load. The filtering capacitor $C_f$ stores the charge increasing $V_{RL}$. During the remainder of the cycle the load is powered from the filter capacitor.

Diodes are nonlinear devices making accurate calculation of losses a complex task. However, the impact of forward voltage on rectifier efficiency can be understood with a simplified model of losses. Neglecting series resistance, an approximation of the half wave diode rectifier efficiency is [68],

$$\eta_{rec} = \frac{V_{DC}}{V_{DC} + V_{FW}}$$

(2-40)

where $V_{DC}$ is the average output voltage,

$$V_{DC} = \frac{1}{2\pi} \int_0^{2\pi} V_{RL} d(\omega t).$$

(2-41)

With low output voltages, $V_{FW}$ can have a large impact on the rectifier efficiency. The effect of rectifying the output changes the effective impedance seen by the pickup. The equivalent input impedance of the rectifier can be shown to be [68],

$$R_{LEQ} = \frac{R_L}{2} \left(1 + \frac{V_{FW}}{V_{DC}}\right).$$

(2-42)

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![Diagram of a half wave diode rectifier](image.png)

**Figure 2.13:** Half wave diode rectifier. $V_{FW}$ shown as 0V.
2.4.3. **Full Wave Bridge Rectifier**

Compared with the half wave rectifier, the full wave rectifier of Figure 2.14 conducts on both the positive and negative peaks of the input voltage. The ripple is half that of the half wave rectifier assuming $C_f R_L$ are the same for both. As the current now flows through two diodes, the forward voltage drop is doubled.

A similar approximation for the full wave bridge rectifier efficiency can be made [68],

$$
\eta_{rec} = \frac{V_{DC}}{V_{DC} + 2V_{FW}}. \quad (2-43)
$$

The equivalent input impedance of the rectifier is [68],

$$
R_{LEQ} = \frac{R_L}{2} \left(1 + \frac{2V_{FW}}{V_{DC}}\right). \quad (2-44)
$$

![Figure 2.14: Full wave diode bridge rectifier. $V_{FW}$ shown as 0V.](image)

Small, full wave Schottky diode rectifiers ranging from 5mm by 6mm in size to 1.2mm by 2mm in size can have forward voltage drops as low as 210mV to 800mV with currents of 100mA [82]–[84]. With a 3.45V load voltage, the efficiency of the full wave rectifier could range from 89% to as low as 68% depending on the rectifier size and power requirements.
2.5. Active Diode Synchronous Rectifier

This section will describe in detail the operation of the active diode synchronous rectifier (ADSR). Details such as switching frequency, delay and hysteresis will be discussed. Efficiency estimates based on switch resistance and gate capacitance are developed.

2.5.1. Operation and Load Power

An active diode rectifier requires circuitry to control the switches based on the input voltage. The control block from Figure 2.15 senses when the voltage \((v_{in+} - v_{in-})\) is larger than \(V_{DD}\) and shorts \(v_{in+}\) to \(V_{DD}\) and \(v_{in-}\) to ground by turning on \(N_2\) and \(P_1\). Similarly, when \((v_{in-} - v_{in+})\) is larger than \(V_{DD}\), \(N_1\) and \(P_2\) are turned on. This results in behaviour similar to the diode full wave bridge rectifier. If \(C_f\) is large enough that the ripple in \(V_{DD}\) is negligible, the average power delivered to the load is \(P_{load} = i_{ave} V_{DD}\). Assuming a sinusoidal input voltage and no offset in the comparator, \(i(t) = (V_i \sin(\omega t) - V_{DD})/R_s\) for,

\[
\left(n\pi + \sin^{-1}\left(\frac{V_{DD}}{V_i}\right)\right) < \omega t < \left((n + 1)\pi - \sin^{-1}\left(\frac{V_{DD}}{V_i}\right)\right)
\]

where \(V_i = V_{in+} - V_{in-}\) and \(n\) is an integer that increases each half cycle.

\[
i_{ave} = \frac{\omega}{R_s \pi} \int_{T_1}^{T_2} V_i \sin(\omega t) - V_{DD} \, dt
\]

\[
i_{ave} = \frac{V_i}{R_s} (\frac{-2\cos(\arcsin(V_{DD}/V_i))}{\pi R_s} - \frac{V_{DD}}{\pi R_s} (\pi - 2 \arcsin\left(\frac{V_{DD}}{V_i}\right)))
\]

\[
P_{load} = \frac{2V_i V_{DD}}{\pi R_s} \sqrt{1 - \left(\frac{V_{DD}}{V_i}\right)^2} - \frac{V_{DD}^2}{\pi R_s} (\pi - 2 \arcsin\left(\frac{V_{DD}}{V_i}\right))
\]

\[\text{(2-45)}\]

\[\text{(2-46)}\]

2.5.2. Losses

Losses in the active diode rectifier can be broken down into resistive losses, switching losses and control losses. The average resistive power loss is shown in Appendix B to be,

\[
P_{loss-ave} = \frac{V_i^2}{2\pi R_s} \left(\pi - 2 \arcsin\left(\frac{V_{DD}}{V_i}\right)\right) - \frac{3V_i V_{DD}}{\pi R_s} \left(\sqrt{1 - \left(\frac{V_{DD}}{V_i}\right)^2}\right)
\]

\[
+ \frac{V_{DD}^2}{\pi R_s} \left(\pi - 2 \arcsin\left(\frac{V_{DD}}{V_i}\right)\right).
\]

\[\text{(2-47)}\]
The average load and resistive loss power are plotted below in Figure 2.16 for an $R_S$ of 0.5Ω. The average load power and loss power both increase with the difference between $V_I$ and $V_{DD}$. The load power also increases with $V_{DD}$ whereas the power loss decreases slightly.

Figure 2.16: Load power and power loss for an active diode synchronous rectifier with zero offset and hysteresis and a voltage source input as a function of $V_{DD}$ and $V_I - V_{DD}$. 

Figure 2.15: Active diode rectifier circuit diagram and waveform.
Switching losses, $P_{SW}$, are a function of frequency and gate capacitance,

$$E_S = \frac{1}{2} C_G V_{GS}^2$$

$$\therefore P_{SW} = \frac{1}{2} C_G V_{GS}^2 f$$

where $C_G$ is the total gate capacitance of all transistors, $V_{GS}$ is the gate voltage the transistor is charged to and $f$ is the frequency of the input waveform. As zero voltage switching is being used, the MOSFET output capacitance is neglected. In contrast to the switch resistance losses, the switching losses increase linearly with transistor width and increase at the square of the gate drive voltage.

For minimum power loss there are two contrasting criteria:

1. Maximise $W$ and $V_{GS}$ to minimise resistive losses.
2. Minimise $W$ and $V_{GS}$ to minimise switching losses.

For each frequency and current there is an optimum transistor size that minimises the combination of resistive and switching losses,

$$P_{\text{loss}} = i(t)^2 R_s + \frac{1}{2} V_{GS}^2 f C_G.$$  

The control block will draw a constant power which is usually negligible compared with the other losses. However, when the load power is on the same order of magnitude as the constant control loss, the rectifier efficiency will be low. Regardless of the efficiency at low power levels, the total power loss and heating will be much lower than while operating at typical power levels. A larger source of control loss is the switching delay loss. The control circuitry that drives the rectifier transistors will have an inherent delay $t_d$. The delay leads to the rectifier transistors switching on and off later than intended resulting in a reverse current shown in Figure 2.17 from the filtering capacitor back to the pickup [69], [73]. This should not be confused with switching losses in hard switched converters. The delay decreases efficiency as there are additional $I^2R$ losses for the reverse current. Switching delay losses become more pronounced as the WPT frequency increases.

---

$^4$ $C_G$ is the total gate capacitance because all gates are charged once per cycle.
2.5.3. Efficiency

The power conversion efficiency of the rectifier ignoring switching losses is,

\[ PCE = \frac{P_{\text{load}}}{P_{\text{load}} + P_{\text{loss}}} \]  \hspace{1cm} (2-51)

and is shown in Figure 2.18. The efficiency decreases with the voltage difference between \( V_I \) and \( V_{DD} \) and slightly increases with \( V_{DD} \). Substituting (2-46) and (2-47) into the equation for PCE gives,

\[ PCE = \frac{2V_I V_{DD} \sqrt{1 - (V_{DD}/V_I)^2} - V_{DD}^2 \left( \pi - 2 \arcsin \left( \frac{V_{DD}}{V_I} \right) \right)}{\frac{V_I^2}{2} \left( \pi - 2 \arcsin \left( \frac{V_{DD}}{V_I} \right) \right) - V_I V_{DD} \sqrt{1 - (V_{DD}/V_I)^2}}. \]  \hspace{1cm} (2-52)

Efficiency of Active Rectifier with Sinusoidal Input Voltage Neglecting Switching Losses

![Figure 2.18: Efficiency for an active diode synchronous rectifier as a function of \( V_{DD} \) and \( V_I - V_{DD} \). The rectifier has zero offset and hysteresis and has a voltage source input.](image-url)
Including switching losses, the efficiency is,

\[
PCE = \frac{2V_I V_{DD} \sqrt{1 - \left(\frac{V_{DD}}{V_I}\right)^2} - V_{DD}^2 \left(\pi - 2 \arcsin \left(\frac{V_{DD}}{V_I}\right)\right)}{V_I^2 \left(\pi - 2 \arcsin \left(\frac{V_{DD}}{V_I}\right)\right) - V_I V_{DD} \sqrt{1 - \left(\frac{V_{DD}}{V_I}\right)^2} + \pi R_S \frac{1}{2} V_{DD}^2 f C_g}.
\] (2-53)

To gain an understanding the efficiency including switching losses, PCE is plotted for transistors with a FOM (figure of merit \(R_S Q_G\)) of 280\(\mu\)Ω\(C\) at 3.3\(V\). \(V_{DD}\) is set to 3.3\(V\) as is \(V_{GS}\). \(V_I\) and \(R_S\) are varied and \(PCE\) is plotted against load power. For each load power in Figure 2.19 there is an optimum switch resistance and hence transistor with that minimises the combination of resistive and switching losses. The active rectifier should be designed to operate over a load power range specified by the target load range. The IPT frequency dictates how severe the switching losses are. Selecting an IPT frequency is therefore a compromise between the desire to increase \(\omega\) to maximise \(\omega^2\) in the link equations (see \(P_{RLmax}\) in Table 2.1 for instance) and the frequency dependent losses in the rectifier.

![Active Diode Synchronous Rectifier Efficiency with Load Power and Switch Resistance](image)

Figure 2.19: Active diode synchronous rectifier efficiency with load power and switch resistance. Switching losses decrease the efficiency at low load powers, and resistive losses decrease the efficiency at higher powers.
2.5.4. Current Spikes and Reduction Techniques

A key design consideration for an active diode rectifier is the peak current spikes. Due to the comparator offset, when the transistors are switched on the input voltage is $V_{off}$ higher than the output voltage. With delay due to the comparators the offset can be larger. The pickup capacitor $C_2$ discharges into $C_L$ across the switch resistance of the transistors. With an offset of 400mV and switch resistance of 250mΩ this would result in spikes of 1.6A through the rectifier. Reducing these spikes lowers the likelihood of damaging the switches and risk of electro-migration, a phenomenon that can lead to metal traces breaking down over time due to excessive current densities [85]. Lowering the voltage offset would make the comparators more susceptible to false triggering from noise. Increasing the switch resistance would decrease the peak current but decrease the efficiency of the rectifier. By breaking the current into current from the pickup inductor $I_{L_2}$ and current from the pickup capacitor $I_{C_2}$ the effect of increasing $R_S$ can be found. To simplify the analysis, the load is approximated as a voltage source. This assumption is accurate providing the capacitor $C_L$ is large enough that the output voltage does not change much during each rectifier period. The current discharge can be modelled as a charged capacitor being connected in series with a resistor and filter capacitor. The current from the capacitor discharge is,

$$I_{spike} = \frac{V_{off}}{R_S} e^{-\frac{t}{C_S R_S}}$$

(2-54)

where $V_{off} = V_A - V_{DD}$ is the offset voltage across the switch, $R_S$ is the switch resistance and $C_S = C_2 C_L / (C_2 + C_L)$ is the combined series capacitance of the pickup and filter capacitors. $C_S \cong C_2$ if the output capacitor is large.

The efficiency of the current coming from an inductor is,

$$\eta_{L_2} = \int_T^{2T} \frac{P_{out-L}(t)}{P_{out-L}(t) + P_{R_S}(t)} dt = \int_T^{2T} \frac{i_{L_2}(t)V_{DD}}{i_{L_2}(t)V_{DD} + i_{L_2}^2(t)R_S} dt$$

(2-55)

$$= \int_T^{2T} \frac{V_{DD}}{V_{DD} + i_{L_2}(t)R_S} dt = \frac{V_{DD}}{V_{DD} + I_{L_2}R_S}.$$ 

As $I_{L_2-ave} = V_{DD}/R_{LE} - I_{C_2-ave}$ where $R_{LE}$ is the effective load resistance, (2-55) can be re-written as,

$$\eta_{L_2} = \frac{V_{DD}}{V_{DD} + (V_{DD}/R_{LE} - I_{C_2-ave})R_S} = \frac{R_L}{R_{LE} + R_S - I_{C_2-ave}R_S/I_{L-ave}}.$$ 

(2-56)

If there was no capacitor the efficiency would be,
\[ \eta_{Lz} = \frac{R_L}{R_L + R_S} \]  

(2-57)

Efficiency decreases with smaller loads and, as expected, increasing switch resistance. The efficiency of current coming from a capacitor is best found in terms of energy. The energy transferred from \( C_2 \) is,

\[ E_{C_2} = \frac{1}{2} C_2 (V_{DD} + V_{off})^2 - \frac{1}{2} C_2 V_{DD}^2 \]

\[ = \frac{1}{2} C_2 (V_{off}^2 + 2V_{off}V_{DD}) \]  

(2-58)

The energy delivered to the output is approximately,

\[ E_{out} = \int_0^\infty I_{spike}V_{out} = \frac{V_{off}V_{out}}{R_S} e^{-\frac{t}{C_2R_S}} = V_{off}V_{out}C_2. \]  

(2-59)

Using (2-57) and (2-59) the efficiency for the current from the capacitor is,

\[ \eta_{C_2} = \frac{E_{out}}{E_{C_2}} = \frac{V_{DD}}{V_{DD} + V_{off}/2}. \]  

(2-60)

The efficiency changes with the offset voltage and is independent of the switch resistance. This is due to redistribution loss \[ [86] \] that will always occur when capacitors with different voltages are connected in parallel.

A design strategy could be to define a peak current limit \( I_{lim} \) and setting \( R_S = V_{off}/I_{lim} \). This would maximise the efficiency while keeping the peak current below a safe limit. However, because the switches are transistors, the switch resistance can be varied. The initial switch resistance can be held at \( R_S = V_{off}/I_{lim} \). As \( V_{off} \) drops, \( R_S \) can be decreased to maintain the current as close to \( I_{lim} \) as possible. This would require a feedback amplifier to control the gate drive voltage on the switching transistors. The power drawn would need to be lower than the power gained by the increase in efficiency from controlling \( R_S \). An alternate strategy is to use a soft turn on for the transistors. By correctly sizing the inverter driving the pass transistor, the pass transistor can be turned on gradually. The resistance of the pass transistor will initially be large but will decrease as the gate voltage increases. This compromise can keep the current below \( I_{lim} \) as shown in Figure 2.20.

The soft turn on does not affect the efficiency of the power from the capacitor and only decreases the efficiency of power from the inductor for the duration of the soft turn on.
Chapter 2  Structure of the Power Link

Representation of $i_C$, $i_L$ and $i_{total}$

Figure 2.20: Representation of the periodic current from the pickup capacitor, pickup inductor and total current through rectifier with a) normal transistor turn on and b) soft transistor turn on.

Figure 2.21 shows how the simulated efficiency and peak current change as the rise time of the soft start increases for a rectifier with a 500$m\Omega$ switch resistance, offset voltage of 150$mV$ and using the test case coil. The efficiency decreases by about 1% from a rise time of 7.5$nS$ to 50$nS$. Over the same range, the peak current decreases approximately 100$mA$. The efficiency with rise times below 10$nS$ levels off due to larger switching losses due to shoot through from driving the inverter. The ideal rise time depends on the coil setup and operating frequency. Parasitic inductances from the PCB will reduce the current spikes further.

Figure 2.21: Effect of changing the pass transistor turn on rise time on efficiency, peak current and load power.
2.6. Voltage and Power Flow Control Strategies

The rectifier by itself cannot control the output voltage. In the ideal set up, the power supplied by the pickup will exactly match the power consumed by the rectifier and load at the desired output voltage. In a practical system, the supplied power and load power will never perfectly match resulting in two cases:

1. Case 1: Power supplied by the pickup is less than the power needed by the load. This results in the monitoring device shutting off as the telemetry circuitry would not have enough power to run. This case could occur when:
   a. The coupling between the primary and secondary decreases due to a change in distance or alignment.
   b. The load increases. This could occur if additional measurements are being taken, more data is being transmitted, etc.

2. Case 2: Power supplied by the pickup is greater than power needed by the load. This increases the voltage at the output of the rectifier. If the voltage increases above the safe operating voltage of the circuitry, the circuitry will be damaged. This case could occur from:
   a. A change in alignment or decrease in distance between the primary and secondary coil which increases coupling.
   b. The load decreasing. This could occur if the pressure monitor goes into shut down or reduces the sensing and data rate.

Of the two cases, the second is more concerning as it could result in permanent damage or failure of the pressure monitor. A method of controlling the power supplied to the load is needed. The following section introduces methods for managing the power across the inductive link.
2.6.1. **Primary Based Power Control**

The most effective way of managing the power link is by making it a closed loop system like Figure 2.22. The voltage induced in the secondary coil is $V_{oc} = j\omega MI_1$. By monitoring $V_{OUT}$ at the secondary, a feedback signal can be transmitted to the primary to increase or decrease $I_1$ or $\omega$ as necessary [87][88]. This is the ideal situation where the power induced in the secondary is maintained equal to the power required by the load despite changes in coupling or the load itself. This strategy ensures excess power is not dissipated in the secondary circuit. However, a wireless feedback loop has a finite latency and data rate limiting the response to sudden changes in load and coupling. A sudden load variation could damage the implant by overpowering it. For a medical implant placed under the skull, the power link must be robust to any unforeseen conditions.

![Diagram](image)

**Figure 2.22: Wireless feedback loop of primary and secondary.**

It is impossible to guarantee a fail-safe wireless link between the primary and secondary for the lifetime of an implantable device. Close proximity of a primary with an incompatible feedback loop or jamming of the feedback frequency could result in feedback loop failure. Therefore, it is desirable to have an additional method of managing the power transferred to the secondary that is independent of the primary.

2.6.2. **Secondary Based Power Control**

The simplest way to prevent over-voltages in the secondary would be to shunt additional power through a variable load, e.g. a Zener diode or a transistor as in Figure 2.23. While this prevents over-voltage, it also increases the power dissipated within the implant creating additional heating.
Detune control is another method of managing the power transfer to the secondary. A detune capacitor, $C_d$, from Figure 2.24, can be switched in parallel with the pickup capacitor of the secondary [89]. By changing the capacitance, the operating point of the pickup changes and is no longer matched with the load and the pickup resonant frequency is no longer matched to the WPT frequency. This decreases the power delivered to the load. By switching the additional capacitor in and out, the output voltage can be maintained within the desired limits. Under this configuration the power dissipated in the load remains constant and no power is directly shunted to waste heat.

\[
C_{eq} = C_2 \left( 1 + \frac{1}{Q_L} \sqrt{\left( \frac{Q_L}{k} \right)^2 - 1} \right) \quad (2-61)
\]

where $C_{eq} = C_2 + C_d$, $Q_L = R_L/\omega L_2$, $k = V_o/V_{OC}$ and the coil losses are assumed to be zero. This can rearranged to give the necessary detune capacitance to maintain the output voltage with a variation in $V_{OC}$ or $R_L$. 

---

**Figure 2.23:** Output voltage control though power shunting.

**Figure 2.24:** Detune control. $V_{out}$ is managed by using a detune capacitor to change the pickup resonance frequency and decrease the input power.
Chapter 2  
Structure of the Power Link

\[ C_d = C_2 \frac{1}{Q_L} \sqrt{\left(\frac{Q_L}{k}\right)^2 - 1}. \]  

(2-62)

Under normal conditions \( C_d = 0 \) and \( k = Q_L \). If \( V_{OC} \) were to increase by a factor \( \alpha \) due to coupling, \( k = Q_L / \alpha \) and hence,

\[ C_d = C_2 \frac{1}{Q_L} \sqrt{\alpha^2 - 1}. \]  

(2-63)

A doubling of \( V_{OC} \) would require \( C_d = C_2 \sqrt{3} / Q_L \). For the test case coil, ignoring the coil losses, the equivalent capacitance to keep the output voltage constant with a doubling of \( V_{OC} \) is \( \approx 0.12C_d \). In practice, the detune capacitor can be lower than this due to the presence of coil losses.

Practically, the switch that attaches the detune capacitor in parallel with the pickup limits the effectiveness of detune control. A limit will be reached where increasing \( C_d \) does not decrease the output voltage unless the switch resistance is reduced. At extreme cases \( C_d \) would be large enough that the switch resistance dominates. A plot of the voltage reduction with different detune capacitances is shown in Figure 2.25 for the test case coil. The switch resistance has been included and can be seen to reduce the effectiveness of detune control at large capacitances.

![Figure 2.25: Detune control for the test case coil matched to a 100Ω load. The detune capacitance is 0nF, 10nF, 100nF and 1µF. Simulations were run with and without 500mΩ switch resistance. The simulations with switch resistance always have a lower peak than without.](image)


2.7. **Shorting Control**

Shorting control is a form of decoupling control that can be used to regulate the output voltage and manage the power delivered to the load [91][92][93]. When the output voltage reaches an upper limit, a switch in parallel with the load is shorted temporarily shunting current from the load. Providing the load is separated from the pickup by a rectifier, the load will continue receiving power from the filter capacitor until the output voltage falls to a set level. The following section will analyse the power loss in the shorting switch and pickup while shorting control is active.

2.7.1. **Shorting Control for Over-voltage protection**

The voltage induced in the secondary coil is $V_{oc} = j\omega M I_1$. At steady state, using the Norton equivalent circuit and ignoring the coil resistance, a loosely-coupled parallel-tuned secondary pickup can be modelled as an AC current source in parallel with a shunt impedance and the load [94] as in Figure 2.26. The current source magnitude is limited by $L_2$ to $I_{IN} = V_{OC}/j\omega L_2 = M I_1/L_2$. Including a switch in parallel with the pickup allows the pickup to be shorted when the voltage becomes too large. Providing the series resistance of the switch $R_S$ is small, most of the current $I_{in}$ will flow through it and only a small amount of power will be dissipated due to $I_{in}^2 R_S$ losses. If a rectifier is inserted before the load, the load is powered by the filter capacitor while the shorting control switch is active. Once the output voltage is below the safe limit, the shorting control switch can be de-activated.

![Figure 2.26: A parallel-tuned pickup can be modelled as a current source in parallel with the pickup. Shorting control uses a switch to bypass the current through the switch resistance.](image)
2.7.2. **Power Losses During Shorting Control**

A major concern while shorting control is active is the amount of power dissipated in the shorting transistors and in the primary coil resistance. The size of the shorting transistors should be large enough to minimise local heating of the transistors themselves and global heating of the implant as a whole.

The amount of power dissipated in the shorting switch of Figure 2.27 depends on the induced voltage in the coil and the pickup parameters. As discussed previously, the pickup is normally designed to have a resonance frequency at the IPT operating frequency. The value of $L_2$ is chosen to match the load resistance for maximum power transfer, maximum efficiency or a compromise between the two. When shorting control is active, the load is disconnected from the pickup by the rectifier and the shorting switch resistance is put in parallel with the pickup.

![Figure 2.27: Pickup, rectifier, load and shorting control model with coil losses.](image)

The plot of the load power and winding losses is repeated in Figure 2.28 for the test case coil matched to a 100Ω load. The power dissipated can be dropped by two orders of magnitude from 120$mW$ at the normal load to 1.2$mW$ by shorting with a 260$m\Omega$ resistance. The winding losses drop by a similar order of magnitude from 120$mW$ to 2.3$mW$.

The output voltage can be regulated even with large input voltages. For a $V_{OC}$ of $1.5V_{rms}$ the load power is 1.12$W$, but only 11.2$mW$ would be dissipated in the shorting transistors. The power dissipated during shorting control is low and will cause minimal heating. The winding losses during shorting control are greatly lower than during rectification. Therefore, shorting control can maintain the output voltage within the voltage band without increasing the power dissipation within the rectifier or coil. Furthermore, large increases in coupling can be managed without the circuitry being damaged.
It is important to note that the amount of power delivered to the shorting transistors depends on the load the pickup is matched to. A pickup matched for maximum power transfer to a 10Ω load and having the same single-turn equivalent values would require a shorting-resistance an order of magnitude lower to get the same reduction in power dissipation. A power plot for the secondary load resistor normalised to the maximum power is a useful tool for understanding the effect different sized shorting-resistances have on the power dissipated for different pickups. From Figure 2.29, two coils with a factor $\beta$ difference in maximum power transfer load will also require shorting-resistances with a factor $\beta$ difference to drop the power transfer by the same magnitude.

Figure 2.28: Load power and winding losses for a parallel pickup tuned to a 100Ω load. The voltage $V_{oc}$ is set to $0.49V_{rms}$.

Figure 2.29: Normalised power delivered to a resistor in parallel to the pickup for a 100Ω load (solid line) and 10Ω load (dashed line).
2.7.3. Shorting Control for Improved Secondary Pickup Efficiency

As the load draws power from $C_f$, $V_{R_L}$ drops. The switch is reopened once $V_{R_L} = V_{th-}$, the lower load voltage limit. If $C_f$ is sufficiently large, the duration the shorting switch is active will contain many IPT periods, and the transient losses from discharging $C_2$ become negligible. In the practical circuit, the current spikes from discharging $C_2$ can be managed using a soft turn on of the rectifier and shorting control switches.

The duration the shorting control switch is open with respect to closed can be found from the time it takes to charge and discharge the load capacitor. The off duration for the shorting control switch $t_{SC,off}$ can be approximated to,

$$t_{SC,off} = \frac{C_f V_H}{(I_{out,off} - I_{R_L})}$$

(2-64)

where $C_f$ is the filter capacitance, $V_H = V_{th+} - V_{th-}$ is the shorting control hysteresis, $I_{out,off}$ is the average rectifier output current while shorting control switch is off and $I_{R_L}$ is the mean load current. The on duration for the shorting control switch is the time to discharge the capacitor,

$$t_{SC, on} = \frac{C_f V_H}{I_{R_L}}$$

(2-65)

As shorting control maintains approximately constant $I_{R_L}$, $t_{SC, on}$ is also constant. Selecting $C_f$ of appropriate size ensures $t_{SC, on}$ is much longer than the IPT period. The off to on duty ratio for the shorting control switch is then,

$$D = \frac{t_{SC, off}}{t_{SC, on} + t_{SC, off}} = \frac{I_{R_L}}{I_{out, off}}$$

(2-66)

The duty ratio represents the proportion of time the shorting control switch is open and the rectifier is active. As the output current from the rectifier increases relative to the load current, the shorting switch is closed more frequently and for a longer period, rectification is active less and the duty ratio decreases.

For a fixed load, maintaining a constant output voltage with SC also maintains a constant output current. Therefore, the mean load current is,

$$I_{R_L} = V_{R_L}/R_L.$$ 

(2-67)
As no current is delivered to the load and filter capacitor while the shorting switch is on, the rectifier output current during rectification has to be greater than the average load current. Substituting (2-67) into (2-66) and rearranging gives,

\[ I_{\text{out,off}} = \frac{V_{RL}}{(DR_L)} = \frac{V_{RL}}{R_{L,\text{eff}}} \]  

(2-68)

where \( R_{L,\text{eff}} = DR_L \) is the effective DC load during rectification. The effective AC load is smaller than the effective DC load by the impedance transform ratio of the rectifier \( \alpha \),

\[ R_{L,\text{AC}} = \alpha R_{L,\text{eff}} \therefore I_{\text{out,off}} = \alpha V_{RL}/R_{L,\text{AC}}. \]  

(2-69)

While rectification is active, \( I_{\text{out,off}} \) in (2-69) can be substituted into (2-35) as \( P_{RL} = I_{\text{out,off}} V_{RL} \) resulting in,

\[ \frac{\alpha V_{RL}^2}{R_{L,\text{AC}}} = \frac{V_{OC}^2 R_{L,\text{AC}}}{R_2^2 + (\sqrt{L_2/C_2} + \sqrt{C_2/L_2} R_{L,\text{AC}} R_2)^2}. \]  

(2-70)

Rearranging and solving for \( R_{L,\text{AC}} \) gives a definition in terms of \( V_{OC} \),

\[ R_{L,\text{AC}} = \frac{\alpha V_{RL}^2 R_2}{\alpha V_{RL}^2 C_2 R_2^2/L_2 - V_{OC}^2} \left( 1 + \frac{1 - (\alpha V_{RL}^2 C_2 R_2^2/L_2 - V_{OC}^2)(R_2 + L_2/C_2)}{\alpha V_{RL}^2 R_2} \right). \]  

(2-71)

\( P_{RL} \) and \( P_{R_2} \) can then be found by substituting (2-71) back into (2-35) and (2-36). To simplify the following analysis, \( \alpha = \eta_{\text{rec}}0.5 \) is approximated where \( \eta_{\text{rec}} \) is the rectifier efficiency. This assumption is justified as,

\[ P_{RL,DC} = \eta_{\text{rec}} P_{RL,\text{AC}} \therefore \frac{V_{RL,DC}^2}{R_L} = \eta_{\text{rec}} \frac{V_{RL,\text{AC}}^2}{R_{L,\text{AC}}} \Rightarrow R_{L,\text{AC}} = \frac{\eta_{\text{rec}} V_{RL,\text{AC}}(\text{peak})^2}{2V_{RL,DC}^2} R_L. \]  

(2-72)

If the voltage drop across the rectifier is small, \( V_{RL,\text{AC}}(\text{peak}) \approx V_{RL,DC} \) and the approximation is justified.

An increase in \( V_{OC} \) decreases the effective load seen by the pickup. This load decrease shifts the secondary matching from maximum power transfer towards maximum efficiency. Ideally, zero power would be dissipated while the shorting control switch is on resulting in the dashed efficiency curve presented in Figure 2.30. As the effective load drops, the efficiency increases until maximum efficiency is reached. This is consistent with the efficiency curve shown in Figure 2.10. In practice, some power is dissipated during shorting control and depends on the duty cycle.
The average load power $P_{RL}$ will be constant regardless of the duty cycle as the load voltage is regulated. Ignoring rectifier losses, the total efficiency of the secondary pickup with shorting control is,

$$
\eta = \frac{P_{RL}}{(P_{RL} + P_{Rz,off}D + P_{SC}(1 - D))}
$$

(2-73)

where $P_{Rz,off}$ is the coil loss during rectification and $P_{SC}$ is the total power loss during shorting control including coil winding and shorting switch losses. These can be calculated from (2-35) and (2-36). The effective AC load and secondary side efficiency with shorting control are shown in Figure 2.30 for a 100Ω AC load. With a 100% duty cycle, shorting control is never active, so the effective load is the real 100Ω AC load. As the open-circuit voltage increases, the duty cycle decreases and the effective load drops. The change in effective load moves the operating point away from the maximum power point and towards the maximum efficiency point. Shorting control losses affect the efficiency most at low duty cycles causing it to deviate from the ideal efficiency curve. This is intuitive as the output power will remain constant as $V_{OC}$ increases, but the shorting control losses will be larger and present for a greater proportion of the duty period.

Figure 2.30: a) Effective load impedance as input voltage increases but output voltage remains $V_{avg}$. b) The efficiency of the secondary including and excluding losses during shorting control. The duty cycle of the rectifier is proportional to the effective load.
2.7.4. **Shorting Control vs Detune Control**

Shorting control can regulate the output voltage of the rectifier and transform the apparent load between the coil’s maximum power transfer point and maximum efficiency point as needed. The sudden changes in load when shorting occurs can be difficult to manage at the primary. For a loosely-coupled link this problem is less significant than for a tightly-coupled link.

Detune control can regulate the output voltage by changing the resonant frequency of the pickup. For small to moderate changes in open-circuit voltage, detune control is an effective method of regulating the output voltage. The changes in loading presented to the primary coil are much smaller than in shorting control. However, for large variations in open-circuit voltage, large detune capacitors are needed and the effectiveness of detune control is effectively limited by the resistance of the switch connecting the detune capacitor in parallel with the pickup.

As shorting control only needs transistors whereas detune control requires a capacitor in addition to transistors, shorting control also gives a smaller circuit. Therefore, shorting control is used for voltage regulation and power management in the implant.

2.8. **Discrete Implementation vs. Integrated Implementation**

A full wave diode bridge rectifier can be implemented with four diodes. Normally, a single package containing four Schottky diodes can be used. However, the efficiency of the rectifier is limited at low output voltages by the forward voltage drop.

Implementing an active diode synchronous rectifier using discrete circuitry requires four transistors, a minimum of two comparators to control them and any additional circuitry required to set the correct comparator threshold voltages. Often, packages containing two transistors are available so only two packages will be needed for all rectifier transistors. Comparators with propagation delays in the 10nS range require relatively large supply currents above 10mA. Generally, low propagation delay comparators are not designed to drive the large capacitive loads presented by the rectifier transistor gates, so it would be necessary to include gate drivers. Parasitic PCB trace inductance and capacitance between the
comparators and transistor gates increases delay between the comparators activating and the transistors switching. Minimum delays are critical for efficient operation of the ADSR. Furthermore, the soft start technique for current spike reduction would require additional components to implement and is difficult to achieve without creating additional losses.

Commercial ideal diode bridge controllers similar to ADSRs are available but operate below 600Hz, work at higher voltages and have supply currents in the milliamp range [95].

Shorting control requires a comparator to sense when the output voltage thresholds are reached. A discrete implementation would likely require resistors to set the thresholds. If a full wave diode bridge rectifier was used, two transistors would be required for shorting. The ADSR could use the rectifier transistors for shorting with the addition of a multiplexor or some logic element.

Disregarding resistors and capacitors, a minimum of three (diode rectifier, shorting transistors, shorting control comparator) to six (PMOS transistors, NMOS transistors, comparators, gate drivers, multiplexors, shorting control comparator) components would be necessary to implement a rectifier and shorting control using discrete components. The large supply current needed for the nS propagation delay comparators and the increased switching losses from trace parasitics would decrease the efficiency of the active rectifier.

An integrated circuit offers the prospect of integrating all four rectifier transistors, three comparators and any additional circuitry on a single chip. Application specific comparators can be built with low propagation delays and low supply currents optimised for the application. In addition, the parasitic capacitance and inductance between rectifier transistor gates and the control circuitry is minimised resulting in lower switching losses and switching delays. Designing an integrated circuit gives optimum performance and minimum size.

2.9. Summary

Chapter 2 introduced the theory of inductive power transfer and covered the important concepts of secondary resonance and single-turn equivalent values, a concept useful for comparing coil designs under constrained geometries. The advantages of parallel-tuned secondary pickups over series-tuned pickups were discussed for the expected load and
coupling conditions of a smart shunt. An analysis of the load power, winding losses and pickup efficiency was carried out for the parallel pickup configuration.

Following the pickup analysis, a range of rectifier topologies were outlined and the active diode synchronous rectifier (ADSR) was introduced. The ADSR operation was explained with extensive analysis of the load power, sources of loss and efficiency. Practical considerations for the ADSR were addressed. Methods for secondary based power flow control were covered with a detailed discussion of shorting control. The interaction between shorting control and the secondary pickup was shown to achieve larger efficiencies with larger open-circuit voltages and larger power transfer with lower open-circuit voltages. The chapter concluded with a discussion on the benefits of implementing the ADSR and power flow controller with an integrated circuit.

A summary of equations and conditions contributed from this thesis is given in Table 2.2

<table>
<thead>
<tr>
<th>Description</th>
<th>Equation</th>
<th>Condition/ Assumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Condition for approximating parallel resonance to $\omega = 1/\sqrt{L_2C_2}$</td>
<td>$1 \gg \frac{Q_2}{1 + Q_2^2}$</td>
<td>$R_L \gg \sqrt{L_2/C_2}$</td>
</tr>
<tr>
<td>Parallel-tuned secondary gain</td>
<td>$A' = \frac{R_L}{\sqrt{R_2^2 + (R_L/Q_2 + Q_2R_2)^2}}$</td>
<td>$R_L \gg \sqrt{L_2/C_2}$</td>
</tr>
<tr>
<td>Series-tuned secondary gain</td>
<td>$A' = \frac{R_L}{R_L + R_2}$</td>
<td></td>
</tr>
<tr>
<td>Condition for parallel tuning to provide greater power transfer than series tuning</td>
<td>$R_L &gt; \omega L_2$</td>
<td>$R_L \gg \sqrt{L_2/C_2}$</td>
</tr>
<tr>
<td>Maximum power turns ratio for series VS parallel-tuned coils</td>
<td>$\frac{N_{\text{2-series}}}{N_{\text{2-parallel}}} = \sqrt{1 + Q_2^2}$</td>
<td></td>
</tr>
<tr>
<td>Secondary efficiency</td>
<td>$\eta_2 = \frac{1}{1 + \frac{R_L}{R_L} \left( \frac{L_2/C_2 + (R_L + R_2 + R_L^2R_2C_2/L_2)^2}{R_2^2 + \left( \sqrt{L_2/C_2} + \sqrt{C_2/L_2} R_2 R_2 \right)^2} \right)}$</td>
<td>$R_L \gg \sqrt{L_2/C_2}$</td>
</tr>
<tr>
<td>ADSR efficiency including switching losses</td>
<td>See equation (2-53)</td>
<td>No comparator hysteresis</td>
</tr>
<tr>
<td>Equivalent load resistance with open-circuit voltage for shorting control</td>
<td>See equation (2-71)</td>
<td></td>
</tr>
</tbody>
</table>

Table 2.2: Summary of derived equations and conditions.
Chapter 3  Integrated Circuit Design

Integrated circuit (IC) technology allows components such as resistors, capacitors, MOSFETs and BJTs to be manufactured on a single silicon chip. Components, and the tracks between them, can be made extremely small resulting in complex circuits only millimetres in size. Furthermore, the complete flexibility in which components are used allows circuits to be customised and optimised for specific applications. This chapter presents the introduction to IC design and some common circuit structures. The requirements of an ADSR and shorting control method are established for an IC implementation. Subsequently, the sub-circuits required for an ADSR, shorting controller and the complete power IPT management circuit are developed.

3.1.  Notation Conventions for this Chapter

When referring to an amplifier or analogue circuit, it is helpful to separate large signal DC notation from small signal AC notation and combined signal notation. Herein the following conventions will be used for voltage and current notation:

- Upper case variables with upper case subscripts refer to a large signal or DC quantities, e.g. $V_{ID}$.
- Lower case variables with lower case subscripts refer to small signal quantities, e.g. $v_{id}$.
- Lower case variables with upper case subscripts refer to the combined DC and small signal quantities, e.g. $v_{id} = v_{id} + V_{ID}$.

For AC signals, voltages will be specified as root mean square values (RMS) unless specified as amplitude or peak values with a $p_k$ subscript such as, $V_{pk}$.

3.2.  Integrated Circuit Fabrication

Silicon (Si) is the base material for many semiconductor devices. Controlled amounts of impurities can be introduced to the silicon in a process called doping [96]. Doping alters the silicon’s properties such as resistivity, and can change the majority conduction carrier to holes or electrons [97], [98]. When the majority carrier is electrons, the silicon is referred to as n-type. P-type refers to the silicon where holes are the majority carrier. This allows the creation of pn junctions and hence devices such as metal oxide field effect transistors.
(MOSFETs), bipolar junction transistors (BJTs) and diodes. An integrated circuit (IC) has many such devices, micro-meters in size, created on a single die (a single piece of a diced silicon wafer).

Very-high-purity crystalline silicon is used as the substrate for an integrated circuit. An ingot of silicon 10-30cm in diameter and 1-2m long is sliced into 400-600µm thick wafers [96] and polished mechanically and chemically to a very fine finish. Oxidization forms a thin layer of silicon dioxide (SiO\textsubscript{2}) on the silicon surface which acts as a barrier to the diffusion of impurities [99]. Photolithography is used to define component structures or metal tracks. A photoresist is spun onto the oxide surface and exposed to light through a mask acting as a stencil. Chemicals are used to remove the photoresist where it has been exposed to light (for a positive photoresist) leaving the device geometry. Thus, the oxide can be selectively removed, and impurities can be added to dope the silicon using diffusion and ion implantation. This process may be repeated multiple times for different dopants and doping levels. Chemical vapour deposition is used to deposit polysilicon for resistors and transistor gates as well as SiO\textsubscript{2} between metal layers [97]. The silicon dioxide insulation layers also allow for the creation of capacitors.

In general, many integrated circuits are fabricated at once on the silicon wafer. Creation of the masks, processing of the wafer and slicing of the wafer into individual die is an expensive process. As such, ICs are expensive when fabricated in small numbers. However, a single silicon wafer may produce hundreds or thousands of ICs resulting in a low cost per die [97].

ICs are typically designed for a particular manufacturer or foundry. The foundry offers a range of technologies with varying features such as minimum transistor gate length, HV transistor options, bipolar junction devices, etc. The IC is designed in the chosen technology and sent to the foundry for fabrication.
3.3. The Integrated Circuit MOSFET and Common Circuit Structures

MOSFETs are the base component for any circuit designed in a complementary metal oxide semiconductor (CMOS) process. As such, the following section covers important concepts of MOSFETs and their design in CMOS. The transistors created in CMOS use polysilicon gates, not metal, and will be referred to as field effect transistors (FETs). An in depth analysis of FETs can be found in [96], [99] but is outside the scope of this thesis. Readers familiar with MOSFET theory, process variation and latchup may wish to skip to Section 3.4.

A FET is a three terminal device having a gate, drain and source. A voltage applied to the gate allows current to flow from the drain to the source. For the following explanation, a p-type silicon substrate is used. Looking at the n-channel (NMOS) transistor in Figure 3.1, two n$^+$ diffusions (heavily doped with majority carrier electrons) are separated by the p-type substrate. The pn-junction formed around each n$^+$ diffusion acts as a diode. Current can flow from the substrate to the diffusion but not vice versa. This state is called cutoff as no current flows when $v_{GS}$ is zero. The polysilicon gate separated from the substrate by an insulator acts like a capacitor. Applying a positive voltage to the gate draws electrons to the substrate surface and forms a “channel” though which current can flow. The gate-source voltage $v_{GS}$ must be larger than the threshold voltage $V_t$ for a channel to form and appreciable current to flow [96]. While $v_{DS}$ is below $v_{GS} - V_t$ the transistor is in the triode region. Once $v_{DS}$ becomes greater than $v_{GS} - V_t$, a phenomenon called pinch-off limits the current flow, and the device is referred to as being in the saturation or active region [99].

![Figure 3.1: NMOS and PMOS physical structure in a CMOS process.](image-url)
Table 3.1 summarises the equations describing the FET drain current in each region for NMOS and PMOS devices. $k' = \mu C_{ox}$ is the gain factor where $\mu$ is the average electron mobility $\mu_n$ for n-channel devices and the average hole mobility $\mu_p$ for p-channel devices. $C_{ox}$ is the gate oxide capacitance per unit area. $W$ and $L$ are transistor width and length respectively and $\lambda$ is a technology dependent parameter. Channel length modulation accounts for the small change in $i_D$ due to changes in $v_{DS}$ when the transistor is in saturation. Typically, $\lambda$ is small and is approximated to zero for DC analysis.

### Table 3.1: NMOS and PMOS drain current and regions of operation.

<table>
<thead>
<tr>
<th>Condition</th>
<th>NMOS &amp; PMOS</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cutoff</td>
<td>$i_D = 0$</td>
<td>$</td>
</tr>
<tr>
<td>Saturation (Active)</td>
<td>$i_D = \frac{k'W}{2L}(</td>
<td>v_{GS}</td>
</tr>
<tr>
<td>Triode</td>
<td>$i_D = \frac{k'W}{2L}(2(</td>
<td>v_{GS}</td>
</tr>
</tbody>
</table>

For FETs acting as switches it is useful to approximate their effective resistance when $v_{DS}$ is small. The resistance can be approximated from the equation for drain current through a MOSFET in triode region which can be rearranged to give,

$$\frac{v_{DS}}{i_D} - \frac{v_{DS}^2}{2(V_{gs} - V_t)i_D} = \frac{L}{k'W(v_{gs} - V_t)}$$

(3-3)

Providing $v_{DS}$ is small (3-3) can be approximated to,

$$R_{ds} = \frac{v_{DS}}{i_D} = \frac{L}{k'W(v_{gs} - V_t)}.$$  

(3-4)

If large gate widths are required, device fingering is commonly used. This is a design method where multiple transistors are connected in parallel sharing a drain and source with neighbouring devices as shown in Figure 3.2. The device area is reduced compared to parallel devices each having their own source and drain.
3.3.1. Small Signal Model for the MOSFET

For signals with small amplitudes, the FET acts as a voltage controlled current source when in saturation. A signal $v_{gs}$ applied between the gate and drain creates a small signal drain current $i_d$. When the FET is in saturation, the transconductance can be approximated to [99],

$$g_m = \frac{\partial i_d}{\partial v_{gs}} = \sqrt{\frac{2k'}{W}l_D}.$$ (3-5)

This approximation is accurate providing the small signal input voltage to the transistor gate is less than twice the overdrive voltage [99] defined as,

$$v_{ov} = v_{gs} - V_t = \sqrt{\frac{2l_D}{k'(W/L)}}.$$ (3-6)

The hybrid-π model shown in Figure 3.3 is used for analysing small signal behaviour. A voltage dependent current source models the drain current as a function of transconductance and gate source voltage. To model the effect of channel length modulation, an output resistance $r_o = 1/\lambda l_D$ is placed in parallel with the current source [99]. Longer channel lengths lead to larger output resistances.

Another non-ideal characteristic of the transistor, body effect, can be included in the hybrid-π model. An additional voltage controlled current source $g_{mb}v_{bs}$ in parallel with $g_mv_{gs}$ accounts for this effect [99]. In this work, body effect will be ignored for simplicity and corrected for in simulation. Some important results from this model are analysed below.
If only a DC voltage is applied to the FET gate, the gate will be grounded for AC signals. The small signal output resistance of the FET drain with a source load resistance $R_L$ can be found from Figure 3.4 by noting,

$$r_{out} = \frac{v_{in}}{i_{in}} = \frac{v_{in}}{g_m v_{gs} + (v_{in} - v_S)/r_o} = \frac{v_{in}}{g_m i_{in} R_L + (v_{in} - i_{in} R_L)/r_o}$$

which can be rearranged to give,

$$r_{outD} = r_o + R_L + g_m r_o R_L.$$  \hfill (3-7)

The small signal output resistance can be significantly larger than the load resistance.
The input resistance looking into the source can be found from Figure 3.5

\[ r_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{in}}{(v_{in} - v_d)/r_o + g_m v_{gs}} = \frac{v_{in}}{(v_{in} - i_{in} R_L)/r_o + g_m v_{in}} \]

which can be re-arranged to give,

\[ r_{inS} = \frac{r_o + R_L}{1 + g_m r_o} \quad (3-8) \]

If \( R_L \) is smaller than \( r_o \) and \( g_m r_o \gg 1 \) then (3-8) can be approximated to,

\[ r_{inS} = \frac{1}{g_m} \quad (3-9) \]

Providing \( g_m \) is large, the small signal source input resistance is small. The source of a FET isolates circuitry from the load at the FET drain.

These results will be useful in analysing the small signal behaviour of circuits later in the chapter.

3.3.2. The MOSFET Current Mirror

Current mirrors are used extensively in IC design justifying their brief introduction. A current source running through a FET with its gate attached to its drain as in Figure 3.6 creates a voltage \( V_{ov} = V_{GS} = \sqrt{2I_{IN}/(k' W/L)} \) [99]. The gate source voltage of \( N_2 \) is identical to that of \( N_1 \) and consequently,

\[ I_{DN2} = \frac{(W/L)_{N2}}{(W/L)_{N1}} I_{IN} = M I_{IN}. \quad (3-10) \]
Due to channel length modulation, a different $V_{DS}$ across $N_2$ and $N_1$ will result in an error between the current mirrors [99]. This is also apparent in the small signal output resistance looking into the drain of $N_2$. Using equation (3-7), $r_{out}$ is found to be $r_o$. The minimum load voltage across $N_2$ for this current mirror is [99],

$$V_{OUT(min)} = V_{ov}$$  \hspace{1cm} (3-11)

while the minimum input voltage across $N_1$ is [99],

$$V_{IN(min)} = V_t + V_{ov}.$$  \hspace{1cm} (3-12)

Techniques such as using a cascode current mirror or Sooch current mirror [99] to decrease the effect of channel length modulation and increase the small signal output resistance are well documented but outside the scope of this thesis.

![Figure 3.6: Simple current mirror. The drain current in $N_2$ mirrors the drain current though $N_1$.](image)

### 3.3.3. Differential Pair

The differential pair is a central circuit structure to IC design with a vast number of applications. The MOSFET source coupled pair will be introduced in this section. For an in-depth understanding [1] and [99] provide extensive analysis of the differential pair.

The source coupled pair shown in Figure 3.7 has two identical transistors $N_1$ and $N_2$ with source terminals shorted. The current source $I_{TAIL}$ is split equally between $N_1$ and $N_2$ when $V_{IN+} = V_{IN-}$. A positive differential voltage $v_{id} = V_{IN+} - V_{IN-}$ will cause an increase in the drain current of $N_1$ and a decrease in the drain current of $N_2$. In turn, this decreases $v_{od} = V_{OUT+} - V_{OUT-}$ due to the change in voltage drop across resistors $R_D$. The small signal differential voltage gain is [99].
\[ A_{dm} = \frac{v_{od}}{v_{id}} = -g_m R_D \]

where \( g_m \) is the transconductance of \( N_1 \) and \( N_2 \). The differential current gain is,

\[ A_{id} = \frac{i_{dN1} - i_{dN2}}{v_{id}} = -g_m. \quad (3-13) \]

![Figure 3.7: Source coupled pair.](image)

### 3.3.4. Process variation and Pelgrom Coefficients

During fabrication, small variations in processing lead to parameter variations across different wafers and within wafers. The effects can be broken down into process variation and device mismatch.

Process variation accounts for variations from wafer-to-wafer. These variations change parameters across the whole integrated circuit. For example, the transistor threshold voltage for all devices on a die will vary about the mean by the same amount. Consequently, circuits cannot be designed assuming parameters will always be identical. Consider the left most amplifier in Figure 3.8 which has a gain of \( v_{out}/v_{id} = -g_m R_L \). Transconductance varies from die to die resulting in different amplifier gains. Thus, the circuit must be designed to account for this. Parameter variation between devices on the same die is much smaller. Thus, an amplifier could be designed to have an accurate gain by using the ratio of resistance between two feedback resistors. The right hand amplifier in Figure 3.8 has feedback resistors
$R_{F2}$ and $R_{F1}$. If the feedback resistors are much larger than $R_L$, and $R_L g_m$ is much greater than one, $V_{out} \approx 1 + R_{F2}/R_{F1}$. Because $\alpha = R_{F2}/R_{F1}$ is a ratio, a resistance increase of all devices across the die has no effect on $\alpha$.

Device mismatch refers to the small, unavoidable differences between identical devices on the same die. For example, the feedback resistors in Figure 3.8 may have a mismatch resulting in a variation of $\alpha$. Layout methods used to reduce the magnitude of mismatch are presented in the next chapter.

Assuming optimised device layout, device mismatch is dependent on device area. Two physically large resistors will have a smaller mismatch than two smaller resistors. This phenomenon is modelled using Pelgrom coefficients. Pelgrom, Duinmaijer and Welbers showed that device mismatch is approximately proportional to the square root of the device area [100]. For a matching parameter such as FET threshold voltage, the standard deviation of the mismatch can be calculated as,

$$\sigma(V_t) = \frac{A_x V_t}{\sqrt{WL}}$$  \hspace{1cm} (3-14)

where $A_x$ is the Pelgrom coefficient and is provided by the foundry. Pelgrom coefficients can be used to define a minimum transistor area or resistor area, etc. for a given allowable standard deviation in matching between two components.
3.3.5. Latchup and Guard Rings

When an NMOS and a PMOS transistor are placed close together two inherent parasitic BJTs are formed. These BJTs form a positive feedback loop such that, if activated and the gain is greater than unity, they continue to sink a large and potentially destructive current. Latchup and techniques to prevent it are well documented [85], [96], [99]. Among other factors, the parasitic BJTs can be activated by application of voltages larger or smaller than the power supply rails, large displacement current in the substrate and sudden node voltage changes. Three methods of reducing the gain of the BJT feedback loop include increasing the separation between NMOS and PMOS devices, using suitably designed substrate and well ties and incorporating guard rings [99]. Substrate and well ties ensure the area surrounding a FET is correctly biased. The p-type substrate is connected to ground and n-wells are connected to VDD. Ties collect any stray currents that would de-bias the substrate or wells and decrease the potential for the BJTs to activate. However, ties only collect majority carriers, holes in the p-type substrate material and electrons in n-type wells. Guard rings are used to collect minority carriers. An n⁺ diffusion in the p-substrate attached to $V_{DD}$ collects stray electrons, and a p⁺ diffusion in an n-well attached to ground collects holes [85]. Together, ties and guard rings significantly reduce the likelihood of latchup.

3.4. Integrated Circuit Design Process

Computer aided design (CAD) is used extensively in the design of integrated circuits. The foundry provides process specifications defining key parameters such as MOSFET gain factor, threshold voltage and gate capacitance per unit area for specific device geometries. A design is completed using the devices defined by the foundry. Parameters such as FET gate length and width can be changed. The geometry of the device however must stay within the design rule specifications, a set of constraints defined by the foundry, for the fabricated parameters to match those defined in the process specifications. In addition to the process specifications, spice models are provided allowing accurate simulation of the circuit.

Specialised CAD software allows creation of the circuit schematic, simulation, physical layout, layout vs schematic checking, design rule checking and parasitic extraction. An overview of the design process is shown in Figure 3.9 and will be explored step by step below.
3.4.1. Concept and Technology

Once the circuit specifications are defined, a concept or system design can be developed. Based on the system design a suitable technology that provides the necessary devices and voltage ranges is selected.

CMOS is the most common technology for integrated circuits allowing design of both analogue and digital circuits. Compared to CMOS processes the bipolar-junction-transistors available in BiCMOS processes provide the best high frequency, high gain circuitry. However, these characteristics are not necessary for this application, and CMOS is typically cheaper. Silicon-on-insulator (SOI) processes have multiple advantages over CMOS including lower parasitic capacitance, device isolation and reduced temperature dependence. Again this comes at higher price than CMOS. For an ADSR, HV CMOS technology can be used to create the comparators, voltage biases, control circuitry and high voltage components.

High voltage (HV) transistors\(^5\) with above 4V operating range are necessary to withstand the pickup input voltage. A thick metal layer is required to minimise resistance and to carry large currents without the occurrence of electromigration, a process by which metal traces degrade due to high current densities [85]. Additionally, a process with low voltage transistors was desired for future development of low power circuitry integrated alongside the power management circuitry. The XH018 HV CMOS process available through X-FAB was selected as an appropriate technology. The minimum feature size is 0.18µm for 1.8V devices but larger for higher voltage devices. Some of the key technology specifications are presented in Table 3.2. Furthermore, X-FAB’s quality management system covers all the requirements of the ISO-13485 standard for medical device design and manufacturing except the product and application assurance activates and requirements. This means the processing and manufacturing of the IC meets the ISO-13485 standard, but the final product design must also be shown to meet the standards.

\(^5\) For CMOS, HV transistors are transistors with operating voltages above the standard CMOS transistor operating voltage. Transistors with operating voltages above 5V will be referred to as HV transistors.
The thick metal layer has a maximum current density of $6\text{mA/\mu m}$. Below $85^\circ\text{C}$ the metal track can carry a DC current with this current density for $10^5$ hours (approximately 11 years) before a 20% shift in resistance occurs. The lifetime is much longer for an AC current that is not operating 24 hours each day. As a conservative estimate, the AC current may approach the maximum current density for a fifth of each rectification cycle. Thus, if operating 24 hours each day, it would last approximately 55 years, five times the DC life at maximum current density.
Table 3.2: Key devices and options available in XH018 CMOS process

<table>
<thead>
<tr>
<th>Process Option</th>
<th>Characteristic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thick Metal</td>
<td>3µm thickness</td>
</tr>
<tr>
<td>1.8V CMOS</td>
<td>1.8V VDS</td>
</tr>
<tr>
<td>3.3V CMOS</td>
<td>3.3V VDS</td>
</tr>
<tr>
<td>HV PMOS</td>
<td>6V VDS</td>
</tr>
<tr>
<td>HV NMOS</td>
<td>6V VDS</td>
</tr>
<tr>
<td>P-Type BJT</td>
<td>-3.6V VCE</td>
</tr>
<tr>
<td>High Resistance Poly</td>
<td>45V terminal to bulk</td>
</tr>
</tbody>
</table>

The 3.3V CMOS module allows creation of analogue and digital circuitry for control of the rectifier. The maximum voltage for reliable operating is 3.6V for $V_{DS}$ and $V_{GS}$ with an absolute maximum (abs max) of 4V before catastrophic failure. The minimum gate length for the 3.3V CMOS transistors is 0.35µm. HV CMOS and HV PMOS modules provide FETS with 6V maximum (8V abs max) $V_{DS}$ and 18V (20V abs max) $V_{GS}$. These FETS have a minimum gate length of 1µm. P-type BJTs, an important building block in bandgap voltage references, are available as part of the standard process. Lastly, high resistance polysilicon resistors are also available as part of the standard process and allow for creation of compact resistors.

### 3.4.2. Electrical Design

Some technologies have circuit blocks, such as comparators and voltage biases, which can be purchased. These are often not specialised enough for the design and hence all sub-circuits must designed at the transistor level. A set of specifications is developed from the system design for each component sub-circuit and is designed using the available transistors, resistors, capacitors and diodes. FETs are the smallest and most versatile device in CMOS. Often a component such as a comparator will be designed exclusively with FETs. Using the available process device specifications (PDS), the circuit can be implemented based on standard device equations and approximations.

Electrical verification involves simulating the design using the simulation models for the technology. The simulation models include technology specific parameters as well as non-linear effects, gate-capacitance, body effect and other parameters that are ignored or
linearised to simplify hand analysis. The cost of fabrication makes re-design prohibitive. Thus, simulations must be accurate enough that the results match the fabricated device. Parasitic resistance and capacitance (parasitics) can be extracted from the physical device layout (as explained in the following section) for the tracks and between devices to increase the simulation accuracy. As an example, two parallel tracks less than $1\mu m$ apart may have a large enough coupling capacitance that it affects the circuit operation. Including parasitics in the simulation reduces the chance of design failure.

Simulating the effect of process variation is a critical step in IC design. To aid in this, the foundry may provide statistical information on the parameter variation and device mismatch. There are two dominant methods used for assessing parameter variation:

1. Corner Simulation
2. Monte Carlo Simulation

Corners typically refer to the worst case fast/slow limits of the NMOS and PMOS devices in a CMOS process. ‘Fast’ and ‘slow’ refer to the switching performance for digital devices. Classically, a specially made slow/fast corner lot is fabricated by the foundry and characterised to define the worst possible fast and slow performance of the NMOS and PMOS devices [101]. The fast NMOS and fast PMOS form one corner of a box, fast NMOS and slow PMOS another corner, etc. The box should contain all of the possible parametric variation, and simulating over the worst case corners allows a design to be verified over the range of possible parameter variation [101]. The corners do not give an indication as to how likely the corner is to occur. A circuit might have to be majorly overdesigned to meet the corner cases that are very rare in practice and will only cause a small number of chips to fail. In addition, for analogue design, the corner cases are not necessarily the worst case process parameters for a design. This has led to Monte Carlo simulation becoming an important simulation method for verifying analogue designs.

Monte Carlo simulation is used to run multiple simulations where the parameter variation and device mismatch are applied to the models. A statistical distribution of the process parameters is provided by the foundry. The simulator randomly samples this distribution and applies the parameters to the simulation models. Simulations are repeated multiple times resulting in a distribution of possible outputs from the circuit. An output distribution from the simulation results is used to calculate the yield of successful chips or verify the design is robust enough to function as expected over the range of variation possible.
3.4.3. Physical Design

Physical design for analogue integrated circuits is normally completed by hand. Each process step of the IC is mapped to a layer such as metal1 layer, p⁺ layer and polysilicon layer. Design rules specified by the foundry provide constraints for the proximity, overlap, crossing, etc. of different layers. In addition, devices such as MOSFETS have specific design rules that must be met for them to operate as specified. Generally, physical models are provided for each device available through the foundry. Schematic driven layout (SDL) maps the schematic to physical devices and highlights connectivity between devices.

One of the key challenges in physical layout is minimising device mismatch though optimum layout. The different methods of reducing device mismatch are presented in Figure 3.10 for a resistive divider which should have low mismatch [85].

1) Increasing device area reduces random variation and increases device matching. Alternately, using multiple devices in parallel or series also increases matching.
2) Keeping devices close together reduces mismatch that may be an effect of a gradient variation across the die.
3) Keeping devices the same size (called a unit cell) reduces mismatch from edge effects and size dependent variation.
4) Common centroid layout reduces mismatch form linear gradient differences across the wafer. Two devices that should match closely can be arranged symmetrically around a common centre.
5) Identical orientation is important to reduce mismatch from directional effects. In addition, current flow though matched devices should be in the same direction.
6) Use of dummy devices reduces mismatch by keeping all devices under the same conditions. Without dummies, the outer devices may have additional etching on the outside edges.

The vast number of devices and connections in a single IC are too complex to accurately verify manually. Physical verification involves running an automated design rule check (DRC) and layout versus schematic (LVS) check. DRC checks that all physical devices and layers meet the technology design rules. LVS is used to check all physical devices are connected as in the schematic circuit design. Incorrect connections, open circuits, short circuits and number of devices are all verified.
Parasitic extraction is the final step in verifying the design. Extraction software is used to estimate the parasitic resistance, capacitance and sometimes inductance on specified nodes. The parasitics can be large enough to significantly degrade circuit performance. In addition, the close proximity of metal tracks increases the chances of capacitive signal coupling. Extracted parasitics are back annotated to the schematic and re-simulated to verify the circuit performance will not significantly degrade as it is physically laid out.

3.4.4. Fabrication and Testing

Once the circuit has been designed, laid out and verified, it is sent to the foundry to be fabricated. It may take multiple months to manufacture the circuit. Wires are attached to bond pads (metal pads large enough to attach a wire situated around the periphery of the IC) allowing electrical connection with the IC. Testing can only be carried out on circuit nodes with bond pads. As bond pads require a large area, only the circuit nodes requiring inputs and outputs to external circuitry are bonded-out. The circuit function must be verified from the available nodes.

3.4.5. IC Design Software

The custom IC design suite from Mentor Graphics⁶ was used to design the IC. Schematic capture was carried out in Pyxis Schematic. Simulation was run in the Eldo Classic simulation environment. Pyxis Layout was used to complete the physical layout. Calibre DRC, LVS and xRC were used for design rule checking, layout VS schematic checking and parasitic extraction respectively.

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⁶ https://www.mentor.com
3.5. ADSR Design for Integrated Circuit Technology

In the following section, the concept for a CMOS implementation of the active diode synchronous rectifier (ADSR) from Chapter 2 is developed. The requirements for the integrated circuit can be split into:

- **ADSR requirements:**
  - When active, the ADSR should be capable of supplying 0-500mW of load power between 3.3V and 3.6V.
  - The efficiency should ideally be high over the entire 0-500mW range but especially at the upper range where a lower efficiency results in greater heating.
  - As the input voltage must increase above the load voltage, all transistors and devices attached to the pickup should be able to withstand greater than 3.6V.
  - Current spikes though the ADSR should be low enough to avoid electromigration.

- **ADSR start-up requirements:**
  - On start-up, the load voltage is 0V, and the ADSR is off. The ADSR needs to work as a passive rectifier until $V_{RL}$ is large enough to power the control circuitry.
  - Once $V_{RL}$ can supply the control circuitry, it can be enabled by a start-up circuit.

- **Shorting control requirements:**
  - Shorting control must accurately monitor $V_{RL}$ such that it never goes above 3.6V. As no external components will be used to generate a reference voltage, an on chip voltage bias that is precise across fabrication runs must be designed.
  - Large pickup currents generated by strong magnetic fields should cause minimal heating.

Figure 3.11 presents an ADSR structure compatible with the above requirements. The transistors $M_{P1}$, $M_{P2}$, $M_{N1}$ and $M_{N2}$ are switched on and off at the correct instances to achieve synchronous rectification of the AC input voltage. While operating as a synchronous rectifier $V_{SC} = 0$, and the top inputs to the multiplexors are connected to the gates. The case
when the input to the rectifier is a sinusoidal voltage across the pickup such that \( V_{IN+} - V_{IN-} = V_I \sin(\omega t) \) is used to explain the ADSR operation. When \( V_{IN-} \) is less than \( V_{out} \) by the PMOS threshold voltage \([V_{th}]\), the cross-coupled PMOS transistor \( M_{P1} \) moves first into the active region and then the triode region. As \( M_{P1} \) is on, the load voltage \( V_{RL} \) is connected to \( V_{IN+} \). However, no current flows because \( M_{N1} \) and \( M_{N2} \) are in cutoff. When \( V_{IN-} \) is less than the negative threshold of the comparator \( V_{th-} \), \( A2 \) will go high putting transistors \( M_{N2} \) into the triode region. Current flows from the pickup into the output capacitor \( C_f \) through \( M_{N2} \) and \( M_{P1} \). When \( V_{IN-} = 0 \), the comparator puts \( M_{N1} \) into cutoff. Thus, the MOSFETS are used as active diodes with zero forward voltage and a low series resistance. Having the PMOS transistors driven by the pickup voltage reduces the circuit switching losses as only two gates are being actively driven from the load voltage.

During start-up, before the load voltage has become large enough to power the active circuitry, the internal diodes of \( M_{N1} \), \( M_{N2} \), \( M_{P1} \) and \( M_{P2} \) work as a standard diode full wave rectifier. The start-up circuit block enables the active circuitry once \( V_{RL} \) is large enough to power it.

The design uses a combination of 6V and 3.6V transistors. If 3.6V transistors were used as pass transistors, \( V_{RL} \) could never reach 3.6V because the input voltage must go higher than this for current to flow. Using 6V transistors at the pickup allows 2.4V overhead for protection from voltage spikes and changes in coupling. The high on-resistance of the HV

![Figure 3.11: Schematic of synchronous rectifier. Circled components are not included in the integrated circuit.](Image)
transistors means they have to be relatively large. The PMOS multiplexors and all of the 
FETs shown in Figure 3.11 use 6V transistors. The other circuitry, including comparators, 
use 3.6V transistors.

Voltage dividers are used to bring the input signals into the comparators’ operating range. To 
prevent over-voltage of the comparator inputs, $M_{N3}$ and $M_{N4}$ are biased with $V_{RL}$ such that 
they are put into cutoff when $V_{IN+}$ or $V_{IN-}$ approach $V_{RL}$. The shorting control block 
compares the load voltage with a reference voltage and maintains $V_{RL}$ below 3.6V, so the 
comparator inputs cannot be subject to overvoltage.

A reference circuit provides a voltage and temperature independent voltage reference for the 
shorting control circuit. It also provides a current reference to bias the comparators.

### 3.6. Power Switches and Start-up Diodes

The minimum size of the transistors $M_{N1}$ and $M_{N2}$ is limited by the power dissipation during 
shorting control. It was established in Chapter 2 that the power dissipated in the load of a 
parallel-tuned secondary is,

$$ P_L = \frac{V_{OC}^2}{R_L^2} + \left( \frac{R_L}{\sqrt{L_2/C_2} + \sqrt{C_2/L_2 R_L R_2}} \right)^2. $$

When shorting control is active the load is the combined NMOS pass transistor resistance. 
The appropriate shorting-resistance $R_S$ can be determined from the maximum allowable 
power dissipation during shorting $P_{L(\text{max})}$ and the maximum possible open-circuit voltage 
$V_{OC(\text{max})}$,

$$ R_S = \frac{L_2}{C_2} \left( \frac{2P_{L(\text{max})}R_2 - V_{OC(\text{max})}^2}{2P_{L(\text{max})}R_2^2} \right) \left( \sqrt{\frac{L_2}{C_2} \left( \frac{2P_{L(\text{max})}R_2 - V_{OC(\text{max})}^2}{2P_{L(\text{max})}R_2^2} \right)} - \frac{L_2}{C_2} \left( 1 + \frac{L_2}{C_2 R_2^2} \right) \right)^2 $$

The FDA standard ISO 14708-1:2000 E states that the surface of an implanted device should 
not rise more than 2°C above body temperature (37°C) [102]. It is difficult to estimate the 
heating of a device from its power dissipation without the final geometry and properties of 
the implanted medium. S. Kim examined the thermal heating of an electrode array 7.88mm
by 7.56mm with a 10 by 10 array of 1.8mm long by 80µm wide silicon spikes. When implanted in the brain the heating was found to be 0.051°C/mW when not covered by the skull and 0.029°C/mW when covered [103]. This indicates that approximately 68mW can be dissipated in the implant before the surface temperature rises by 2°C. The pressure monitor would be larger than the implant from [103]. Therefore, if less than approximately 70mW can be dissipated we would not expect the hydrocephalus monitor to cause heating concerns.

It is possible for an arbitrarily large $V_{OC}$ to be generated by the primary. To constrain the size of the shorting transistors, the following assumptions about the magnitude of $V_{OC}$ are made.

1. The largest magnetic field created by the primary will be that needed to power the monitor at its maximum power output.
2. The primary will require maximum coupling when supplying the secondary’s maximum load, hence the coupling cannot increase.
3. The shorting-resistance will be designed for a field strength twice what is expected as a safety factor.
4. No alternate source will generate a stronger magnetic field at the IPT resonant frequency than the primary.

Hence the worst case power dissipation for shorting control occurs when the field strength is set for supplying 500mW, but the load is infinite (no power draw). The open-circuit voltage needed to power a load can be found by rearranging (2-35) in terms of $V_{OC}$ to give,

$$V_{OC} = \sqrt{\frac{P_L}{R_L}} \left( R_S^2 + \left( \sqrt{L_2/C_2} + \sqrt{C_2/L_2} R_S^2 \right)^2 \right).$$  \hfill (3-17)

At the maximum expected output power of 500mW and load voltage of 3.3V, the load will be approximately 22Ω. For the test case coil matched to 100Ω with $L_2 = 1.873\mu H$ and $C_2 = 35.89nF$, $V_{OC}$ must be 1.868$V_{pk}$ to supply 500mW. A safety factor of two gives an open-circuit voltage of 3.736$V_{pk}$. Figure 3.12 shows the power dissipation in the shorting transistors as $V_{OC}$ and $R_S$ increase. The minimum shorting-resistance to drop the power dissipation to 70mW is 530mΩ from (3-16). The winding losses should also be considered for the case where the coil is included within the implant package. In this situation, the package would be larger, and more power could be dissipated with the same heating.

Figure 3.13 shows that shorting-resistance makes little difference to the coil losses over the range from 0.1Ω-1Ω. The coil loss is approximately 67mW with an open-circuit voltage of
3.736\(V_{pk}\). A 530m\(\Omega\) shorting-resistance would give a combined power loss of 137mW. Losses in the shorting-resistance would need to be less than 3mW to bring the combined power loss below 70mW. The shorting-resistance required to achieve this would require an excessive transistor area on the IC.

Figure 3.12: Power dissipated in shorting transistors with increasing resistance and open-circuit voltage.

Figure 3.13: Power dissipated in secondary coil with increasing shorting-resistance and open-circuit voltage. Shorting-resistance has little effect on losses in this range. An open-circuit voltage of 3.736\(V_{pk}\) results in 66.93mW of power dissipation in the coil winding resistance.
Using a 200mΩ shorting-resistance would result in 26.5mW of power dissipation in the shorting resistor, a combined power dissipation of 94mW with the winding losses. As heat dissipation is approximately proportional to surface area [104] the coil could be mounted within an implant package with approximately 130% more surface area than the implant from [103] without causing excessive heating during shorting control. Because there are two NMOS pass transistors in series, each transistor would need to have a resistance of 100mΩ.

The above estimates are approximations and depend heavily on the device geometry, materials, and implantation site. However, they provide constraints to the design for the necessary shorting control resistance.

The transistor size necessary to achieve 100mΩ can be found from simulating the 6V NMOS (referred to as NMA) transistor resistance with an expected 3.3V gate voltage over a range of input currents. For the maximum open-circuit voltage of 3.736\(V_{pk}\) the peak current through the shorting transistors would be 515\(mA_{pk}\) (\(I = \sqrt{P/R}\)).

The on-resistance for an NMA device when \(|V_{GS}| = 3.3V\) was found through simulation to be approximately 10 \(K\Omega/\mu m\). Therefore, the NMA transistors’ widths should be \(W = R_W/R_S\) where \(R_W\) is the resistance per micro meter of width for the NMA transistor and \(R_S\) is the shorting-resistance. For an NMA resistance of 100mΩ a transistor width of 100\(mm\) is required. This gate length is implemented practically as many parallel devices.

The gate capacitance of the PMOS transistor does not affect the rectifier efficiency as it is not being charged from the load voltage. Therefore, it should be sized as large as possible to allow for minimum resistance. The layout area for the 6V PMA transistors is larger than for the NMA transistors due to design rule requirements. An optimisation for the relative sizes of the PMA and NMA devises based on die area and \(R_S\) is possible as formulated in [69]. However, for practicality of layout, the PMA device has been sized with a width of 80\(mm\) to use the same die area as the NMA device. This gives an on-resistance of approximately 400mΩ for the PMOS bridge transistors.

The efficiency of the rectifier can be estimated with equation (2-53) from Chapter 2 repeated here for convenience,
\[ PCE = \frac{2V_iV_{DD}\sqrt{1 - (V_{DD}/V_i)^2} - V_{DD}^2 \left( \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) \right)}{\frac{V_i^2}{2} \left( \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) \right)} - V_iV_{DD}\sqrt{1 - (V_{DD}/V_i)^2} + \pi R_S \frac{1}{2} V_{DD}^2 f C_g. \]

The total switch resistance \( R_S = 500m\Omega \) for the NMA and PMA FETs. The gate capacitance \( C_g \) for the NMOS device is calculated from the process specifications to be \( 85pF \). For the PMOS devise, the gate capacitance is taken as zero because the PMOS gates are controlled passively from the pickup voltage and are not switched with the control circuitry. With \( V_{DD} = 3.3V \) the figure of merit of the combined PMA and NMA is \( 140p\Omega \). The analytical ADSR efficiency considering only rectifier MOSFET losses is plotted in Figure 3.14 over a range of \( 5mW \) to \( 1W \). Greater than 90% efficiency is achieved over the \( 50mW \) - \( 500mW \) output power range required for the ICP monitor. The control current will decrease the efficiency at low powers but will not affect the efficiency at high powers. For example, a \( 5mW \) power draw in the control circuitry would decrease the efficiency at an output power of \( 10mW \) to below 50%. The efficiency is also expected to be somewhat lower over the entire range in a practical implementation due to comparator delays and hysteresis.

![Figure 3.14: ADSR efficiency with 100mΩ NMA and 400mΩ PMA.](image-url)
3.6.1. Diode Resistance

During start-up the body diodes of the bridge transistors work as a full wave diode bridge rectifier. Their forward voltage drops and series resistances affect how efficient the rectifier is during start-up. The body diode for the PMA and NMA devices is not commonly used or described in the process device specifications or model parameters. The parameters have been estimated through simulation. The simulated NMA and PMA devices had the same parameters: $W = 20\mu m$, $L = 1\mu m$ and $NF = 28$.

For the PMA transistor, the gate, source and body were connected together such that the gate source voltage was always zero. The drain was grounded, and the source voltage decreased from $0V$ to $-1.5V$. As can be seen in Figure 3.15, the body diode forward voltage is between $-1.1V$ and $-1.2V$. Past $-1.2V$, the body diode current becomes excessively high. In practice, the thermal dissipation within the diode would likely damage it before it could rise to one amp. The gradient of the curve from $-1.4V$ to $-1.5V$ can be used to find the internal resistance of the simulation model to be $9.53\Omega \mu m$. This is suspiciously low. The NMA body, source and gate were grounded, and the drain voltage was decreased from $0V$ to $-1.5V$ as in Figure 3.15. Again, the forward voltage is between $-1.1V$ and $-1.2V$, and the internal resistance is found to be extremely low at $7.84\Omega \mu m$. The manufacturer provides no data on the expected characteristics of the body diode with which to compare the simulation results.

If the simulations are accurate, the diode resistance can be ignored as the total resistance of the NMA and PMA devices would be less than $200\mu \Omega$. With forward voltage drops of $1.2V$, the rectifier would be highly inefficient during start up. Fortunately, with an external voltage regulator or resistive load, the current draw from the load will be low until the load voltage increases at which point the rectifier efficiency will improve. In addition, the PMA gates are not attached to their sources but are cross coupled with the pickup. As such, the PMA transistors will start operating once the pickup voltage amplitude rises above the PMA threshold voltage. The measured results from fabricated dice will need to be compared to the simulated results to guarantee the NMA and PMA body diodes are suitable for rectification during start-up.
With an RC load and ignoring diode resistance, the input power required to reach a load voltage can be found from,

\[
\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{V_{RL}}{V_{RL} + V_{FW}} \tag{3-18}
\]

where \( V_{FW} \) is the total forward voltage drop of the bridge. Substituting the output power \( P_{\text{out}} = V_{RL}^2/R_L \) into (3-23) and re-arranging gives,

\[
P_{\text{in}} = \frac{V_{RL}^2 + V_{FW}V_{RL}}{R_L} = P_{RL} + I_LV_{FW}. \tag{3-19}
\]

This states that the input power is the load power and average load current multiplied with the forward voltage drop of the rectifier bridge. The input power required to reach start-up is,

\[
P_{\text{in}} = \frac{V_{START}^2 + V_{FW}V_{START}}{R_L} = \frac{1}{\eta_{V_{START}}} \frac{V_{START}^2}{R_L}. \tag{3-20}
\]

Therefore, the start-up rectifier efficiency determines the necessary input power to activate the ADSR. If the start-up efficiency is low, the input power for start-up may be larger than under normal operation. With the combined 2.4V diode forward voltage, the necessary input power to reach a start-up voltage of 2.5V with a 100Ω load is approximately 120mW. The start-up power relative to the active power is,

\[
\frac{P_{\text{in(START)}}}{P_{\text{in(ACTIVE)}}} = \frac{V_{START}^2 + V_{FW}V_{START}}{(1/\eta_{ACTIVE})V_{ACTIVE}^2}. \tag{3-21}
\]

For the ADSR to start-up the following condition must be met,

\[
V_{FW} \geq \frac{V_{ACTIVE}^2}{\eta_{ACTIVE}V_{START}} - V_{START}. \tag{3-22}
\]
3.7. Comparator and Bias Circuit

The comparators act as the control circuitry for the ADSR. The load voltage is compared with the pickup voltage, and the comparators switch state when the rectifier bridge NMA transistors should be turned on. The comparators must have low propagation delays and have small power consumptions. In addition, changes in the threshold voltages and delays from process variation must be small.

3.7.1. Bias Circuit Operation and Design

The bias circuit in Figure 3.16 sets the required bias voltages for the comparator in Figure 3.17 using two Sooch current mirrors. Compared with the current mirror of Section 3.3.2, the Sooch current mirror uses four transistors, \( B_{P1} \) though \( B_{P4} \), on the input side and two on the output side, \( B_{P5} \) and \( B_{P6} \). This gives the advantage of a greatly increased small signal output resistance \( r_{OBP6}(1 + G_{mBP6}r_{OBP5}) + r_{OBP5} \). Additionally, channel length modulation is significantly reduced as the Sooch current mirror structure maintains \( V_{DSBP1} = V_{BPSS} \). However, the minimum input voltage and load voltages are larger at \( 2V_t + 3V_{ov} \) and \( 2V_{ov} \) respectively.

![Bias Circuit Diagram](image.png)

Figure 3.16: The bias circuit sets up the bias voltages for the comparator.
$V_{BP1}$ from the first Sooch current mirror is attached to two FETs in the comparator making them mirror the bias current and act like current sources. The bias voltages $V_{BN1}$ and $V_{BN2}$ are also set using a Sooch current mirror consisting of $B_{N1}$ though $B_{N4}$. These voltages allow an additional two transistors in the comparator to act together as a current source. The actual value of the bias voltages $V_{BP1}$, $V_{BN1}$ and $V_{BN2}$ are not important. They are only used to form current mirrors where the current in the comparator FETs will be a ratio of the bias current. $V_{BP2}$ is not used to form a current mirror. Its value is,

$$V_{BP2} = V_{DD} - (|V_t| + 2|V_{ovP}|).$$

(3-23)

Unit devices are used to increase matching between the FETs. The transistors in the comparator can sink and source bias current based on the ratio of unit devices between the bias circuit FETs and the comparator FETs. The unit devices in the comparator that will act as current sinks and sources require large lengths to give large small signal output resistances. Making $L = 10 \mu m$, the small signal output resistance $r_0$ of the transistors will be over $10 M\Omega$ when in saturation\(^7\). The unit device width is determined by the minimum operating $V_{DD}$ for the bias circuit [99],

$$V_{DD(min)} = 2V_t N + 3V_{ovN} + 2V_{ovP}.$$  

(3-24)

Using the widths in Table 3.3 and the parameters from the PDS, the minimum supply voltage is approximately $2.2 V$. Thus, when $V_{DD}$ is below $2.2 V$, the bias circuit cannot set up the correct bias voltages and the comparator will not operate as designed.

\(^7\) The $r_0$ values are estimated from a datasheet available through XFAB on signing an NDA. The exact parameter estimates cannot be released for this reason.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Calculated $W/L$</th>
<th>After Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$W/\mu m$</td>
<td>$L/\mu m$</td>
</tr>
<tr>
<td>$B_{P1},B_{P2},B_{P4},B_{P5},B_{P6}$</td>
<td>$6 \times 2.2/10$</td>
<td>2.2</td>
</tr>
<tr>
<td>$B_{P3}$</td>
<td>$2 \times 2.2/10$</td>
<td>2.2</td>
</tr>
<tr>
<td>$B_{N1},B_{N2},B_{N4}$</td>
<td>$6 \times 2.2/10$</td>
<td>2.2</td>
</tr>
<tr>
<td>$B_{N3}$</td>
<td>$2 \times 2.2/10$</td>
<td>2.2</td>
</tr>
</tbody>
</table>
3.7.2. Comparator Operation

The comparator shown in Figure 3.17 consists of two stages. The first stage is a folded cascode amplifier with a positive feedback latch. The second stage is a level shifter with zero static current draw. The folded cascode amplifier and latch are made up from N₁ through N₈ and P₁ through P₄.

![Comparator schematic](image)

The folded cascode amplifier provides preamplification and is made up by transistors N₁ to N₄ and P₁ to P₄. Transistors P₁ and P₂ are each biased to source a current Iᵢ. N₃ and N₄ together sink a current Iₛₛ. If the inputs to the gates of N₁ and N₂ are equal both transistors will sink Iₛₛ/2 from the bias currents Iᵢ. Thus, the bias currents flowing through P₃ and P₄ are both Iᵢ - Iₛₛ/2 when vᵢᵣ₊ and vᵢᵣ₋ are equal.

A small signal differential input voltage vᵢ Airbnb = vᵢᵣ₊ - vᵢᵣ₋ sets up a differential current in the amplifier,

\[ i_{id} = i_{dN1} - i_{dN2} = -g_m v_{id}. \]  

(3-25)

Considering one half of the differential circuit, equations (3-7) and (3-9) can be used to find the input resistances of P₃ and P₁. The drain of P₃ has an input resistance of rₒₚ₃ ≈ 1/(gₘₚ₃) whereas P₁ has a much greater resistance of ≈ rₒₚ₄. Therefore, most of the small signal current flows through P₃ and P₄.
It can be shown that [99],

\[
    i_{dp3} = -i_{dp4} = -\frac{g_m v_{id}}{2}
\]

where the transconductance of \( N_1 \) and \( N_2 \) are equal such that \( g_{mN1} = g_{mN2} = g_m \). Adding the small signal current \( i_{p3} \) and bias current \( I_{P3} \) gives,

\[
    i_{p3} = I_B - \left( g_m \frac{v_{id}}{2} + \frac{I_{SS}}{2} \right) \\
    i_{p4} = I_B + \left( g_m \frac{v_{id}}{2} - \frac{I_{SS}}{2} \right)
\]

These are the currents flowing into the latch. The differential current triggers the latch when \( i_{diff} = k' (2I_B - I_{SS}) \) or equivalently when \( v_{id} = k' (2I_B - I_{SS}) / g_m \), and the outputs switch from high to low or low to high. The second stage of the comparator pulls the inputs to ground or to \( V_{DD} \) giving a rail to tail output.

### 3.7.3. Comparator First Stage Design

Some key definitions and design equations for the comparator are presented in Table 3.4 and derived in Appendix A. The device sizes and parameters are presented in Table 3.5 at the end of the section. Some of the values are modified after simulation due to factors including body effect, short channel effect, etc. These are not accounted for in the calculations and need to be corrected for in simulation.

| Input stage transconductance | \( g_{mN1} = \sqrt{\mu n C_{ox} I_{SS} W/L} = \sqrt{k_1 I_{SS}} \) | (3-28) |
| Beta Ratio | \( \hat{\beta} = \frac{k_B - k_A}{k_B + k_A} \) | (3-29) |
| Threshold Voltage | \( V_{th} = \hat{\beta} \left( \frac{2I_B - I_{SS}}{g_m} \right) \) | (3-30) |
| Threshold mismatch from \( \beta \) ratio | \( \varepsilon = 1 - \frac{\Delta M^2 + M(\Delta - 1) - 1}{\Delta M^2 + M(1 - \Delta) - 1} \) | (3-31) |

The following section will explain in detail the necessary sizing for each transistor in the comparator.
Latch

The latch is the decision circuit of the comparator. It is used to switch the differential output if the differential input voltage is greater than some threshold. Noise on the inductive pickup can cause the comparators to turn on at the incorrect times. To avoid this, 75mV of hysteresis is designed into the comparator. The input voltage to the comparator will be halved by a voltage divider making the total hysteresis 150mV. An offset is also introduced in the comparator to prevent reverse currents from the load to the pickup at turn off. Equation (3-30) from Table 3.4 is used to place constraints on the latch. The threshold is set by changing the folded cascode input gain $g_m$, either of the bias currents and the beta ratio. The beta ratio in (3-10) is a ratio between \( k = \mu C_{ox} W/L \) of $N_5$ to $N_7$ where $k_{N5} = k_{N8} = k_A$ and $k_{N6} = k_{N7} = k_B$ and can be written as,

$$ \hat{\beta} = \frac{(W/L)_B - (W/L)_A}{(W/L)_B + (W/L)_A} $$

There is a limit to how large the ratio $\hat{\beta}$ can be. For switching to occur,

$$ v_{id} \geq \hat{\beta} \left( \frac{2I_B - I_{SS}}{g_m} \right) $$

which can be rearranged to give,

$$ g_m v_{id} \geq \hat{\beta} (2I_B - I_{SS}) \equiv i_{id} \geq \hat{\beta} (2I_B - I_{SS}) $$

The differential current is limited by $I_{SS}$ such that $i_{id} \leq I_{SS}$ resulting in,

$$ \hat{\beta} \leq I_{SS} / (2I_B - I_{SS}) $$

If $I_B = \alpha I_{SS}$,

$$ \hat{\beta} \leq 1 / (2\alpha - 1) $$

The condition $I_B > I_{SS}$ should be met to avoid $P_3$ or $P_4$ going into cutoff when $i_{id} = I_{SS}$. Making $I_B = 1.2I_{SS}$ prevents this and allows $\hat{\beta}$ to go as high as 0.714. As $i_{id}$ approaches $I_{SS}$, the differential amplifier moves out of the linear region used for small signal analysis and $i_{id} \neq g_m v_{id}$. To ensure the input stage remains in the linear region of operation while differential voltage is close to the threshold voltage, the threshold voltage is set such that $i_{id} = 0.5I_{SS}$ at the switching point. This constrains the design further as,

$$ i_{id} = g_m v_{id} = 0.5I_{SS} = \hat{\beta} (2I_B - I_{SS}) $$

making $\hat{\beta} = 0.357$. Setting $k_B = 2k_A$ makes $\hat{\beta} = 1/3 \approx 0.357$. This gives a differential current of $i_{id} = 0.467I_{SS}$ at the switching point, well within the linear region of the differential amplifier. To introduce offset the design can be modified such that $Mk_{N5} = Mk_{N6} = Mk_{N8} = k_7$, and the threshold voltages are,
\[
V_{thp} = 0 \\
V_{thn} = -\frac{M - 1}{M + 1} \left( \frac{2I_B - I_{SS}}{g_m} \right).
\] (3-35)

The latch uses unit transistors to improve matching. Thus, \( M \) in the beta ratio is introduced via adding unit transistors. To reduce the load capacitance and improve the rise time and hence delay of the comparator, the unit transistor size for the latch should be as small as possible while still meeting matching requirements. Equation (3-29) can be re-arranged to find the minimum \( W \) and \( L \) for the unit transistor based on matching constraints,

\[
\Delta = \frac{\varepsilon(1 - M) + 2M}{\varepsilon(M^2 - M) + 2M}
\] (3-36)

where \( \varepsilon = (V_{th} - V_{th\text{(actual)}})/V_{th} \) is the maximum allowable threshold error and \( \Delta = M k_A / k_B \) is the ratio of the desired and actual mismatch between \( N_5 \) and \( N_6 \). \( \Delta \) is one if the unit transistors are identical. Setting the maximum two-standard-deviation error in threshold to \( \pm 5\% \) and knowing \( M = 2 \) gives a maximum gain factor mismatch of \( \Delta = 3.66\% \). The Pelgrom coefficients provided by the foundry can be used to calculate the necessary area for the required mismatch. Using the coefficient for gain factor mismatch and the required area to keep mismatch within the desired limit is\(^8\),

\[
W_{eff}.L_{eff} = \left( \frac{A_B}{\sigma(\Delta \beta / \beta)} \right)^2 = 0.317\mu m^2.
\]

This is for well laid out devices with best possible matching. To avoid short channel effects \( L \) is set to \( 1.05\mu m \), and \( W \) is set to \( 4W_{min} \) (0.88\( \mu m \)) giving an area approximately 2.9 times larger than necessary. This gives an estimated standard deviation using the Pelgrom coefficients of 2.8\% in the comparator threshold value due to process variation in the latch transistors.

**Bias Currents**

The ratio of the bias currents has already been set at \( I_B = 1.2I_{SS} \). The value of the bias currents can be determined by the desired slew rate. There will be two stages before a tapered buffer and the max delay wanted is approximately 10\( ns \) (1\% of the input sine wave cycle at 1MHz) so the rise time should be 5\( ns \) per stage. Consider the low to high rise time of \( V_{A+} \). There are three transistor gates from \( N_5, N_6 \) and \( N_9 \) contributing to a load capacitance \( C_L \) that

\(^8\) The actual value of the Pelgrom coefficient cannot be given as a NDA must be signed to view the PDS.
must be charged. The positive feedback of the latch makes an analytical solution for the rise time intractable. Simulation was used to find the rise and fall times over a range of bias currents with $I_B$ set to $1.2I_{SS}$. $I_{SS}$ and $I_B$ were varied via changing the number of unit devices each with width and length equal to the unit device of the bias circuit. An $I_{SS}$ of $13.3\mu A$ and $I_B$ of $16\mu A$ gave rise and fall times of $7.6nS$ and $6nS$ for $V_{A+}$ and $6nS$ and $9nS$ for $V_{A-}$ respectively. The difference in rise and fall times between $V_{A+}$ and $V_{A-}$ arises due to the fact that $N_7$ is twice as large as the other latch transistors. For the above bias currents, twenty unit transistors are used for $N_3$ and $N_4$ such that $(W/L)_{N3} = (W/L)_{N4} = 44\mu m/10\mu m$. Twenty-four unit transistors were used for $P_3$ and $P_4$ making $(W/L)_{P1} = (W/L)_{P2} = 52.8\mu m/10\mu m$.

$N_1$, $N_2$ and the Threshold Voltage

As $I_{SS}$, $I_B$ and $\hat{\beta}$ are known $(W/L)_{N1}$ and $(W/L)_{N2}$ can be found using (3-30),

$$g_m = \frac{\hat{\beta}}{V_{th}} \approx 83 \mu A/V.$$  

The $W/L$ ratio can be found with equation (3-14) and the gain factor $k'$ from the process specifications,

$$(W/L)_{N1} = \frac{(g_m)^2}{k'nI_{SS}} \approx 2.7.$$  

A length $L = 1.05\mu m$ results in short channel effects having little impact. Therefore, a width of $W \approx 2.85\mu m$ provides the correct width to length ratio. When tested in simulation, the gain factor $\beta'$ for a device with a $1\mu m$ gate length was approximately half the value provided in the process specifications. Using the simulated $\beta'$ value,

$$(W/L)_{N1} = \frac{(g_m)^2}{k'nI_{SS}} \approx 6.$$  

With $L = 1.05\mu m$ the widths for $N_1$ and $N_2$ are $W \approx 6.3\mu m$. Using Pelgrom coefficients, the transistor area of $6.09\mu m$ gives an expected drain current mismatch of approximately $1.5\%$. 

85
Both $P_3$ and $P_4$ are sized identically. Therefore, only $P_3$ is analysed. The primary purpose of $P_3$ is to stop the load and voltage at node $V_{A+}$ affecting $N_1$. The half circuit of Figure 3.18 simplifies the analysis for $P_3$ and $P_4$.

From (3.8), the resistance looking into the source of $P_3$ is,

$$R_{P3} = \frac{r_0 + Z_L}{1 + g_m r_0} \approx \frac{1}{g_m P_3}$$

(3.37)

where $Z_L$ is the output impedance at node $V_{A+}$. $r_0$ is on the order of $1M\Omega - 10M\Omega$ making the approximation $R_{P3} = 1/g_m P_3$ accurate. Consequently, the output impedance has a negligible effect on the resistance seen when looking into the source of $P_3$.

Providing $P_3$ stays in saturation the following equation holds,

$$V_{SP3} = V_{BP2} + V_{tp} + \sqrt{2I_{DP3}/k_{P3}}$$

where $V_{SP3}$ is the voltage at the source of $P_3$. This voltage must not put $P_1$ into cutoff. Setting $V_{SP3} \leq V_{DD} - |V_{ovP1}|$ will keep $P_1$ in saturation. This can be achieved by sizing $P_3$ such that,

$$\left(\frac{W}{L}\right)_{P3} \geq \frac{2I_{DP3}}{k_P (V_{DD} - |V_{ovP1}| - V_{BP2} - |V_{tp}|)^2}.$$  

(3.38)

Noting $V_{BP2} = V_{DD} - 2|V_{ovP1}|$ from (3.35), the maximum possible current through $P_3$ is $I_B$ and $|V_{ovP1}| = \sqrt{2I_B/k_{P1}}$. The width to length ratio can be re-written as,
\[
\left(\frac{W}{L}\right)_{p3} \geq \frac{2I_B}{k_p'(|V_{ovP1}| - |V_{tp}|)^2} = \frac{2I_B}{\left(\sqrt{2I_BL_{P1}/W_{P1}} - \sqrt{k_p'|V_{tp}|}\right)^2}.
\]

Using the parameters from the process specifications for \(k'\) and \(V_t\) and because the following parameters have been set \(W/L_{P1} = 5.28\) and \(I_B = 16\mu A\), the width to length ratio is,
\[
\left(\frac{W}{L}\right)_{p3} \geq 7.43.
\]

To allow for process variation and allow for variation in \(I_B\), the width of \(P_3\) is doubled to \((W/L)_{p3} = 12\mu /1\mu\).

**Input Voltage Range and Output Voltage Swing**

Each transistor in the current sink composed of \(N_3\) and \(N_4\) requires a voltage drop of \(V_{ov} = \sqrt{2I_{SS}/k} \approx 0.18V\) across it to remain in saturation. The minimum voltage at the drain of \(N_3\) is approximately 0.36V. The minimum common mode input voltage is \(v_{CMmin} = 0.36 + V_tn + V_{ovN1}\). From simulation the overdrive voltage for \(N_1\) is \(V_{ovN1} = 0.16V\). This results in a minimum common source voltage of,
\[
v_{CMmin} = 1.21V.
\]

The largest common mode voltage is constrained by preventing the input transistors from entering the triode region. This can be ensured by maintaining the input common mode voltage below,
\[
v_{CM(max)} = Vtn + VDD - V_{OVP1} \approx VDD + 0.31.
\]

The output voltage from the first stage \(V_{A+}\) swings from approximately,
\[
V_{A+(high)} = \sqrt{(2I_B + g_m v_{id} - I_{ss})/k_{N5}} + Vtn
\]
when \(v_{id}\) is negative to,
\[
V_{A+(low)} \approx 0
\]
when \(v_{id}\) is positive. When \(V_{A+}\) is low \(N_6\) is in the triode region and \(v_{DS} \approx 0\). Substituting the calculated bias currents and \(g_m v_{id} = g_m v_{th}\) at the threshold voltage into (3-40) gives a high output voltage of,
\[
V_{A+(high)} \approx 1.53V.
\]

\(V_{A-(high)}\) is slightly lower than \(V_{A+high}\) as \(g_m v_{id} = 0\) at the threshold. Consequently,
\[
V_{A-(low)} \approx 1.41V.
\]
Table 3.5: Comparator first stage transistor sizes and design variable summary. W is width, L is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Calculated $W/L$</th>
<th>After Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$W (\mu m)$</td>
<td>$L (\mu m)$</td>
</tr>
<tr>
<td>$N_1, N_2$</td>
<td>5.8/1.05</td>
<td>5.06</td>
</tr>
<tr>
<td>$N_3, N_4$</td>
<td>44/10</td>
<td>2.2</td>
</tr>
<tr>
<td>$N_6$</td>
<td>1.76/1.05</td>
<td>0.88</td>
</tr>
<tr>
<td>$N_5, N_7, N_8$</td>
<td>0.88/1.05</td>
<td>0.88</td>
</tr>
<tr>
<td>$P_1, P_2$</td>
<td>52.8/10</td>
<td>2.2</td>
</tr>
<tr>
<td>$P_3, P_4$</td>
<td>12/1</td>
<td>6</td>
</tr>
</tbody>
</table>

Parameter | Calculated | Simulated | Unit |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ss}$</td>
<td>13.333</td>
<td>13.333</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_B$</td>
<td>16</td>
<td>17</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$V_{th}$</td>
<td>75</td>
<td>75</td>
<td>$mV$</td>
</tr>
</tbody>
</table>

3.7.4. Second Stage

The second stage of the comparator uses the level shifter of Figure 3.19 to convert the small output voltage of the first stage into a rail to rail output. The device sizes are summarised in Table 3.6 below.

Table 3.6: Transistor sizes calculated for the comparator’s second stage. W is width, L is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Calculated $(W/L)$</th>
<th>After Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$W (\mu m)$</td>
<td>$L (\mu m)$</td>
</tr>
<tr>
<td>$N_9, N_{10}$</td>
<td>0.22/0.35</td>
<td>0.22</td>
</tr>
<tr>
<td>$P_5, P_6$</td>
<td>0.22/1.5</td>
<td>0.22</td>
</tr>
</tbody>
</table>

When $V_{out^+}$ is high $P_6$ is in cutoff, $V_{out^-}$ is low and $P_5$ is in triode. For the outputs to flip, $I_{D9} > I_{D5} \equiv \beta_{N9}(V_{GS} - V_{th})^2 > \beta_{P5}(V_{DD} - V_{out^+} - V_{th})^2$. Therefore, a positive voltage at $V_{A+}$ gives a low output voltage at $V_{out^+}$. When $N_9$ is on, $P_5$ is off whereas when $P_5$ is on, $N_5$ is off. Therefore, the level shifter has zero static current draw. Moghe, Lehmann and Piessens provide a method of sizing the NMOS and PMOS transistors [105],

$$\frac{W}{L} = 2 \frac{K_p}{K_n} \left( V_{DD} - |V_{tp}| \right) \left( V_{DDL} - V_{th} \right)$$  \hspace{1cm} (3-42)

where $V_{DDL}$ is the low logic level, in this case $V_{A+}$ and $V_{A-}$.  

88
Moghe et al. note that the NMOS/PMOS ratio should be set for the slow N/fast P corner with maximum $V_{DD}$ and minimum $V_{DDL}$ for the latch to work over all process corners and possible voltages [105]. To minimise the gate capacitance at $V_{A+}$, $(W/L)_{N9}$ is set to the minimum size with $(W/L)_{N9} = 0.22\mu m/0.35\mu m$. Rearranging (3-42) gives,

$$\left(\frac{W}{L}\right)_{P5} = \left(\frac{W}{L}\right)_{N9} \frac{K'_N}{2K'_P} \frac{(V_{DDL} - V_{tr})^2}{(V_{DDH} - |V_{tp}|)|V_{tp}|}.$$ 

Using a maximum $V_{DDH}$ of 3.6V, minimum $V_{DDL}$ of 1.41V and the gain factor values for $K'_N$ and $K'_P$ from the process specifications,

$$(W/L)_{P5} \approx 0.6(W/L)_{N9} \approx 0.22\mu m/0.6\mu m.$$ 

To ensure switching occurs at the slow N/fast P corner and with process variation the length of $P_5$ is made 2.5 times larger than calculated. Therefore, the final value is,

$$(W/L)_{P5} = 0.22\mu m/1.5\mu m.$$ 

Matching is not a high priority for the latch as it is digital and operates correctly as long as the NMOS transistors have enough drive strength to pull the outputs low.

### 3.7.5. Comparator Simulation

Simulation was used to verify the comparator and bias circuit design. The comparator schematic was created as per the calculated values. Only $N_1$ and $N_2$ were modified because the transconductance was significantly lower than expected given the bias conditions, possibly due to short channel effects. As such, the width of $N_1$ and $N_2$ were increased from 5.6$\mu m$ to 10.12$\mu m$ to account for the difference. The bias current $I_B$ was also 1$\mu A$ larger than expected at 17$\mu A$ due to channel length modulation as a consequence of different $V_{DS}$ between $P_1, P_2$ and the bias transistors.
To test the comparator, the negative input was held at $1.65V$, and the positive input was given a square wave with a high voltage of $1.75V$ and low voltage of $1.475V$. $V_{A+}$ and $V_{A-}$ had high and low outputs of approximately $1.24V$ and $0.03V$ respectively. The delays were found when the input was 100% and 0% of its positive value until the output reached 90% and 10% of the highest output voltage respectively. The measurements for the first and second stage positive outputs can be seen in Figure 3.20 and Figure 3.21. The low to high (LH) and high to low (HL) delays for $V_{A+}$ were found to be approximately $7.9\,\text{nS}$ and $6.6\,\text{nS}$ respectively. For $V_{A-}$, the LH delay was $5.7\,\text{nS}$, and the HL delay was $9.9\,\text{nS}$. The overall delay in the first stage from the input voltage switching to the second stage output switching was approximately $10\,\text{nS}$ and $11.5\,\text{nS}$ high to high (HH) delay and $11.7\,\text{nS}$ and $7.4\,\text{nS}$ low to low (LL) delay for $V_{out+}$ and $V_{out-}$ respectively.

![Figure 3.20: Simulated comparator rise and fall times for $V_{A-}$ and $V_{A+}$ respectively.](image-url)
3.8. Bridge-Driver

The rectifier bridge-driver refers to the combined voltage divider, comparator, multiplexor and buffer. Directly attaching the pickup nodes to the comparator input is not feasible as the voltage would damage the low voltage input transistors. The HV transistors used for the rectifier bridge are not suitable for the input as they have low transconductance and poor matching parameters. A voltage divider and over-voltage protection circuit are used to move the input voltage into the comparators’ input range. Between the comparator and output buffer, a multiplexor is used for enabling and disabling shorting control. The output stage requires a large current driving capability to drive the large capacitive load presented by the gate of the NMA rectifier transistors. A tapered buffer is used to implement the output stage.

3.8.1. Voltage Divider and Overvoltage Protection

The hysteresis designed into the comparator is $75m\text{V}$ with a $-75m\text{V}$ offset. The differential input is measured between the pickup and ground. From (3-39), the comparator cannot work with a common mode input voltage below $1.21V$. Hence the comparator cannot directly measure the pickup voltage or ground. To overcome this, the input is halved with respect to $V_{\text{rec}}$ using the resistive voltage divider of Figure 3.22 where $V_{\text{rec}} = V_{RL}$ is the rectifier load.
voltage. This maintains the comparator common mode voltage at approximately 1.65V when the input voltage is below ground by the comparator threshold voltage.

The resistive divider also increases the overall hysteresis to 150mV. The divider is designed to give accurate matching between the branches. Each resistor is 50KΩ giving each branch 200KΩ of resistance. When $V_{RL} = 3.3V$, the power loss in the grounded branch is 55μW and less than 27μW in the remaining two branches with AC inputs. The RC delay at 1MHz introduced by the divider is $\cong 3.7nS$.

![Figure 3.22: Voltage divider circuit with over-voltage protection.](image)

6V NMOS transistors are used to prevent overvoltage of the comparator inputs. The NMOS transistor gates are attached to $V_{rec}$ forcing the transistors into cutoff as $V_{p1}$ and $V_{p2}$ approach $V_{rec}$. The NMA transistors are made large enough to have a negligible effect on the resistive divider.
3.8.2. **Shorting Control Multiplexor**

The multiplexor circuit in Figure 3.23 is used as an input for shorting control. Transistors $M_7$ and $M_8$ form a ‘pass transistor’. As an NMOS and a PMOS transistor are used and have complementary inputs, the pass transistor can pass positive and negative logic changes effectively. One pass transistor ($M_7$ and $M_8$) is attached to the comparator output and the other pass transistor ($M_9$ and $M_{10}$) is attached to $V_{\text{start}}$ which is equal to the rectifier output $V_{\text{rec}}$. The shorting control input $SC$ is inverted to $\overline{SC}$ using the inverter composed of $M_{12}$ and $M_5$. $SC$ and $\overline{SC}$ act as the select input to the multiplexor by controlling which pass transistor is on. If the shorting control signal $SC$ goes high, the input line attached to $V_{\text{start}}$ is selected which turns the NMA rectifier bridge transistors on. The transistor sizes for the multiplexor are presented in Table 3.7.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$M_7, M_9$</th>
<th>$M_8, M_{10}$</th>
<th>$M_{12}$</th>
<th>$M_{13}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>W ($\mu m$)</td>
<td>2</td>
<td>4</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>L ($\mu m$)</td>
<td>0.35</td>
<td>0.3</td>
<td>0.3</td>
<td>0.7</td>
</tr>
<tr>
<td>NF</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>N</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

3.8.3. **Tapered Buffer**

The tapered buffer in Figure 3.23 consists of two inverters with the shorting control multiplexor between. For a minimum overall propagation delay in the tapered buffer, the delay between each inverter should be equal. This has been set through simulation. The delay from the end of the comparator second stage output $V_{\text{out+}}$ switching to the third inverter gate $V_{\text{out}}$ switching is $2.9nS$. The transistor widths, lengths and number of fingers vary as an attempt to keep a low current density in the metal tracks leading to the devices. As the transistors gain more fingers, the lengths are generally increased to allow enough metal routing to reach the device.

The first inverter in the tapered buffer is supplied from $V_{\text{start}}$. This forces the output of the buffer to be low until $V_{\text{start}}$ is attached to $V_{\text{rec}}$ by the start-up circuit.
Table 3.8: Transistor sizes for shorting control multiplexor. W is width, L is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$M_1$</th>
<th>$M_2$</th>
<th>$M_3$</th>
<th>$M_4$</th>
</tr>
</thead>
<tbody>
<tr>
<td>W ($\mu$m)</td>
<td>1.7</td>
<td>3</td>
<td>1.76</td>
<td>4.4</td>
</tr>
<tr>
<td>L ($\mu$m)</td>
<td>0.7</td>
<td>0.4</td>
<td>1</td>
<td>0.6</td>
</tr>
<tr>
<td>NF</td>
<td>1</td>
<td>1</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>N</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

3.8.4. Simulation

The important parameters for the comparator are hysteresis and offset with parasitics included, the effect of process variation on hysteresis and offset, delay from the voltage divider, total delay with parasitics and power dissipation. The test setup is shown below in Figure 3.24. The output power is measured including the voltage divider using a square wave with a period of $1\mu$S.

Figure 3.23: Bridge-driver circuit with multiplexor for shorting control input. Multiplexor is circled in blue.
Hysteresis and Offset

The hysteresis and thresholds were found using a DC sweep with and without layout parasitics included and were the same in both cases. Therefore, parasitics were not used in the Monte Carlo simulation to reduce computation time. A 500 point Monte Carlo simulation was run with $6\sigma$ models to assess the effects of process variation. The results are shown in Table 3.9. The simulated values are close to the designed values. Process variation has a moderate effect on threshold and hysteresis values but will not prevent the circuit from functioning correctly. 95\% of the circuits ($2\sigma$) will be within $\pm 26mV$ ($\pm 17.4\%$) of the correct hysteresis.

Delay

The high to high (HH) and low to low (LL) delays were measured from the input $V_{P1}$ to the output $V_{OUT}$. For the HH delay, a voltage 90\% of the final high square wave value was used as the start and end measurement point for of $V_{P1}$ and $V_{OUT}$ respectively. A voltage 10\% of the final low square wave value was used as the start and end measurement point for the LL delay. The input $V_{P1}$ was a square wave with a 0.35V step from -0.25V to 0.1V with 1ns rise and fall times. Parasitics from the NMOS driver and voltage divider cell layouts were added. A 500 point Monte Carlo simulation was run without parasitics to characterise the change in delay with process variation. The delay results are also presented in Table 3.9.
Table 3.9: Simulation result summary for the NMOS Driver.

<table>
<thead>
<tr>
<th>Delay</th>
<th>PEX</th>
<th>σ (no PEX)</th>
<th>Range (no PEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LL</td>
<td>31.74 ns</td>
<td>0.96 ns</td>
<td>17.8 ns to 24.8 ns</td>
</tr>
<tr>
<td>HH</td>
<td>30.16 ns</td>
<td>0.89 ns</td>
<td>17.4 ns to 23.2 ns</td>
</tr>
<tr>
<td>Voltage Divider</td>
<td>3.74 ns @ 1 MHz</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Thresholds</th>
<th>Mean</th>
<th>σ</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>High</td>
<td>−6.3 mV</td>
<td>11.8 mV</td>
<td>−35.5 mV to 32.9 mV</td>
</tr>
<tr>
<td>Low</td>
<td>−152.6 mV</td>
<td>14.8 mV</td>
<td>−213.2 mV to −107 mV</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>147 mV</td>
<td>13 mV</td>
<td>108.1 mV to 185.3 mV</td>
</tr>
</tbody>
</table>

Power Draw with $1\mu S$ Square Wave Period (excluding voltage divider)

$V_{DD} = 3.3V$ | 202 $\mu W$ | - | - |

3.9. Shorting Controller

The shorting controller compares the rectifier load voltage $V_{rec}$ with a reference voltage and triggers shorting control when $V_{rec}$ reaches an upper safe operating voltage. Once the load voltage has dropped below a safe threshold, shorting control is disabled and the rectifier continues.

3.9.1. Design

The comparator of section 3.7 was used as the basis for the shorting control circuit in Figure 3.25. The input $V_{ref}$ comes from a voltage reference and is expected to be 1.1V. The second input comes from the rectifier load voltage $V_{rec}$. The maximum voltage the 3.3V transistors can withstand is 3.6V. Therefore, the comparator was desinged to short the coil when $V_{DD}$ approaches this voltage. 3.575V was chosen as the high threshold to keep $V_{DD}$ below 3.6V despite process variation and delay in the comparator. The comparators have a positive threshold voltage $V_{th+} = 0V$ and a negative threshold voltage $V_{th-} = −150 mV$. The threshold is set with the voltage divider such that,

$$V_{HIGH} = \frac{V_{ref} R_2}{(R_1 + R_2)}$$

$$V_{LOW} = \left(\frac{V_{ref} - V_{th-}}{R_2}/(R_1 + R_2)\right)$$

A resistive voltage divider with a ratio of $4R_1 = 9R_2$ makes the designed high threshold $V_{HIGH} = 3.575V$, the low threshold $V_{LOW} \approx 3.33V$ and the hysteresis $V_{HYST} \approx 245 mV$. $V_{rec}$ powers the comparator and output inverter. Resistors $R_1$ and $R_2$ consist of $100 k\Omega$ unit resistors allowing accurate matching and, in turn, an accurate resistive divider ratio. The total resistance of $R_1$ and $R_2$ is $650 K\Omega$ giving an average power draw of approximately $20 \mu W$.
with a load voltage of 3.6\text{V}. The first inverter after the comparator is powered from $V_{\text{start}}$ such that $SC1$ will always be low until the start-up circuit has gone high.

$SC$ acts as the select for the multiplexor in the bridge-driver. When it is activated the drivers both go high turning on both NMOS pass transistors and shorting the coil. This makes the voltage on either side of the coil approach 0\text{V} turning on the PMOS pass transistors and shorting the load to ground. To prevent this, the circuitry in Figure 3.26 is used. Normally $SC$ is high and $SC2$ is low shorting the pickup voltage $V_{P1}$ to the PMOS pass transistor gate $V_{GP2}$.

![Figure 3.25: Shorting control circuit with voltage divider.](image)

When shorting control is activated $SC$ and $SC2$ go low and high respectively. $V_{GP2}$ is shorted to $V_{DD}$ putting the PMOS pass transistors in cut-off. 6\text{V} FETs are used as they are subject to voltages exceeding 3.6\text{V}.
3.9.2. Simulations

Switching delay and shorting threshold voltage simulations were run using the simulation test setup in Figure 3.27. The switching delay was simulated including parasitics from the layout. Threshold voltages were simulated with parasitics, using Monte Carlo (MC) analysis and with a temperature sweep. MC simulations and temperature sweeps were run without parasitics as they had little effect on the thresholds. The results of the different simulations are summarised in Table 3.10. For all of the simulations, $V_{\text{ref}}$ and $I_{\text{ref}}$ were 1.1V and 4μA respectively.

![Diagram](image1)

Figure 3.26: Shorting of the load to ground through the PMA transistors is prevented by the PMA shorting control circuitry.

![Diagram](image2)

Figure 3.27: Test setup for shorting control with 1.1V reference voltage and 4μA reference current. Output capacitance C1 and C2 are taken from parasitic extraction of final circuit.


**Delay**

For the high to low (HL) delay, a transient analysis was run, the input voltage was stepped from 3.2V to 3.65V and the delay to $SC$ was measured. The output inverter is included for accurate capacitive loading. The additional capacitance $C_1$ attempts to model the parasitics from the full layout parasitic extraction. LH delay was measured by stepping the input in the opposite direction and measuring the delay.

**Threshold**

A DC simulation was used to find the switching voltages and hysteresis. Transient analysis was used for the Monte Carlo simulation and temperature sweep. V1 was set as a ramp with 3.25V minimum, 3.65V peak and 500μs fall and rise time to ensure the comparator delay did not affect measurement.

500 simulations using device and lot variation were run using the $6\sigma$ Gaussian models provided by XFAB. $V_{\text{high}}, V_{\text{low}}$ and $V_{\text{hyst}}$ were extracted for each run.

The temperature sweep was run in $1^\circ$ steps from $0^\circ – 70^\circ$.

<table>
<thead>
<tr>
<th></th>
<th>PEX</th>
<th>$\sigma$</th>
<th>Range</th>
<th>$0^\circ – 70^\circ$ Sensitivity</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Delay</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HL</td>
<td>29.77ns</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>LH</td>
<td>48.76ns</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>Thresholds</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High</td>
<td>3.568V</td>
<td>16.8mV</td>
<td>3.5V – 3.63V</td>
<td>$-68.3ppm/^\circ$</td>
</tr>
<tr>
<td>Low</td>
<td>3.296V</td>
<td>21.9mV</td>
<td>3.25V – 3.36V</td>
<td>$-666ppm/^\circ$</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>272mV</td>
<td>24mV</td>
<td>192mV – 347mV</td>
<td>$-598ppm/^\circ$</td>
</tr>
<tr>
<td><strong>Power with 3.6V $V_{\text{rec}}$</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>$-156.37\mu W$</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
3.10. Voltage and Current Reference

The rectification control comparators and shorting control comparator require an accurate current reference. Additionally, the shorting controller requires an accurate voltage reference to define the shorting threshold voltages. A bandgap voltage reference doubling as a current reference can provide an accurate voltage that is insensitive to temperature changes. An in depth introduction to bandgap voltage references can be found in [99] and [101].

3.10.1. Required Accuracy of the Voltage and Current Reference

The voltage and current reference accuracy is constrained by the key parameters of the comparators and shorting controller.

**Comparator and bridge-driver accuracy**

The three key parameters of the comparator affected by current variation are the hysteresis, the low to high (LH) and high to low (HL) delay. Using (3-10) and (3-11), the change in threshold voltage from a change in the bias current is,

\[ V_{th1} = V_{th2} \sqrt{I_{bias1}/I_{bias2}}. \]  

(3-44)

This indicates the threshold voltage is proportional to the square root of the bias current. This helps reduce the hysteresis variation due to current reference variation. A DC sweep was run on the negative input voltage of the bridge-driver with the positive input voltage at 1.5V. The negative input voltage at the switching point was extracted and the sweep was repeated in 11 steps from 3μA to 5μA as can be seen in Figure 3.28. It does not change as expected from (3-44) possibly due to saturation of the bias circuit or input transistors. However, the high threshold variation of \(-5.45mV\) to \(-6.35mV\) and low threshold variation of \(-147mV\) to \(-157mV\) are small compared with the current bias variation.

HH and LL delay are also affected by bias current. A simulation of the bridge-driver with a bias current from 3μA to 5μA is shown in Figure 3.29. The HH delay is affected most and, at worst, increases by 3.8nS which is 18% of the nominal delay at 4μA.

Overall, changes in the bias current affect the parameters of interest, but with a ±25% variation in bias current the comparators would still function correctly.
Figure 3.28: Simulation of high and low threshold variation with bias current.

Figure 3.29: HH and LL delay changes due to current bias variation (without layout parasitics).
Shorting control accuracy

The shorting control thresholds are directly proportional to variations in the voltage reference. Shorting control is designed to limit the load voltage to between $3.575V$ and $3.33V$. The maximum allowable load voltage is $3.6V$. Therefore the voltage reference should not vary by more than $+0.7\%$. A negative variation of more than $-0.9\%$ will result in the lowest load voltage of the rectifier going below the $3.3V$ desired minimum but will not damage the circuit.

3.10.2. Design of the Voltage and Current Reference

The key design limit is a maximum variation in the voltage reference of $+0.7\%$. This includes changes due to temperature, input voltage and process variation. The voltage reference should also work with voltages as low as $2.2V$ which is the minimum operating voltage of the comparator.

The current and voltage reference operates in the same way as the self-biasing voltage reference with cascoded current mirrors described by Grey and Meyer [99]. However, to achieve a lower operating voltage and reduce the effect of channel length modulation, the cascoded current mirrors are replaced with two low-voltage current mirrors with channel length modulation correction. One current mirror, described in [99], is shown in Figure 3.30. The mirror acts much like the Sooch current mirror of Section 3.7. $N_6$ and $N_5$ set up the gate voltage of $N_2$ to $V_t + 2V_{ov}$ such that the gate source voltage is $V_{gs2} = V_{gs1} = V_t + V_{ov}$. $N_4$ has the same gate source voltage as $N_2$. Thus, the drain source voltages of $N_3$ and $N_1$ are equal, and $I_{OUT}$ will match $I_{IN}$ very closely. Only device mismatch will influence the current matching.

The voltage reference utilises two current mirrors as shown in Figure 3.31. The current mirrors force the current in all branches to be identical and hence the source voltages of $N_3$ and $N_1$ will be identical leading to,

$$V_T ln\left(\frac{I_Q}{I_{s1}}\right) = V_T ln\left(\frac{I_Q}{I_{s2}}\right) + I_Q R$$  \hspace{1cm} (3-45) \\
which can be re-arranged to give,

$$I_Q = \frac{V_T}{R_1} ln\left(\frac{I_Q I_{s2}}{I_Q I_{s1}}\right) = \frac{V_T}{R_1} ln(N).$$  \hspace{1cm} (3-46) \\
where $N$ is the ratio of unit devices between $Q_2$ and $Q_1$. The bias voltage is.
\[ V_{\text{bias}} = MI Q R_2 + V_{be3} = M \frac{R_2}{R_1} \ln(N) V_T + V_{be3} \]  

**(3-47)**

where \( M \) is the mirror ratio between \( P_7, P_8 \) and \( P_1, P_2 \) respectively. The input of the left most branch of the current mirror in Figure 3.30 requires the largest operating voltage of \( V_{IN} = V_{Tn} + 2V_{OVn} \). The minimum output voltage for the two right most branches is \( 2V_{OVn} \). As the top current mirror is identical to the bottom mirror, the minimum voltage at which the bias circuit can operated is the larger of,

\[
\begin{align*}
V_{DD(\text{min})} &= V_{Tn} + 2V_{OVn} + 2|V_{OVp}| + V_{BE1} \\
V_{DD(\text{min})} &= |V_{tp}| + 2|OV| + 2V_{OVn} + V_{BE1}.
\end{align*}
\]

**(3-48)**

With \( V_t = |V_{BE}| \approx 0.7V \) and \( V_{OVn} = V_{OVp} = 0.1V \) the minimum operating voltage is 1.8V. A threshold mismatch between two FETs leads to a current mismatch in the drain through the equation \( I_D = k(V_{GS} - V_t)^2 \). This mismatch can be reduced by increasing \( V_{GS} \) and hence \( V_{OV} \). To this end, \( V_{OV} \) was designed to be larger at 0.2V resulting in a minimum 2.2V operating voltage.

---

**Figure 3.30**: Current mirror with minimum supply voltage of \( V_t + 2V_{OV} \) and zero systematic gain offset.

To simplify a common centroid layout and improve matching, \( N = 8 \) was used allowing \( Q_1 \) to be laid out surrounded by the \( Q_2 \) unit devices. Using \( R_1 = 54K\Omega \) and \( R_2 = 216K\Omega \) with \( M = 7/2 \) gives a bias voltage of \( V_{\text{ref}} = 1.1V \). It also allowed the temperature coefficient of \( V_T \) to cancel with that of \( V_{be3} \) resulting in low temperature variation in \( V_{\text{ref}} \). The current reference is taken from another pair of FETs in the same way as \( P_7 \) and \( P_8 \). It is mirrored with a factor of eight increase to get 4\( \mu \)A bias currents for the comparators. The transistor sizing is given in Table 3.11.
The reference circuit naturally starts in an off state where zero current flows. Two transistors are used to pull the gates of the $P_1$ and $P_2$ transistors low until the start-up circuit from Section 3.11 disables them. This forces the voltage reference out of the zero current state.

Table 3.11: Voltage and current reference transistor sizing. W is width, L is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W ($\mu m$)</th>
<th>L ($\mu m$)</th>
<th>NF</th>
<th>Parallel Devices</th>
<th>Series Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{1A}, P_{1B}, P_{2A}, P_{2B}, P_3, P_4, P_6$</td>
<td>3</td>
<td>3</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>$P_5$</td>
<td>3</td>
<td>3</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>$P_7, P_8$</td>
<td>3</td>
<td>3</td>
<td>1</td>
<td>7</td>
<td>1</td>
</tr>
<tr>
<td>$N_{1A}, N_{1B}, N_{2A}, N_{2B}, N_3, N_4, N_6$</td>
<td>1.5</td>
<td>6</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>$N_5$</td>
<td>1.5</td>
<td>6</td>
<td>1</td>
<td>2</td>
<td>3</td>
</tr>
</tbody>
</table>

Figure 3.31: Two low input voltage current mirrors are combined making a low supply voltage, high accuracy bandgap voltage reference and current mirror.
3.10.3. Simulated Performance

The performance of the voltage/current reference can be seen in Table 3.12. The most important parameter was maintaining the voltage bias variation below +0.7%. Some dice will be exposed to small over-voltages before shorting control occurs as the standard deviation is double this. However, the average threshold voltage for the comparator is not actually 0V but $-6mV$, and the voltage reference at body temperature ($\approx 37^\circ C$) is approximately $-2mV$ lower allowing an actual increase in $V_{\text{ref}}$ of 0.9%. Between approximately 25% and 30% of chips will be subject to small over-voltages below 0.1V. To decrease the variation and increase yield, the bias circuit FETs could be made larger to increase matching, the overdrive voltage could be increased or a trimming circuit could be added. Alternatively, the shorting control high threshold could be lowered reducing the shorting control hysteresis and allowing a larger variation.

Table 3.12: The mean bias voltage and bias current are presented as well as the standard deviation (STD) obtained from a 500 point Monte Carlo simulation.

<table>
<thead>
<tr>
<th>Simulated VDD</th>
<th>2.5V</th>
<th>3.5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean $V_{\text{bias}}$</td>
<td>1.10V</td>
<td>1.10V</td>
</tr>
<tr>
<td>Mean $I_{\text{bias}}$</td>
<td>3.98$\mu A$</td>
<td>4.00$\mu A$</td>
</tr>
<tr>
<td>$\sigma$ (mV) $V_{\text{bias}}$</td>
<td>18.14$mV$</td>
<td>18.26$mV$</td>
</tr>
<tr>
<td>$\sigma$ (mV) $I_{\text{bias}}$</td>
<td>243$nA$</td>
<td>244$nA$</td>
</tr>
<tr>
<td>$\sigma$ as % of Mean $V_{\text{bias}}$</td>
<td>1.65%</td>
<td>1.66%</td>
</tr>
<tr>
<td>$\sigma$ as % of Mean $I_{\text{bias}}$</td>
<td>6.10%</td>
<td>6.12%</td>
</tr>
<tr>
<td>Line Regulation 2.5 − 3.5V</td>
<td>1.49$mV/V$</td>
<td></td>
</tr>
<tr>
<td>Temp Coeff (defined in [101])</td>
<td>$-194\mu V/{^\circ C}$</td>
<td></td>
</tr>
<tr>
<td>Power at 3.5V</td>
<td>28$\mu W$</td>
<td></td>
</tr>
</tbody>
</table>
3.10.4. Layout

The accuracy of the reference circuit is highly dependent on the layout quality. As such, the techniques and methods used to ensure accurate matching are covered below.

\(Q_2\) is eight times larger than \(Q_1\) and is made of eight unit devices to improve matching. They are laid out such that \(Q_1\) is in the middle and surrounded by the eight \(Q_2\) transistors to achieve common centroid geometry [85] as shown in Figure 3.32. The metal tracks crossing the device are symmetrical across all \(Q_1\) and \(Q_2\) unit devices. A guard band surrounds the whole transistor group to pick up any minority carriers from the substrate [85].

![Common centroid BJT layout.](image)

It is important that \(N_{2A}, N_{2B}, N_4\) and \(N_6\) all match to keep the currents equal between the branches of the current mirror. \(N_{1A}, N_{1B}, N_3\) and \(N_5\) must also be matched. The layout of Figure 3.33 is used to achieve accurate matching. All FETs are laid out with a common centroid and have symmetric current flow [85]. Dummy devices are used at the ends of all rows to keep the etch rate equal in all polysilicon gates [85]. The PMOS side is similar to the NMOS except \(P_7\) and \(P_8\) also need to be matched. Because there are an uneven number of transistors, the average current flow is not perfectly symmetrical but is still well matched.
Figure 3.33: Common centroid FET layout of the bias circuit with symmetric current flow and guard bands.

The resistors in Figure 3.34 are also laid out with common centroid geometry. Dummy resistors on the top and bottom of the resistor group keep the polysilicon etch rate equal for all devices.

Figure 3.34: Common centroid resistor layout for the reference circuit.
3.11. Start-up Circuit

The start-up circuit has a high output voltage until \( V_{rec} \) has reached the threshold voltage \( V_{start} \) whereupon it will go low. It prevents all of the control circuitry including comparators, shorting control and bias circuits from functioning while \( V_{rec} \) is below a value that can stably power the control circuitry. The circuit shown in Figure 3.35 uses \( M_8 \) to create positive feedback [69], [106]. \( M_8 \) is turned on when the output of the “sense” inverter composed of \( M_5 \) and \( M_4 \) goes below \( V_{DD} - |V_{thp}| \). This happens approximately when the supply voltage rises above the combined threshold voltages of \( M_1, M_2, M_{11}, \) and \( M_{12} \) such that \( V_{DD} = V_{thn} + 3|V_{thp}| \). With the XFAB threshold voltages given in the process design specifications, this value is 2.57V. Once the start-up circuit is triggered, the source of \( M_{12} \) is disconnected from ground by an inverter preventing any static current draw. While the voltage \( V_{rec} \) is rising, there is an area of operation below 0.5V when the circuit is unstable and can trigger. \( V_{rec} \) must move through this region before the gate capacitor of \( M_3 \) can charge. The time until this false start-up happens will be referred to as the false start-up delay. \( M_{13} \) is used to help discharge the gate capacitance of \( M_3 \) if \( V_{rec} \) falls to ground.

![Figure 3.35: Zero static current start-up circuit.](image)
3.11.1. Simulations

The start-up voltage value with parasitics, parameter variation and temperature dependence were measured. Also, the delay time before false start-up with parasitics and statistical variation were measured using the test setup in Figure 3.36.

Start-up Voltage

A ramp with a 100\(\text{ms}\) rise time from 0 to 3V was used as the input. The voltage at which the start-up circuit turned on was measured. Five hundred runs were performed with the Monte Carlo simulation using 6\(\sigma\) device models. The results are presented in Table 3.13 as the standard deviation and range of values.

![Figure 3.36: Test setup for the start-up circuits start up voltage and false start delay.](image)

False Start-up Delay

The false start-up delay was measured as the time delay until start-up circuit turn on from a 0.5V pulse with a 1\(\mu\)s rise time. A five hundred run Monte Carlo simulation was performed to assess the effect of process variation. Based on the measured false start-up delay, the slope of the rectifier load voltage rise must be greater than 6.2\(V/S\) to prevent false triggering.

<table>
<thead>
<tr>
<th>Delay</th>
<th>PEX</th>
<th>(\sigma)</th>
<th>Range</th>
<th>0° – 70° Sensitivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start-up Voltage</td>
<td>2.73V</td>
<td>56.33mV</td>
<td>2.56V to 2.89V</td>
<td>3.26V to 2.57V</td>
</tr>
<tr>
<td>False Start-up Delay</td>
<td>80.36ms</td>
<td>5.3mS</td>
<td>66.32ms to 96.38ms</td>
<td>-</td>
</tr>
</tbody>
</table>
3.12. ADSR Design, Simulation and Layout

The ADSR design utilises the sub-circuits from previous sections in combination with some additional circuitry. Once the connectivity between the sub-circuits has been explained, the physical layout of the full chip will be covered. Lastly, the ADSR efficiency will be predicted from simulations.

3.12.1. Design

The full circuit is shown in Figure 3.38. Five 75 \( \mu m \) by 75 \( \mu m \) bond pads were used for \( V_{DD} \) and GND with ten 75 \( \mu m \) by 75 \( \mu m \) bond pads for \( V_{in-} \) and \( V_{in+} \) to provide adequate metal to prevent electromigration and minimise additional resistance. An additional bias circuit with three 53 \( \mu m \) by 66 \( \mu m \) bond pads (\( V_{DD}, V_{start}, V_{bias} \)) was included allowing the voltage bias value to be measured. Two 53 \( \mu m \) by 66 \( \mu m \) bond pads were connected to the NMA gates allowing control signal measurements. Lastly, two additional 53 \( \mu m \) by 66 \( \mu m \) bond pads with foundry designed 3.3V ESD protection were added, one for \( V_{RL} \) and one for ground. This was necessary as \( V_{RL} \) and ground have direct connections to low voltage circuitry that can be damaged by ESD. \( V_{IN+} \) and \( V_{IN-} \), however, have only high voltage transistors attached. The large total transistor area allows the HV devices to be self-protecting, though the complete design rules required to withstand a 2KV HBM ESD pulse were not followed in order to decrease device size. Thus, anti-static precautions should be taken when handling the dice.

The start-up circuit highlighted in brown has an inverter at the output. The NMOS transistor keeps \( V_{start} \) low until the start-up circuit has triggered. The PMOS transistor provides current to two inverters in each bridge-driver and one inverter in the shorting control circuit. The NMOS transistor and PMOS transistor have \( W = 2 \mu m, L = 0.35 \mu \) and \( NF = M = 1 \) and \( W = 20 \mu m, L = 0.3 \mu, NF = 20 \) and \( M = 1 \) respectively.

An inverter following the bridge-driver is used to control the turn on rise time of the NMA bridge transistors. From Figure 3.37, with shorting control off, \( M_4 \) and \( M_5 \) form a pass transistor allowing \( M_1 \) and \( M_2 \) to drive the NMA bridge transistor gate capacitance together. When shorting control triggers, the gate of \( M_2 \) is pulled to \( V_{DD} \) by \( M_6 \) turning it off. Thus, only \( M_1 \) is on and the turn on rise time of the bridge transistors increase. This reduces the peak current when shoring control is triggered and, additionally, allows the PMA pass
transistor cut-off circuitry to activate first preventing any back current from the load to the pickup. The transistor sizes for the turn on time control output are given in Table 3.14.

![Figure 3.37: Bridge-driver buffer with rise time control.](image)

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$M_1$</th>
<th>$M_2$</th>
<th>$M_3$</th>
<th>$M_4$</th>
<th>$M_5$</th>
<th>$M_6$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W$ ($\mu m$)</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>4</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>$L$ ($\mu m$)</td>
<td>0.6</td>
<td>0.9</td>
<td>1.6</td>
<td>0.7</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>NF</td>
<td>1</td>
<td>12</td>
<td>16</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>N</td>
<td>1</td>
<td>5</td>
<td>5</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 3.14: Transistor sizes for NMOS bridge transistor turn on rise time control. $W$ is width, $L$ is length, NF is number of fingers (connected parallel devices) and N is number of separate parallel devices.
Figure 3.38: Complete FWR circuit. Rectifier control circuitry (red), voltage divider (green) start-up circuitry (brown), shorting control circuitry (orange) rectifier bridge (blue) and reference circuit (purple).
3.12.2. Layout

The layout of the circuit presented in Figure 3.39 has been designed with electromigration, substrate noise and latch-up in mind. The number of bond pads and metallisation area were designed to reduce the risk of electromigration, a process by which a conductor degrades due to high current densities [85], and minimise track resistance. Christmas tree routing was used for the large transistors [107]. As seen from Figure 3.40, current runs along the tree it goes down into the transistors decreasing the current and maintaining the current density. Maintaining constant current density decreases the chance of electromigration and reduces the overall track resistance. Metal slotting has been used as recommended by the foundry to provide optimum reliability for high current densities, thermal expansion and mechanical stress.

Large currents running through the pass transistors result in substrate noise posing a problem for the sensitive analogue comparators [108]. To reduce substrate leakage, the transistor bases have been well connected to the rails with many substrate ties. In addition, large guard rings 3μm surround each transistor to pick up any stray minority carriers. These precautions also reduce the chances of latch-up. Additionally, all PMOS and NMOS transistors are separated by at least the minimum distance recommended in the XFAB XH018 documentation.

The pass transistors were laid out as multiple devices with many fingers to give a compact shape. The NMA pass transistors used four devices made up of five hundred fingers each forty micro meters in width and two micro meters in length giving the total gate with of one hundred millimetres. The PMA pass transistors used the same width, length and number of fingers but only four devices for a total width of eighty millimetres.
Figure 3.39: Layout of the full wave rectifier including NMA transistors (white boxes), PMA transistors (brown boxes), control circuitry (red box) and surrounding bond pads. Top metal layer is not shown.
3.12.3. Simulation

Simulations of the ADSR efficiency and power loss during shorting control will be used to characterise the ADSR design.

Efficiency

The test circuit for rectifier efficiency is shown in Figure 3.41. The test case coil parameters were used to model the pickup. PCE (power conversion efficiency) was measured using transient simulation using the Mentor Graphics simulator Eldo. The output load was modelled as a voltage source forcing the effective DC load to be matched to the input power with a DC load voltage of $3.3V$. This is accurate assuming a large filter capacitance is used to ensure the ripple voltage is small. The input power is calculated across ten periods as,

$$ PCE = \frac{P_{out}}{P_{in}} = \frac{1}{kN} \int_{n_0+kN}^{n_o+kn} \frac{V_R^2[n]}{R_L} / \frac{1}{kN} \int_{n_0}^{n_o+kn} V_{in}[n], I_{in}[n] $$  \hspace{1cm} (3-49)

where $N$ is the number of samples per period of the input voltage and $k$ is the number of cycles integrated over. $P_{in}$ is the average rectifier input power and is equal to $P_{V_1} - P_{R2}$. This gives the efficiency of the rectifier disregarding the losses in the pickup. The input voltage amplitude from $V_1$ was incremented from 0.45V to 4V. The simulated PCE is plotted against the output power in Figure 3.42 with the analytical PCE from Section 3.6. From approximately $30mW$ to $600mW$ the simulated PCE remains above 90% with a 92.5% peak PCE occurring at $150mW$.

The simulated PCE is lower than the analytically calculated PCE, partially due to the lack of control circuit power losses in the analytical estimate. The total simulated control losses at
600kHz amount to 2.42mW, of which 1.44mW is lost in the inverters driving the pass transistors. The analytical PCE is also re-plotted including the simulated control circuitry losses. Including the control losses significantly improves the accuracy of the analytical solution at low output powers. The remaining discrepancy between the analytical and simulated results could result from the comparator hysteresis and reverse currents due to switching delays, both of which are not accounted for in the analytical solution. Also, the analytical solution assumes the rectifier input is a sinusoidal voltage source. The parallel-tuned pickup however is not an ideal voltage source.

![Figure 3.41: FWR efficiency test setup.](image)

**Figure 3.41:** FWR efficiency test setup.

**Figure 3.42:** Simulated and analytical PCE of the ADSR with output power. Analytical PCE is re-plotted with the simulated control losses included (Simulated without parasitics).
**Efficiency with Turn On Soft Start**

The turn on rise time of the NMOS bridge transistors was set to 11nS. This was designed to limit the peak current under maximum load conditions below 1A. The efficiency was measured with different rise times that were varied by changing the width of transistor $M_2$ from Figure 3.37. A plot of the rectifier efficiency and peak current against rise time is shown in Figure 3.43 with a 500mW output power and 600KHz input frequency. Rise times above 11nS gave a negligible increase in PCE but resulted in a larger peak current. The peak current with an 11nS rise time is 1.075A slightly above the desired maximum current limit. However, it is expected PCB and wire bond inductance will lower the peak current slightly.

![Plot of Efficiency and Peak Current Against Rise Time](image)

**Figure 3.43: Efficiency and peak current against rise time.**

**Power Dissipation During Shorting**

A large power dissipation during shorting control will result in excessive heating of the IC and implant as a whole. The circuit in Figure 3.41 was used to measure the shorting control transistor losses and winding losses. $V_2$ was set to 3.6V forcing shorting control to be active. The open-circuit voltage was increased from 0.350V to 3.736V. Winding losses and the combined power dissipation in the NMOS transistors were measured. The results are
presented in Figure 3.44 and Figure 3.45 respectively. At the maximum specified open-circuit voltage of 3.736V from Section 3.6, the shorting transistor power dissipation is approximately 26.5mW as expected. The winding losses are slightly above 66mW giving a combined power dissipation of 94mW.

Figure 3.44: Simulated shorting control transistor losses with $V_{OC}$ from 0.35V to 3.736V.

Figure 3.45: Simulated shorting control winding losses with $V_{OC}$ from 0.35V to 3.736V for a 500m$\Omega$ winding resistance.
3.13. Summary

Chapter 3 began with an introduction to integrated circuit (IC) fabrication and the integrated circuit MOSFET. The important concepts of the small-signal model, current mirror, differential amplifier, process variation and guard rings were introduced. An overview of the IC design process was given to providing an understanding of the design steps involved.

Key ADSR requirements were developed including a 0-500mW output power range, self-start-up ability, maximum input voltage capability of 6V and a maximum load voltage of 3.6V maintained with shorting control.

The analysis, design, layout and expected performance for each ADSR sub-circuit was covered. To maintain the device heating below 2°C with the maximum expected field strength, an NMA transistor width of 100mm (4 devices with 500 fingers and 40μm width) was used. The total power loss including winding losses was expected to be below 100mW. An ADSR efficiency above 90% was estimated with output powers between 5mW and 500mW.

The expected propagation delay though the bridge-driver was approximately 30nS which is equivalent to 1.8% of the IPT period at 600KHz. A voltage and current reference circuit was designed and the voltage reference standard deviation from process variation was simulated to be only 1.66% of the mean value. A design method was developed to create a complete ADSR and power flow controller. Circuit layout was performed considering practical limitations such as process variation and electromigration. Design and simulation results were presented with the ADSR maintaining an efficiency above 90% between 50mW and 500mW. It was concluded that differences between the analytically estimated and simulated efficiency were predominantly due to control losses. A soft turn on technique was shown to be capable of maintaining current spikes though the rectifier close to 1A.
Novel design approaches in this chapter include:

1. Using the ADSR pass transistors for shorting control as a power management strategy.
2. Analysis of the shorting transistor and pickup winding losses during shorting control.
3. Analysis of the passive diode rectifier’s capability to provide the required start-up voltage.
4. Sizing the two comparator latches differently to introduce hysteresis.
5. Utilising HV NMOS transistors connected to the load voltage as an over voltage protection mechanism to protect the comparator inputs.
6. Design of a new voltage reference (also used as a current reference).
7. Implementation of a soft turn on mechanism for the pass transistors.

In Chapter 4 the physical ADSR fabricated using XFABs XH018 process is evaluated.
Chapter 4  Measuring the Integrated Circuit Rectifier and Power Link Performance

Upon completion of the DRC and LVS, the ADSR design files were sent to XFAB for fabrication. Thirty dice were manufactured and shipped back for testing. Chapter 4 outlines the process of validating the simulations. This included designing test circuits to measure the ADSR efficiency and the effect of shorting control on secondary efficiency along with the process of attaching the dice to the external test circuits.

The fabricated ADSR is shown in Figure 4.1. The five large bond pads to the left of the photo are connected to $V_{RL}$, one small bond pad for ESD protection and three small bond pads are connected to an additional reference circuit included for testing. The large bond pads to the right are connected to ground with two small bond pads for the switching signals and one small bond pad for ESD protection. The upper and lower bond pads are for $V_{IN-}$ and $V_{IN+}$ respectively (refer to Figure 4.3 for circuit diagram). The bridge transistor locations can be seen from the Christmas tree routing. Each transistor has five bond pads to provide adequate metal area.

![Figure 4.1: Photo of an ADSR die (1.29mm by 2.12mm). Christmas tree structures and metal slotting are visible on the top metal layer. Small metal squares are part of the fill pattern inserted by the foundry to ensure reliable manufacturing.](image-url)
4.1. Wire Bonding

Wire bonding is the process of linking an integrated circuit with the outside world. An ultrasonic wire bonding machine uses ultrasonic vibrations to fuse a wire to a bond pad on the die [109]. The wire end is melted into a small ball and placed on the surface of the die. Using pressure and ultrasonic vibrations, the wire is bonded with the metal pad [109]. The wire is then fed from a spool as it is moved to an external location on a chip carrier or PCB where a second bond is used to connect the wire and tear it from the spool. Bond pads on the die, typically 75µm by 75µm, for 25µm wire, provide areas to attach the wires. The bond pads have an exposed metal surface with no passivation layer. Due to the mechanical stresses subjected to the bond pads during bonding, the silicon underneath is typically not used for circuitry by designers [85], [110]. It can be used for electro-static-discharge (ESD) protection with specialised circuitry normally designed by the foundry. For small circuits, the bond pads can require a large proportion of the overall die.

The TPT HB10 wire bonder⁹ at the University of Auckland was used to ball bond 25µm and 17µm gold wires from the die to a PCB. The bonder has four settings, the last three of which are set for the first and second bond separately:

1. Stand temperature: Sets the temperature of the stand on which the die to be bonded is placed. A temperature of 120°C was used.
2. Ultrasonic energy: Controls the amplitude of the ultrasonic vibrations. An ultrasonic setting of 250 was used for the first bond (on IC) and 500 for the second (on PCB).
3. Time: Sets the bond time for ultrasonic energy and force to be applied. 200mS was used for both bonds.
4. Force: Sets the force with which the wire is pressed against the die surface. A force setting of 300 was used for bond one and 1000 for bond two.

25µm wire was used for all of the necessary inputs and outputs from the rectifier for its lower resistance and larger current carrying capacity. 17µm wire was only used for test outputs such as the voltage regulator output and comparator outputs. Bonding with the 17µm wire was significantly more difficult compared to the 25µm as the wire was more prone to snap, the bond pads were smaller and the bond tool tip was prone to blockage.

⁹ http://www.tpt-wirebonder.com
Chapter 4  
Measuring the Integrated Circuit Rectifier and Power Link Performance

Five dice labelled $A_1$ through to $A_5$ were bonded-out to the test PCBs as in Figure 4.2 to measure the sub-circuit components (comparator, start-up circuit, voltage reference, etc.) and three dice were bonded-out to test the ADSR and shorting control. The bonded dice were glued to the PCB with heat curing DELOMONOPOX MK096 epoxy from Delo\textsuperscript{10} before bonding and after bonding were coated in Polytec\textsuperscript{11} UV2144 UV curing epoxy to protect the bond wires. During testing, the DC voltages and currents applied for sub-circuit measurements caused four dice to fail. However, none of the three dice failed when operating as rectifiers.

![Figure 4.2: ADSR die attached to a PCB with gold wire bonds before epoxy is used.](image)

4.2. Sub-Circuit Measurements

As only the reference circuit, NMA gates, $V_{R_L}$, ground and pickup inputs were bonded-out, not all of the sub-circuits could be measured directly. However, most of the important performance criteria could be inferred using the available bond pads. The NMA and PMA

\textsuperscript{10} https://www.delo-adhesives.com

\textsuperscript{11} http://www.polytec-pt.com
transistor body diodes, bridge-driver characteristics, voltage reference and start-up circuit were all measured. A block diagram of the ADSR is presented in Figure 3.11 below for reference.

![Block diagram of the ADSR](image)

**Figure 4.3: Schematic of synchronous rectifier. Circled components are not included in the integrated circuit.**

### 4.2.1. Body Diodes

The NMA and PMA body currents were measured from one die as process variation was not expected to significantly affect the forward voltage or diode resistance.

For the NMA devices, $V_{IN+}$ and $V_{IN-}$ were held at 0V ensuring the PMA transistors $M_{P1}$ and $M_{P2}$ were in cutoff. The NMA gates were attached to GND putting them into cutoff. $V_{RL}$ and GND were shorted to ensure the ESD protection circuitry did not trigger. $V_{RL}$ and GND were then increased until the NMA body diodes started to conduct and further increased until the current reached approximately 180mA in each transistor.

The PMA body diodes were tested in a similar way. $V_{RL}$ and GND were held a 0V while $V_{IN+}$ and $V_{IN-}$ were increased until the PMA body diodes conducted 180mA each. The NMA transistor gates were attached to $V_{IN+}$ and $V_{IN-}$ to put them into cutoff.

The results are presented in Figure 4.4. Simulations predicted forward voltage drops between 1.1V and 1.2V for both NMA and PMA devices. The simulated diode resistances were 7.84Ωµm and 9.53Ωµm for NMA and PMA devices respectively. It is clear that the simulations were inaccurate when predicting the body to drain current. The experimental
forward voltage was half the simulated value at approximately 0.5\(V\) for NMA devices and 0.65\(V\) for PMA devices. However, the diode resistance was three orders of magnitude greater, approximately 64\(m\Omega\) (6.4\(K\Omega\mu m\)) for the NMA devices and 27\(m\Omega\) (2.2\(K\Omega\mu m\)) for the PMA devices. During start-up, the total forward voltage drop and resistance of the rectifier is approximately 1.15\(V\) and 90\(m\Omega\) respectively. Ignoring diode resistance, the start-up rectifier efficiency is plotted as a function of output voltage using the formula, \(\eta = \frac{V_{RL}}{V_{RL} + V_{FW}}\) in Figure 4.5.

![Measured Bridge Transistor Body Current](image)

**Figure 4.4:** Measured \(I_B, V_{DS}\) curve for NMA and PMA transistors.

![Start-up Rectifier Efficiency vs. Load Voltage](image)

**Figure 4.5:** Analytical start-up rectifier efficiency as a function of load voltage with measured 1.15\(V\) diode forward voltage.
From (3-21) in Chapter 3, the ratio of start-up input power to active input power with $V_{START} = 2.7V$, $V_{FW} = 1.15V$, and $V_{ACTIVE} = 3.3V$ is,

$$\frac{P_{in(\text{START})}}{P_{in(\text{ACTIVE})}} = \frac{10.395}{(1/\eta_{\text{ACTIVE}})10.89}$$ (4-1)

Even with a 100% efficient active rectifier, the input power required for start-up is lower than the full output voltage load power. Thus, the start-up rectifier is capable of allowing the ADSR to reach the start-up voltage without a larger initial open-circuit voltage or a stronger magnetic field. The power dissipation during start-up will be larger than during active rectification but will only operate briefly before the active rectifier kicks in.

### 4.2.2. Bridge-Driver Measurements

Three bonded-out dice were used to measure the threshold voltages for the complete rectifier bridge-drivers. The drives are integrated amid other circuitry within the rectifier complicating measurements. Their inputs were accessible from the pickup inputs, and the outputs from the rectifier bridge transistor gates. The following method was used for the bias measurements:

1. Make $V_{DD} = V_{in+} = 3.3V$ and $V_{in+} = 0V$.
2. Decrease $V_{in+}$ until switching occurs on $V_{G(M_{N1})}$ and measure voltage for $V_{th-}$.
3. Increase $V_{in+}$ until switching occurs again and measure voltage for $V_{th+}$.

The results are presented in Table 4.1.

<table>
<thead>
<tr>
<th>Die</th>
<th>High (mV)</th>
<th>Low (mV)</th>
<th>Hysteresis (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sim</td>
<td>-6.3</td>
<td>-152.6</td>
<td>147</td>
</tr>
<tr>
<td>A1</td>
<td>-7.8</td>
<td>-168.8</td>
<td>161</td>
</tr>
<tr>
<td>A3</td>
<td>-9.1</td>
<td>-164.2</td>
<td>155.1</td>
</tr>
<tr>
<td>A4</td>
<td>-20.2</td>
<td>-157.4</td>
<td>137.2</td>
</tr>
</tbody>
</table>

Upon activation of the NMA switches, the input voltage is connected to ground across the low resistance of the bridge transistor. This made measuring the bridge-driver delay using a 50Ω function generator difficult. When the function generator input fell below the negative threshold voltage, the NMA FET shorted the input. Because the voltage drop across the 50Ω output resistance of the function generator was much larger than the NMA resistance, the input voltage to the comparator returned to 0V, and the comparator turned the NMA transistor off. This lead to oscillations during the negative section of a square wave input.
Despite this, the LL (low-low) delay could be measured from the function generator input and NMA gate voltage. $V_{DD}$ and $V_{IN-}$ were held at 3.3V and ground at 0V. A 1MHz square wave with $1V_{pk}$ was input to $V_{IN+}$. The delay between $V_{IN+}$ going low and the NMA gate voltage $V_{GN1}$ beginning to go high was measured. This gave the approximate LL delay from the input to output of the bridge-driver. The results are presented in Table 4.2. HH (high-high) delay could not be measured as a result of the oscillations. The simulations give no reason to believe the HH delay should be significantly different from the LL delay.

Due to the test setup constraints, the test conditions are not identical to the simulated test setup. However, they provide validation that the delay is within the range predicted by simulation. As the comparator’s first stage propagation delay is dependent on the amplitude of the input voltage, the measured delay was slightly lower than the simulated results due to the larger amplitude of the input waveform.

<table>
<thead>
<tr>
<th>Die</th>
<th>LL delay (nS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sim</td>
<td>32</td>
</tr>
<tr>
<td>A2</td>
<td>24</td>
</tr>
</tbody>
</table>

### 4.2.3. Voltage Reference

An additional voltage reference was included within each die allowing test measurements to be performed. A separate supply, $V_{DD2}$, was used for the test voltage reference. This pin was bonded-out in addition to a start-up pin, $V_{st}$, and the voltage reference output pin, $V_{bias}$. A Keithley\(^{12}\) 2002 8 ½ digit multimeter with an accuracy of 14.6μV for the measurement range and reading value was used to measure the bias voltages from all five dice that had been bonded-out for sub-circuit measurements. The Keithly input resistance for the measurement voltage range was greater than 100GΩ, large enough to prevent loading effects on the voltage bias. The devices were measured at room temperature ($\approx 26^\circ C$) and the results are presented in Table 4.3. All of the measured dice were within the predicted standard deviation. Furthermore, none had a bias voltage large enough to result in over-voltage of the circuit from an increase in shorting control threshold voltage.

\(^{12}\)http://www.tek.com/keithley
### Table 4.3: Voltage bias measurements from five dice. Simulated min and max are ± 2σ

<table>
<thead>
<tr>
<th>V\text{bias}</th>
<th>Measured</th>
<th>Sim</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\text{DD2}</td>
<td>2.5V</td>
<td>3.5V</td>
</tr>
<tr>
<td>Mean</td>
<td>1.099</td>
<td>1.100</td>
</tr>
<tr>
<td>Min</td>
<td>1.092</td>
<td>1.094</td>
</tr>
<tr>
<td>Max</td>
<td>1.106</td>
<td>1.107</td>
</tr>
<tr>
<td>V\text{DD2}</td>
<td>2.5V</td>
<td>3.5V</td>
</tr>
<tr>
<td>Mean</td>
<td>1.100</td>
<td>1.102</td>
</tr>
<tr>
<td>Min</td>
<td>1.064</td>
<td>1.065</td>
</tr>
<tr>
<td>Max</td>
<td>1.136</td>
<td>1.139</td>
</tr>
</tbody>
</table>

#### 4.2.4. Start-up Circuit Measurement Results

$V_{R_L}$ and $V_{in-}$ were ramped from 0V to 3.3V with a triangle wave having a slew rate greater than 6.2 V/s. $V_{in+}$ was held below −0.4V. The comparator output and input triangle wave were measured with an oscilloscope. The ramp voltage was measured when the comparator output went high as this indicated the start-up circuit had triggered. The measurement was carried out on two dice. Both were found to have start-up voltages of approximately 2.7V, close to the 2.73V simulated value. The test setup using the oscilloscope did not allow a measurement accuracy greater than 100mV.

#### 4.3. Measuring the Power Conversion Efficiency

The key performance criterion for the rectifier is power conversion efficiency (PCE). Accurate power measurements from high frequency switched power supplies are challenging. The test setup used to characterise the rectifier performance was a significant design challenge and is described in the subsequent section followed by the measurement results. This section describes the methods used to remove error sources from the measurements and to compensate for magnetic field noise that could not be designed out of the test setup.

#### 4.3.1. PCE Test Circuit

A number of methods have been used to measure the PCE of active or synchronous rectifiers in the literature. One of the most common is to insert a resistor, often between 1-10Ω, in series with the rectifier input [70][73] as in Figure 4.6. The voltage $V_S$ across the sense-resistor is measured with an oscilloscope, and $I_{in} = V_S/R_{sense}$ is multiplied with $V_{in}$ to get the input power. The output power is derived from the output voltage and load resistor. PCE is calculated based on the average input and output powers as,
\[
P_{\text{CE}} = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{1}{kN} \int_{n_0}^{n_0+kN} V_{\text{OUT}}^2[n]/R_L \quad (4-2)
\]

where \(N\) is the number of samples per period of the input voltage, and \(k\) is the number of cycles that are integrated over. A Tektronix\textsuperscript{13} TDS 2014C oscilloscope with a 2500 data point record length was used to measure the waveforms. Using a sampling period of 1\(\text{ns}\) allowed one period to be recorded. To increase the measurement accuracy, the average function on the oscilloscope was used to average 64 waveforms.

The magnetic field was generated from a primary designed by Ho Yan Leung that uses a technique called energy injection control [80], [111] to maintain constant primary current and hence field strength despite changes in coupling. The primary coil inner diameter was approximately 60mm and the outer diameter 72mm. Compared with the test case coil effective diameter, the primary coil is large and only a small percentage of the primary field intersects the secondary helping to ensure a loosely-coupled link. This results in the equivalent impedance seen by the primary due to the coupled secondary being small. Hence changes in the secondary’s load have little effect on the primary.

![Figure 4.6: Measurement setup for PCE and peak current measurements. The sense-resistor and trace have a small parasitic inductance.](http://www.tek.com)

\textsuperscript{13} http://www.tek.com
**Test circuit PCB and experimental setup**

The test circuit and test setup using the test case coil are shown in Figure 4.7. The PCB was designed to minimise parasitic inductances that could degrade the ADSR performance. Most importantly, the trace lengths between $V_{DD}$, $C_f$ and ground were made as small as possible with multiple vias. Inductance between $V_{DD}$ and $C_f$ or $C_f$ and ground creates voltage spikes as the current pulses though the rectifier. If too large, the spikes will trigger shorting control incorrectly. A total parasitic capacitance less than approximately $6nH$ between $V_{DD}$ and ground was found though simulation to prevent false shorting control triggering. A battery was used for the DC supply allowing the amplifier to have a floating DC voltage and prevent interference with the floating pickup voltage.

![Test circuit PCB and experimental setup](image)

*Figure 4.7: Test PCB with ferrite core test case coil. Parasitic inductance was minimised by keeping key traces as short as possible (top). A large coil was used in the constant current primary to keep the loosely-coupled approximation true (bottom).*
**Sense-resistor error**

The sense-resistor is in the path of the input current and hence impacts the active rectifier’s operation. Figure 4.8 shows the simulated effect on the PCE of increasing the sense-resistor resistance. If incorrectly chosen, the resistor will increase the apparent PCE by a few per cent and decrease the output power. Although the apparent PCE increases, the overall secondary efficiency will decrease as additional total power is lost. As can be seen in Figure 4.8, for this ADSR and pickup a 50mΩ sense-resistor has a negligible effect on the measurement.

![Figure 4.8](image)

**Figure 4.8:** (Top) Increase in apparent efficiency due to the influence of Rsense at two different output powers. (Bottom) Decrease in output power with approximately 5.6mW output power (Left) and 55mW output power (Right).
**Amplifier bandwidth requirements**

To provide an accurately measurable voltage for the oscilloscope, the voltage across the sense-resistor was amplified using a LT6268 amplifier from Linear Technology\(^\text{14}\) with 500MHz gain bandwidth product (GBP). The power spectral density of the simulated voltage across the sense-resistor (without parasitic inductance) was calculated at a 600\(\text{kHz}\) wireless power frequency and is presented in Figure 4.9. 99% of the signal power was contained within a 50\(\text{MHz}\) bandwidth. The amplifier gain was set to 18\(\text{dB}\) giving an expected \(-3\text{dB}\) frequency of 90\(\text{MHz}\). LTspice\(^\text{15}\) was used to simulate the LT6268 model with a 50\(\text{pF}\) output capacitance to account for the probe and trace capacitances. The \(-3\text{dB}\) frequency dropped to approximately 70\(\text{MHz}\), still large enough to amplify the sense-voltage accurately.

![Power spectral density of sense-voltage waveform during ADSR operation.](image)

**Amplifier delay compensation**

The amplifier introduces a delay in the current measurement. From simulation using the LT6268 model in LTspice, the phase is approximately linear below 70\(\text{MHz}\) giving an “ideal delay” [112]. This results in a constant 3.4\(\text{nS}\) time delay in the amplified sense-voltage. As the input power is calculated from two time varying waveforms, the delay introduces an error into the calculated power. To quantify the error introduced by this delay, the following derivation is made using the Fourier series where \(E[x]\) is the expected value,

\(^{14}\) http://www.linear.com
\(^{15}\) http://www.linear.com
Chapter 4  Measuring the Integrated Circuit Rectifier and Power Link Performance

\[ P_{in(meas)} = E \left[ \sum_{n=1}^{\infty} V_{in_n} \sin(n\omega_0 t) \sum_{m=1}^{\infty} I_{in_m} \sin(m\omega_0 t + \theta_m) \right] \]  \hspace{1cm} (4-3)

\[ = E \left[ \sum_{n=1}^{\infty} \sum_{m=1}^{\infty} \frac{V_{in_n} I_{in_n}}{2} \cos((n\omega_0 - m\omega_0) t - \theta_m) - \cos((n\omega_0 + m\omega_0) t + \theta_m) \right] \]  \hspace{1cm} (4-4)

where \( \theta_m \) is the phase at \( \omega_0 m \tau \), \( \omega_0 = 2\pi/T \) and \( T \) is the period the Fourier series is the period of voltage and current signals [113]. For all components where \( n \neq m \) the expected value is zero giving,

\[ P_{in(meas)} = \sum_{n=1}^{\infty} \frac{V_{in_n} I_{in_n}}{2} \cos(\theta_n). \]  \hspace{1cm} (4-5)

With no delay the actual power is,

\[ P_{in} = \sum_{n=1}^{\infty} \frac{V_{in_n} I_{in_n}}{2}. \]  \hspace{1cm} (4-6)

The error introduced by the delay can be found as a function of frequency using (4-5) and (4-6),

\[ \varepsilon(f) = 1 - \cos(\theta_f) \]  \hspace{1cm} (4-7)

where \( f = n\omega_0/2\pi \). Error is plotted against frequency in Figure 4.10 for the 3.4\( nS \) delay. To reduce the error introduced by the comparator delay, the voltage measurements can be delayed by three samples in software giving a 3\( nS \) delay. This reduces the delay between voltage and current measurements to 0.4\( nS \) and reducing the error at 50\( MHz \) to less than 1\%.

![Error from Measurement Delay as a Function of Frequency](image)

Figure 4.10: Measurement error in the input power frequency components due to a 3.4\( nS \) delay introduced by the amplifier.
Parasitic inductance compensation

Parasitic inductance from the trace and sense-resistor was large enough to distort the voltage measurements. The measured voltage can be defined in the s domain as,

\[ V_s = I_{\text{in}}(R_S + sL_S) \]  \hspace{1cm} (4-8)

where \( R_S \) and \( L_S \) are the combined sense and trace resistance respectively. The inductance was measured with an LCR meter between the coil attachment to the PCB and the amplifier input as shown in Figure 4.7 and was found to be 2.5\( nH \). Within the spectral range from 1\( MHz \) to 10\( MHz \) the inductor impedance is 16m\( \Omega \) – 160m\( \Omega \) which is larger than the sense-resistor. The effect of \( L_{\text{sense}} \) can be removed in software by convolving the measured sense-voltage \( V_{\text{sense}} \) with the inductor and resistor impulse response such that,

\[ I_{\text{in}}[n] = V_s[n] \ast \frac{1}{L_s} e^{-\frac{R_{\text{sense}}}{L_s} n} \]  \hspace{1cm} (4-9)

where \( n \) is the \( n^{th} \) sample.

Primary field probe coupling

The final source of measurement error was signal coupling induced in the probes from the primary’s magnetic field. The sense-voltage was the smallest signal and hence coupling onto it introduced the largest error in the power measurement. The coupled signal from the primary was a sinusoid at the same frequency as the input voltage. When multiplied with the input voltage, an input power offset was introduced. Fortunately, the coupled signal amplitude remained constant providing the physical position of the probes and probe wires did not change. To compensate for the coupled voltage, the amplifier was turned off such that only the coupled voltage was on the probe. This voltage was multiplied with the input voltage measurement on the oscilloscope, and the average power offset was calculated and recorded. The amplifier was then switched back on, and the data was recorded. After the input power was calculated in Matlab for the measured data, the recorded offset power was subtracted.
4.3.2. **Quantification of Measurement Error**

Sources of error in the experimental setup will be identified and used to provide an estimated worst case measurement error.

1. **Sense-resistor error:**
   a. The 50mΩ sense-resistor has a 1% worst case error when purchased.
   b. As this resistor has a small value, it will have a very small power dissipation and heating effects are ignored.

2. **Operational amplifier gain error:**
   a. The op-amp uses a non-inverting configuration giving it a gain of \((1 + \frac{R_1}{R_2})\). \(R_1 = 750\) and \(R_2 = 107\) are both 1% accurate resistors giving a worst case gain error of +1.77% and −1.73%.
   b. The op-amp offset worst case error is ±700μV.
   c. The amplifier delay error after correction is negligible relative to other error sources.
   d. Input offset current is extremely low ±20μA for the LTC6268 and is ignored.

3. **Oscilloscope:**
   a. The Oscilloscope has a DC vertical gain accuracy of ±3% and an offset of ±2.5mV for the current readings and ±225mV for the voltage readings due to the vertical range.
   b. Quantisation error with 8 bits is less than 1% of the reading and is ignored.
   c. Skew between measured signals should be minimal as identical probes were used for all measurements.

4. **Parasitic inductance measurement and compensation error:**
   a. The measured inductance included the sense-resistor inductance and section of trace between the op-amp inputs where the switching current flows as shown in Figure 4.7. The inductance was measured with a Keysight\(^{16}\) 4285A precision LCR meter. For the measurement 2.5nH inductance at a test frequency of 30MHz, the inductance accuracy is expected to be ±10%. The deconvolution algorithm was run with the minimum and maximum sense inductance and the PCE was calculated with both results. With the worst case

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\(^{16}\) http://www.keysight.com
inductance measurement error, the PCE was between ±0.6% of the PCE calculated with the nominal measured sense inductance.

5. Primary field coupling error:
   a. The input power offset created by the primary field coupling into the current measurement probe is calibrated for and is assumed to be negligible.

6. Load resistance measurement accuracy:
   a. ±1% accurate load resistors were used.
   b. Measurements were taken directly after the primary field was turned on and rectifier became active to minimise temperature dependent resistance changes.

Using the following error sources, the total PCE error will be derived. The sense-resistor error is defined by \( \epsilon_{Rs} \), the amplifier gain error is \( \epsilon_{Av} \), the oscilloscope gain error is \( \epsilon_S \), the amplifier delay error is \( \epsilon_{Ad} \) and the deconvolution error from the sense inductance error is \( \epsilon_d \).

The offset errors \( \epsilon_s \) and \( \epsilon_{Av} \) are the oscilloscope offset and amplifier offset respectively. Errors with the notation \( \epsilon \) represent percentage errors and \( \epsilon \) represents offsets errors in volts.

The worst case measured input voltage is,

\[
\hat{V}_{IN} = V_{IN}(1 + \epsilon_S) + \epsilon_S.
\]

The worst case measured input current is,

\[
\hat{I}_{IN} = I_{IN}(1 + \epsilon_S + \epsilon_{Av} + \epsilon_{Rs}) + \epsilon_S + \epsilon_{Av}.
\]

The worst case output voltage is,

\[
\hat{V}_{OUT} = V_{VDD}(1 + \epsilon_S) - V_{GND}(1 + \epsilon_S) + 2\epsilon_S.
\]

Including the errors into (4-2) gives,

\[
PCE = \frac{E[(V_{DD}(1 \pm \epsilon_S) - V_{GND}(1 \pm \epsilon_S) \pm 2\epsilon_S)/(R_L(1 \pm \epsilon_{RL}))]}{E[(V_{IN}(1 \pm \epsilon_S) \pm \epsilon_S)(I_{IN}(1 \pm \epsilon_S \pm \epsilon_{Av} \pm \epsilon_{Rs}) \pm \epsilon_S \pm \epsilon_{Av})]}.
\]

\[
PCE = \frac{E[(V_{OUT}(1 \pm 2\epsilon_S) \pm 2\epsilon_S)/(R_L(1 \pm \epsilon_{RL}))]}{E[(V_{IN}(1 \pm \epsilon_S) \pm \epsilon_S)(I_{IN}(1 \pm \epsilon_S \pm \epsilon_{Av} \pm \epsilon_{Rs}) \pm \epsilon_S \pm \epsilon_{Av})]}.
\]

where \( E[x] \) is the expected value of \( x \). The measured signals \( V_{IN} \) and \( I_{IN} \) are zero mean. Therefore, the offsets in the denominator of (4-13) have no effect when multiplied with the measured signals. Assuming the second order terms are much smaller than the first order terms the PCE error can be approximated to,

\[
\Delta PCE = 4\epsilon_S + \frac{4\epsilon_S}{V_{OUT}} + \epsilon_{Rs} + \epsilon_{Av} + \epsilon_{RL} + \epsilon_d.
\]
With $V_{OUT} \approx 3.45V$ and with offset error removed by calibration, the worst case PCE error is $\pm 16.4\%$. The error predominantly arises due to the oscilloscope DC vertical gain error. As no statistical data is provided for the likelihood of the gain error only worst case values can be given.

To compensate for the oscilloscope gain error, the gain error on all probes were measured and found to be equal at +1.8%. This results in the gain error in the numerator cancelling with the gain error in the denominator and gives a measurement accuracy of $\pm 4.4\%$.

### 4.3.3. Experimental Results

The results were measured with an oscilloscope and all corrections were performed in Matlab. All of the measurements were taken with a $600KHz$ wireless power transfer frequency. The simulated and measured results are plotted against the output power in Figure 4.11. A PCE above 90% is maintained over a $40mW$ to $600mW$ output power range for the simulated rectifier. Including the inductance from the sense-resistor and trace results in a 0% decrease in simulated PCE. However, there is a 5% decrease in simulated PCE when PCE is calculated using the sense-voltage across the parasitic inductance. After convolving the sense-voltage with the sense-resistor and inductor impulse response in Matlab, the PCE closely matches the simulated PCE without $L_S$. Thus, convolving successfully removes the distortion from the parasitic inductance.

The experimental measurements were taken with different loads, and the field strength from the primary was adjusted to maintain an output voltage of 3.3V. The measured data and convolution corrected data follow the simulated results. An efficiency greater than 85% is maintained from approximately $30mW$ to $600mW$. The peak measured efficiency of 93% occurs with a $120mW$ output power. Due to parasitic inductance and resistance from the PCB and bond wires, the peak currents are between $100mA$ and $200mA$ lower than the simulated values.

The probe measurement locations are shown in Figure 4.12 as a reference for the following figures. The sinusoidal voltage coupled into the sense-voltage (voltage drop across the sense-resistor) probe is visible in the oscilloscope window in Figure 4.13. As it is approximately
180° out of phase with the input voltage, the power offset is negative. Ringing due to the sense-resistor and trace inductance is also visible on the sense-voltage.

It was difficult to obtain accurate measurements below 50mW due to the small size of the voltage across the sense-resistor compared with the coupled voltage from the primary. The power offset was approximately $-18\,\text{mV}$, on the same order of magnitude as the lower input power measurements. Thus, small errors in the coupled power measurements had a large effect on the calculated output power.

![Simulated and Measured PCE and Peak Current against Output Power](image)

**Figure 4.11:** Simulated and measured PCE and peak current through rectifier. The influence of the parasitic inductance has been removed with convolution correction. Simulated: simulated data without using the sense-resistor. Sim from Rs: simulated data calculated using the simulated voltage across a sense-resistor with a parasitic inductance. Ls correction: data after using the discrete time deconvolution to remove effect of parasitic inductance.
In addition, the ADSR did not function as expected when supplying low powers. The rectifier was only activated once per input cycle as seen in Figure 4.14. This was a result of the pickup tank requiring a full period of the induced voltage to charge $V_{in}$ above $V_{RL}$. The one sided switching always occurred on the same NMA transistor indicating a lower comparator threshold voltage on one side due to process variation. The threshold variation explains this behaviour which was not seen in simulation. In theory, this would result in an increased efficiency as the switching losses would be halved. This provides some justification for the higher than expected efficiency at the two lowest power measurements.

![Diagam of Rectifier IC and Load](image)

**Figure 4.12**: Probe measurement points for PCE measurements.

![Oscilloscope Window](image)

**Figure 4.13**: Oscilloscope window showing voltage across the sense-resistor (yellow), differential input voltage to the ADSR (blue), floating output voltage (purple) and floating ground (green) for the 150Ω load.
4.4. Multiple Triggering

When the rectifier output voltage reaches 3.5V, a multiple triggering occurs on one side of the rectifier. The NMOS transistor is turned on as normal. Partway through the on-time, the bridge-driver switches back low temporarily before returning high.

Current spikes though the bond wires’ inductance from $V_{DD}$ and ground to the PCB create small voltage spikes. When $V_{DD}$ is close to the shorting control threshold, the voltage spikes can be large enough to trigger shorting control. This leads to the PMA transistors switching off and preventing current flow though the rectifier. The sudden switching causes the pickup voltage to oscillate and the comparator’s input voltage goes above ground causing the NMA transistor to shut off. When the PMA transistor turns off, there is also a ripple in the supply voltage large enough to switch shorting control back off. Therefore, the PMA transistors turn back on. The comparator input voltage goes below the threshold voltage again and switches back on. This normally happens only once per cycle. Though simulation it was found that 6nH was enough to cause the multiple triggering.
One option to prevent this is inclusion of a capacitor on chip before the bond wires to reduce the voltage spike magnitude. A $1\mu F$ capacitor would be required to reduce the voltage spikes enough to prevent false triggering. The die area required for this capacitor would be impractical however. An alternative strategy is to include voltage sense pins that measure the voltage across the filter capacitor and load directly. Having the shorting control voltage measurement inputs bonded-out would only require two additional bond pads. The bonded-out voltage measurement or “sense” pins shown in Figure 4.15 would remove the voltage spikes across the bond wire inductance from the load voltage measurement.

![Figure 4.15](image)

**Figure 4.15:** Rectifier with output pins for shorting control voltage measurement inputs.

The secondary efficiency was measured when operating without multiple triggering. The secondary coil was then moved slightly closer to the primary increasing the output voltage to the point where multiple triggering just began to occur. A $200\Omega$ load was used for the measurements. Without multiple triggering, the output power was $56\,mW$. Due to the slight increase in output voltage required to cause multiple triggering, the output power for the second measurement was $59\,mW$. There was no change in load however. The difference in measured secondary efficiency between the normal operation and multiple triggering was 4% with 46.2% and 42.2% respectively.
4.5. Measuring Secondary Efficiency with Shorting Control

Secondary efficiency was introduced in Chapter 2 and describes the amount of power lost in the secondary IPT pickup relative to the output power. It does not include losses in the primary coil. To test the effect of shorting control on the secondary pickup efficiency, the circuit from Figure 4.16 was used. The secondary efficiency in this setup includes the rectifier losses and is measured as,

\[
\eta_2 = \frac{P_{RL}}{P_{OC}} = \frac{V_{RL}^2/R_L}{Re\{V_{OC}I_2\}} = \frac{V_{RL}^2/R_L}{P_{R_2} + P_{rec} + V_{RL}^2/R_L} \tag{4-16}
\]

where \(P_{OC}\) is the real power from the open-circuit voltage and \(P_{rec}\) is the power lost in the rectifier. The open-circuit voltage or input power cannot be measured directly. However, if \(R_2\) is known, the pickup input current can be measured across a sense-resistor and the winding losses including the sense-resistor losses can be calculated as,

\[
P_{R_2} = I_2(R_2 + R_S). \tag{4-17}
\]

The rectifier power conversion efficiency is already known allowing the rectifier losses to be approximated as,

\[
P_{rec} = (1 - PCE)P_{RL} \tag{4-18}
\]

![Figure 4.16: Test circuit for secondary efficiency with shorting control.](image)

The test PCB was modified placing the sense-resistor in series with the coil resistance. This allowed the secondary current \(I_2\) to be measured but changed the effective \(R_0\) of the coil. Inferring the input power requires the coil resistance to be known. It is difficult to accurately measure the winding resistance in the ferrite core test case coil used previously due to the non-linear core losses which depend on the pickup voltage. To simplify the analysis, a new air core coil was used and the winding resistance could be measured with an LCR meter. The
coil parameters were measured with a Keysight\(^{17}\) 4285A precision LCR meter to be \(L_2 \approx 2\mu H\) and \(R_2 = 250m\Omega\). The inductance measurement accuracy at 600\(KHz\) with a 2\(\mu H\) inductance was \(\pm 0.23\%\). A 440\(m\Omega\) sense-resistor in series with the coil gave an effective \(R_2 = 690m\Omega\) and resulted in the pickup matching a 90\(\Omega\) load. Unlike the test setup for rectifier PCE, the sense-resistor did not affect the rectifier efficiency as it was not between the pickup capacitor and the rectifier. An amplifier was not required as the sense-resistor was large enough to accurately measure using an oscilloscope. This simplified the test setup and removing additional sources of error. The secondary capacitor \(C_2 = 35nF\) was used to tune the pickup to 600\(KHz\). A 200\(\Omega\) DC load was used with a filter capacitance of 4.7\(\mu F\). The modified test circuit with the new coil is shown in Figure 4.17.

![Figure 4.17: Test circuit for measuring the effect of shorting control on secondary pickup efficiency.](image)

The measurements were taken with an oscilloscope by moving the position of the secondary coil with respect to the primary coil to arrive at set shorting control duty cycles. The oscilloscope window was adjusted to capture a complete duty cycle period. Due to the

\(^{17}\) http://www.keysight.com
oscilloscope data limit, the 90% duty cycle could not be measured as the window length was too large and the sampling rate and record length did not allow accurate measurements. A window of the measured data with a 50% duty cycle is shown in Figure 4.18.

The experimental data was processed in Excel, and the secondary efficiency was calculated using (4-16).

The experimental results are plotted against the analytical results in Figure 4.19. To simplify comparison between the analytical curve (without rectifier losses) and experimental data, 10% efficiency has been added to the experimental data and plotted as w/o rectifier losses. As the experimental AC load is not exactly 90Ω and the rectifier losses vary slightly with output power, there are some deviations between the experimental and analytical results. However, the shape of the curve follows the analytical results for shorting control closely. At 100% duty cycle the measured secondary efficiency is 42% with 58% of power lost in the secondary pickup and rectifier. A maximum efficiency of 56% is reached with a duty cycle of 30%. Shorting control can dynamically change the effective load seen by the pickup. This change in load allows the secondary to achieve maximum power transfer when the coupling is low and up to 16% increased efficiency as the coupling increases and excess power is available.
Figure 4.19: Efficiency of the secondary and rectifier including and excluding losses during shorting control. The effective load is proportional to the rectifier duty cycle.

4.6. Shorting Control Power Loss

The air core coil was used to measure the power dissipation during shorting control with the test setup of Figure 4.16. Open-circuit voltage could not be measured directly but could be inferred from the input voltage as,

\[ V_{OC} = \sqrt{(V_{IN} + R_2 I_2)^2 + (j\omega L_2 I_2)^2}. \] (4-19)

As \( V_{IN} + R_2 I_2 \ll \omega L_2 I_2 \), the open-circuit voltage can be approximated as the inductor voltage and calculated as,

\[ V_{OC} = V_{L2} = \omega L_2 I_2. \] (4-20)

Shorting control was activated by attaching \( V_{OUT} \) to 3.6V from a power source. The secondary coil was moved within the primary to give an open-circuit voltage close to 1.878V and 3.756V, the maximum voltages defined in Chapter 3 Section 3.6. Shorting power and winding losses were calculated from,

\[ P_{SC} = \frac{V_{IN} I_2}{P_2} = (R_2 + R_s) I_2^2 \] (4-21)
where the losses in the sense-resistor $R_S$ are included in the winding losses. The impedance of $C_2$ at 600KHz is much larger than the impedance of the shorting switch allowing the current through the shorting switch to be approximated as $I_2$. As can be seen from Figure 4.20 the open circuit varies slightly with time. To account for this the power measurements were taken over 30 cycles. The average amplitude was calculated from the measured data $v[n]$ over $N$ samples as,

$$V_{oc} = \sqrt{\frac{2}{N} \sum_{n=1}^{N} v[n]^2}. \quad (4-22)$$

![Open-Circuit Voltage](image)

**Figure 4.20:** Measured open-circuit voltage calculated from the secondary current through the sense-resistor. The open-circuit voltage amplitude varies from cycle to cycle but average amplitude (Vpeak) is shown.

The measured data is presented in Table 4.4 with analytical shorting and winding losses recalculated for the air core coil as a reference. The measured winding losses are close to the analytically calculated values. Shorting transistor losses however are higher than what is expected analytically. This indicates the shorting transistor resistance is slightly larger than expected. The difference is more pronounced with a larger open-circuit voltage and is, in part, a result of the approximation that the drain source voltage is low enough to model the transistor as an on-resistance. With a 3.835V open-circuit voltage, the drain source voltage of the NMA transistors is approximately 140mV and will have a small effect on the on-
resistance approximation. Additionally, greater power dissipation with a 3.835\(V\) open-circuit voltage will cause greater heating. The NMA transistors’ on-resistance has a positive temperature coefficient and hence the resistance will increase with greater power dissipation.

Table 4.4: Measured and calculated power loss during shorting control.

<table>
<thead>
<tr>
<th>(V_{OC})</th>
<th>(P_{SC})</th>
<th>(P_2)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Analytical</td>
<td>Measured</td>
</tr>
<tr>
<td>1.935(V)</td>
<td>6.5(mW)</td>
<td>8.2(mW)</td>
</tr>
<tr>
<td>3.835(V)</td>
<td>22.3(mW)</td>
<td>32.4(mW)</td>
</tr>
</tbody>
</table>

4.7. Comparison with Previous Work

Table 4.5 benchmarks the rectifier against other recent integrated rectifier solutions for IPT and wireless power transfer. This design operates at a lower frequency than much of the other work as it provides lower switching losses. The power supply range fits in between lower power sub 100\(mW\) range and higher power over 1\(W\) range within the literature. The higher power rectifiers within the literature use series tuning and do not suffer from current spikes but also cannot produce output voltages larger than their induced voltage [78], [91]. This work benefits from the voltage boost up of parallel-tuned pickups, provides greater output power than previous designs for parallel-tuned pickups and provides comparable PCE to recent work. This design also includes shorting control as a power flow control method integrated into the secondary pickup side of the IPT link. Previous work has integrated a current shunting over voltage protection mechanism [114]. This form of over voltage protection dissipates excessive power for use as an implant. Detune control has been used in multiple designs at the cost of an additional off-chip capacitor [70], [115], [116]. A final power flow control method uses a technique referred to as Q-modulation where the pickup is shorted at the zero crossing of the induced current for a section of the IPT period has been developed [117]. This is similar to shorting control but is activated every half period of the induced IPT waveform. This results in more frequent switching and hence larger losses, but may have greater control over transforming the effective load seen by the secondary pickup. The ADSR and power flow controller in this thesis has been designed to withstand large increases in coupling while maintaining low power dissipation. This concept has not been considered in the previous literature on integrated circuits for IPT.
Table 4.5: Comparison of ADSR with previous work.

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
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</thead>
<tbody>
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<td>Technology</td>
<td>0.18 µm</td>
<td>-</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
<td>0.18 µm</td>
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<tr>
<td>Chip Area</td>
<td>0.34mm² (core)</td>
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<td>0.189mm²</td>
<td>3.06mm²</td>
<td>4.77mm²</td>
<td>2.73mm²</td>
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<td>Load Cap</td>
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<td>4.7µF-22µF</td>
<td>1.5nF</td>
<td>-</td>
<td>4.7µF</td>
<td>4.7µF</td>
</tr>
<tr>
<td>Frequency</td>
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<td>100-200KHz</td>
<td>13.56MHz</td>
<td>13.56MHz</td>
<td>6.78MHz</td>
<td>600KHz</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>1.2V</td>
<td>5V</td>
<td>1.28V-3.56V</td>
<td>3.6V</td>
<td>5V</td>
<td>3.3V</td>
</tr>
<tr>
<td>Max $P_{OUT}$</td>
<td>450mW</td>
<td>2.5W</td>
<td>24.8mW</td>
<td>102mW</td>
<td>6W</td>
<td>600mW</td>
</tr>
<tr>
<td>Max PCE</td>
<td>Simulated</td>
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<td>90.7%</td>
<td>-</td>
<td>-~95%</td>
<td>~93%</td>
</tr>
<tr>
<td></td>
<td>Measured</td>
<td>93%</td>
<td>93%</td>
<td>92.6%</td>
<td>92.2%</td>
<td>~93%</td>
</tr>
<tr>
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<td>-</td>
<td>~20-100mW</td>
<td>~1.6W</td>
<td>~30-600mW</td>
</tr>
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<td>Primary based</td>
<td>Not included</td>
<td>Primary based</td>
<td>Not included</td>
<td>Shorting control</td>
</tr>
</tbody>
</table>

4.8. Summary

Chapter 4 provides validation of the designed and simulated ADSR and power flow controller. The process of wire bonding was introduced describing how integrated circuits are connected out to PCBs or chip carriers allowing them to be used and tested.

Available die outputs were used to test the ADSR sub-circuits allowing comparison with the simulated results. The parameters for the NMA and PMA body diodes were found experimentally. In comparison to the simulated results, the body diode parameters were favourable for the passive start-up rectifier. Given the open-circuit voltage was large enough to power the load, the start-up circuit could provide the necessary start-up voltage to enable the active rectification circuitry. Experimentally measured results for the bridge-driver, voltage reference and start-up circuit were all close to the simulated values.

An experimental setup was developed for validation of the ADSR efficiency. Practical measurement challenges were identified and addressed and the worst case measurement accuracy was estimated. Experimental results lined up closely with the simulated results. Efficiency was slightly larger than expected at low output powers, partially due to measurement accuracy and partially due to “one-sided-switching” that occurred due to process variation. favourably, due to the high frequency nature of the current though the
rectifier, peak currents were $100 - 200m\text{A}$ lower than simulated as a result of bond wire and PCB parasitic inductance.

A new, air-core coil was used to allow experimental measurement of the secondary efficiency. The effect of shorting control on the secondary efficiency of a pickup matched to a load for maximum power transfer was measured. Experimental results followed the analytical results very closely. Shorting control was found to increase the secondary efficiency by a maximum of 16% as coupling increased.

A multiple triggering problem was identified and explained. Methods to correct it were presented and a practical solution using two additional bond pads to allow external output voltage measure across the filter capacitor was proposed.

Experimental measurements for the power loss during shorting control were undertaken. It was found that the power loss was slightly higher than expected, particularly at high open-circuit voltages. The observation was explained by the transistor on-resistance approximation being less accurate with larger drain-source voltages in combination with the positive transistor resistance temperature coefficient.

The chapter concluded with a comparison of the ADSR and power flow controller designed in this thesis with previous work.
Chapter 5  Powering a Pressure Monitor and Micropump

The mouse telemeter available from Millar\(^{18}\) is an example of a wireless, implantable telemeter with supercapacitors for energy storage and inductive power transfer. Though the housing is not suitable for human implantation, and pressure measurement circuitry is not used, the circuitry demonstrates the desired features for a hydrocephalous monitor. Therefore, it has been used to demonstrate the ADSR performance in a telemeter. In addition, a piezoelectric micropump has been used to demonstrate the high power capability of the ADSR.

5.1. An Example Telemeter for Hydrocephalus Monitoring

The mouse telemeter is powered wirelessly from a primary that dynamically changes the primary field strength as needed to supply the required power. Field strength is controlled through the primary current via a wireless feedback loop. The telemeter draws approximately 30\(\, \text{mW}\) when transmitting and an additional 30 – 50\(\, \text{mW}\) when charging the super capacitors. Pressure and temperature data are transmitted to a receiver and can be recorded on a PC. Some key aspects of the telemeter are outlined in the following section.

**Pickup and Regulator**

The pickup inductor uses a coil similar to the test case coil. It has the same \(L_0\) and \(R_0\) values but triple the number of turns. The voltage is stepped down using a capacitive tap as in Figure 5.1. The combined capacitance \(C_1C_2/(C_2 + C_2)\) is tuned to the wireless power resonance frequency. The voltage division ratio changes the effective load such that,

\[
R_L(\text{eq}) = \frac{R_L(C_{2A} + C_{2B})}{C_{2B}}.
\]

This provides more freedom in the physical pickup design while still allowing load matching. A full wave diode bridge rectifier is used to convert the sinusoidal voltage into a DC supply that is then regulated with an LDO regulator to provide a stable DC voltage to the circuitry.

\(^{18}\) http://millar.com/
Chapter 5  Powering a Pressure Monitor and Micropump

**Figure 5.1**: Capacitive divider for load matching.

**Shorting Control**
A comparator with two NMOS transistors is used for shorting control across the pickup coil. The combined resistance of the NMOS transistors is approximately 700mΩ. This would result in a 92.75mW power dissipation during shorting control at maximum coupling. This is 3.5 times larger than the calculated 26.5mW dissipated in the IC.

**Super Capacitor**
A supercapacitor bank is managed with an IC and provides a power buffer in times when the inductive power transfer coupling is too low to power the circuit. The total capacitance is 11.25mF giving approximately 140mJ of energy storage when charged to 5V by the supercapacitor management circuit.

**Transceiver and Microcontroller**
Data storage, transmission and processing all occur on the Nordic\(^{19}\) nRF24LE1 wireless system on chip. It includes an 8-bit CPU, embedded flash and a 2.4GHz transceiver.

**Signal Conditioning and Sensor**
The telemeter also has biopotential measurement circuitry for monitoring heart rate. It includes a differential amplifier, voltage reference and ADC, similar to what would be required for a wheatstone bridge piezoresistive pressure sensor.

\(^{19}\) http://www.nordicsemi.com
5.1.1. Adding the ADSR

The diode bridge, shorting control comparator and associated resistors and capacitors were removed from the PCB. The pickup coil and capacitive tap were replaced with the ferrite core test case coil and a single resonant capacitor. A carrier PCB shown in Figure 5.2 was used to attach the IC to the telemeter. The IC was fixed to the PCB using heat curing epoxy, and wire bonds were used to connect the IC nodes to the PCB. The IC and bond wires were then coated in UV light curing epoxy to prevent damage during handling and soldering. PCB was then soldered to the telemeter. Additionally, a supply pad and ground pad were used to connect wires for supplying power to the micropump.

![Figure 5.2: Carrier PCB (left) and carrier PCB with a bonded-out IC attached to mouse telemeter (right).](image)

The telemeter was then encapsulated in a 20 x 15 x 8mm ceramic shell sealed with UV epoxy, and the micropump supply wires exited a feed through as shown in Figure 5.3.

![Figure 5.3: TxM mouse telemeter with integrated circuit. Power leads supply the micropump controller directly from the rectifier output. Ceramic shell is approximately 20mm x 15mm x 8mm.](image)
5.2. Powering a Piezoelectric Micro Pump

The air core coil was used to obtain secondary efficiency measurements for powering the micropump as the ferrite core coil encapsulated in the ceramic housing has non-linear core losses with open-circuit voltage.

Bartel’s mp6 micropump and micropump controller [39] were powered directly from the ADSR output voltage. The specifications predict the micropump uses less than $200\,mW$ and the micropump driver approximately $150\,mW$ giving a total power consumption of $350\,mW$. The pump was set up to pump water between $5\,ml/min$ and $7\,ml/min$ according to the product specifications.

Bartel’s mp6 micropump driver requires a supply voltage between $2.5\,V$ and $5.5\,V$. The ADSR output voltage stays between $3.3\,V$ and $3.6\,V$ and could directly power the micropump driver without a low dropout regulator. The supply current was measured with a Tectronix\textsuperscript{20} TDS2014C oscilloscope across a $250\,m\Omega$ sense-resistor between the rectifier output supply and the micropump controller input. Using Excel, the current was multiplied with the measured supply voltage to find an actual power draw of $390\,mW$ for the micropump and controller. This results in an effective DC resistance of $30\,\Omega$ at the average supply voltage of $3.45\,V$ which is approximately a $15\,\Omega$ AC load. The secondary efficiency can be found from the plot for the air core coil shown in Figure 5.4 found using equation (2-38).

With the effective $15\,\Omega$ load, the secondary is expected to be approximately $82\%$ efficient. For a $390\,mW$ load this results in a winding loss of approximately $70\,mW$. The winding loss was measured as in Section 4.4 over four shorting control cycles and was found to be $66\,mW$.

The effective AC load for which maximum power transfer is reached is $100\,\Omega$. This is achieved with an approximate $200\,\Omega$ DC load. With a $3.45\,V$ output voltage, the output power at this load would be $60\,mW$. The coil losses at the maximum power transfer load are equal to the load power. This result is desirable as the winding losses of $66\,mW$ when supplying $390\,mW$ are only $17\%$ larger than the winding losses when supplying $60\,mW$ at

\textsuperscript{20}http://www.tek.com
maximum power transfer. Assuming the load power is not dissipated directly as heat, there will be little difference in heating between powering the micropump and telemeter.

![Secondary Pickup Efficiency](image)

Figure 5.4: Air core coil secondary efficiency when tuned to 600KHz.

5.3. Summary

The integrated circuit ADSR was attached to a wirelessly powered bio-potential telemeter for mice and encapsulated in a 20mm x 15mm x 8mm ceramic shell. Leads were attached directly to the ADSR output to supply a micropump. Tests with an air core coils demonstrate the ADSR can supply the required 390mW for the micropump and micropump driver with only 66mW power dissipation in the secondary IPT pickup. The power dissipation is only 6mW larger than the expected losses when supplying a 60mW load.
Chapter 6  Conclusions and Future Work

6.1. General Conclusions

A rectifier and power flow controller suitable for inductively powering an implantable ICP monitor with a micropump or microvalve has been designed, fabricated and experimentally validated.

With the aim of advancing inductive power transfer management to implantable devices, Hydrocephalus was introduced in Chapter 1 as the motivation for this work. The most common treatment options for hydrocephalus patients were outlined and their shortcomings explained. The exceedingly high shunt failure rate, difficulty of shunt failure detection and cost of detection both economically and socially give motivation for the concept of a smart shunt. An implantable electronic device capable of monitoring, active valve adjustment and blockage prevention could greatly improve hydrocephalus patients’ quality of life. It was concluded that batteries could not practically provide power for lifetime implantation based on the concepts of on-demand ICP monitoring, continuous ICP monitoring and active pump or valve adjustment. The suitability of inductive power transfer to provide lifetime power to an implantable device made it the most feasible power supply choice.

The background of IPT was introduced with key concepts such as pickup resonance and single-turn equivalent values. Important differences between series-tuned pickups and parallel-tuned pickups were outlined. A parallel-tuned pickup allowed a more practical coil design with a lower number of turns for the required load range and selected 600kHz operating frequency. Furthermore, the parallel-tuned pickup maximum efficiency was shown to occur with a smaller load than the maximum power transfer load. This allowed greater secondary pickup efficiency for times of higher power draw such as during pumping.

Following pickup design, different rectifier topologies were introduced and the active diode synchronous rectifier was analysed in detail. Equations for load power, losses and ADSR efficiency were developed. The practical challenges of limiting current spikes were addressed using a proposed soft turn on technique. Power flow control techniques were also introduced and shorting control was found to be suitable for integration within an IC without any additional components. It was shown that shorting control reduced the effective load
resistance seen by the pickup with increased open-circuit voltage. Combined with a parallel-tuned pickup matched to the load for maximum power transfer, the decreased load resulted in increased secondary efficiency. Equations describing this result were developed. It was argued that designing an ADSR and shorting control circuit together on a single IC would provide the smallest implant size and highest performance.

A background into integrated circuit fabrication and the CMOS MOSFET was given to provide insight into the challenges faced in IC design. Some basic but important models and circuit structures were explained. An appropriate technology for the rectifier and SC circuit was selected and a background on the IC design process and design tools was also provided. Requirements and a suitable structure were developed for an IC version of the rectifier and SC circuit. Once the ADSR structure was defined, each sub-circuit was developed. The ADSR bridge transistors were sized to provide minimal heating and high rectifier efficiency. An overview of the full ADSR layout was presented with simulations of the efficiency with output power. The rectifier was expected to be over 90% efficient from 30mW to 600mW. The peak current limiting soft start technique was investigated and found to keep the current close to 1A without a significant effect on efficiency. Power losses in the shorting control transistors were also simulated and lined up closely with the expected analytical values.

Experimental validation was carried out on fabricated ICs in Chapter 4. Due to the limited number of bond pads, only a limited number of sub-circuits could be tested. The experimental results matched well with the simulated results with the exception of the pass transistor body diodes. Fortunately, the measured body diode forward voltage was significantly lower than expected from simulation giving a higher efficiency during start-up. Measurement setups for the ADSR power conversion efficiency, effect of shorting control on secondary pickup efficiency and shorting control power loss were designed. The experimental results for all setups matched closely with the simulations. The ADSR efficiency was greater than 85% with output powers from approximately 30mW to 600mW.

The ADSR was included in a telemeter designed for bio-potential measurements within mice. Except for the pressure sensor, the telemeter demonstrated the small size, necessary components and similar power draw of an ICP monitor. Using the ADSR instead of discrete circuitry removed additional components and allowed a micropump to be included.
6.2. Contributions

The development of an active diode synchronous rectifier and shorting control power flow controller in CMOS has led to contributions not only in integrated circuit power electronic design but also in rectifier and power flow controller analysis, secondary pickup design, and experimental methods for verifying synchronous rectifier performance. The main contributions of this thesis include:

- Designed and fabricated an ADSR integrated circuit suitable for use powering a range of mid-range power active implantable devices including a smart shunt for hydrocephalus.
- The first integrated circuit implementation of shorting control.
- Analysis of the effective load resistance with shorting control (Section 2.7).
- Novel use of the change in effective load resistance from shorting control to increase pickup efficiency with an increase in IPT pickup coupling (Section 2.7 & Section 4.5).
- Novel analysis of current spikes in an ADSR without a DC smoothing inductor (Section 2.5.4).
- Development of a soft-turn-on method to reduce to reduce current spikes in an ADSR rectifier (Section 3.12.3)
- Development of equations characterising the shorting control transistor resistance necessary to remain below a given power dissipation (Section 3.6).
- Improvement of an experimental setup used to calculate the ADSR’s power conversion efficiency providing improved accuracy for measurement results (Section 4.3).
- Development of an analytical equation describing the efficiency and losses in an ADSR (Section 2.5).
- A novel, low-power, band-gap voltage reference circuit was developed (Section 3.10).
- Characterisation of the maximum diode forward voltage drop required for a start-up rectifier to allow ADSR start-up without increased initial field strength or coupling (Section 3.6.1).
- Modification of an existing start-up circuit allowed the design to be implemented with zero static current draw (Section 3.11).
• Implementation of a telemeter with wireless communications and a micropump powered from the designed integrated circuit ADSR (Section 5.1.1).
• Finally, this is the first IC designed, simulated, fabricated and tested at the Auckland Bioengineering Institute. This included, setting up software environment, PDK and identifying the fabrication process appropriate for the ASDR as well as for future use in analogue circuitry to be implemented by the group.

6.3. Publications

6.3.1. Journal Papers

Submitted to IEEE Transactions on Circuits and Systems Part I:
Robert Gallichan, Ho Yan Leung, David M. Budgett, Rezaul Hasan, Aiguo Patrick Hu and Daniel McCormick, “0-600mW Synchronous Rectifier with Integrated Shorting Control for Transcutaneous Energy Transfer to Medical Implants”

Accepted in Cambridge Wireless Power Transfer Journal:

6.3.2. Conference Papers


6.3.3. Conference Abstracts

6.4. Suggestions for Future Work

The following areas of research were identified as useful topics with the potential for improving either the smart-shunt power supply or the ICP monitor:

- Inclusion of signal conditioning circuitry, super capacitor charging circuitry or battery charging circuitry could provide significant decreases in the final ICP monitor size.
- XFAB offers MEMS pressure sensor CMOS integration with IP block that can be purchased for signal conditioning and RF transmission. Currently, the pressure sensor can only be integrated with 0.35\(\mu m\) processes and above. However, this offers great prospects for integration of multiple functions onto one die potentially resulting in an extremely small implant suitable for implantation below the skull.

To improve the ADSR and shorting control performance, the following design features could be added:

- Zero-voltage switching of shorting control. This would be simple to implement and would reduce current spikes and power dissipation in the shorting control transistors.
- Lower delay comparators would allow the rectifier to be used at higher frequencies without significant degradation in efficiency.
- An integrated DC-DC converter would allow the NMA transistors to be driven with a higher voltage during shorting control to reduce the on-resistance. They could also be driven at a higher voltage during rectification. However, this would increase the switching losses resulting in increased efficiency under high power conditions and decreased efficiency under low power conditions.
- A DC-DC converter would allow the rectifier output voltage to be stepped up to charge batteries.

The following design challenges would need to be addressed for the CMOS ADSR to be suitable for production with good yield:

- Fuse or externally programmable voltage reference trimming could improve yield and reduce cost per die. Process variation has a small but significant effect on the voltage reference. Fortunately, all of the tested dice reference voltages were below the +0.7% limit to prevent over voltages from a shorting control threshold increase. However, the simulations predict some of the fabricated dice will have reference voltages with an increase greater than 0.7% resulting in some chips being exposed to over-voltages.
As a rough approximation, between 25% and 30% of the dice are expected to have slight over-voltages.

- Obtaining an IC lifetime estimate for the ADSR is crucial for use in a medical device. Stress testing could be run under strong magnetic fields (large open-circuit voltages) and raised heat to obtain lifetime estimates for the IC. It is expected that chips will survive at least 55 years of continuous operation when used below 85°C. The effect of small over-voltages from voltage reference variation could also be investigated.

- The start-up circuit requires the rectifier output voltage to go back to zero before it can restart the circuit. Hence, if the voltage drops below the minimum voltage reference input voltage ($\approx 2V$) but does not return to zero before rising back above the voltage reference minimum voltage, the start-up circuit does not restart the voltage reference and does not output the correct voltage. Consequently, the active circuitry does not work, the rectifier efficiency is greatly decreased and shorting control does not prevent over-voltages. This would have to be addressed for an implantable medical device.

- Slimming the wafer with wafer grinding would decrease the die thickness.

- The die could have ball bumps added making it suitable for flip chip attachment and decreasing the telemeter size.
Appendix A  Secondary Load Power

The load power for the parallel-tuned pickup is derived based on the open-circuit voltage. The secondary load power can be found from the load voltage calculated in Section 2.3,

\[
V_L = V_{oc} \frac{(R_L/(1 + j \omega C_2 R_L))}{j \omega L_2 + R_2 + R_L/(1 + j \omega C_2 R_L)}
\]

\[
= V_{oc} \frac{R_L}{R_L + R_2 - \omega^2 L_2 C_2 R_L + j \omega L_2 + j \omega C_2 R_L R_2}.
\]  

(A-1)

Substituting \( \omega = 1/\sqrt{C_2 L_2} \) into (A-7) results in,

\[
= V_{oc} \frac{R_L}{R_L + R_2 - R_L + j \sqrt{L_2/C_2} + j \omega \sqrt{C_2/L_2} R_2 R_L}
\]

and multiplying though with the conjugate of the denominator gives,

\[
= V_{oc} \frac{R_L \sqrt{L_2/C_2} + \sqrt{C_2/L_2} R_2^2 R_L + j R_2 R_L}{R_2^2 + (\sqrt{L_2/C_2} + \sqrt{C_2/L_2} R_2 R_L)^2}.
\]

The magnitude of the load voltage is,

\[
|V_L| = V_{oc} \sqrt{R_L^2 + 2 R_L \sqrt{L_2/C_2} + \sqrt{C_2/L_2} R_2 R_L + \sqrt{C_2/L_2} R_2 R_L^2 + \sqrt{L_2/C_2} R_2^2 R_L + \sqrt{L_2/C_2} R_2 R_L^2 + \sqrt{C_2/L_2} R_2 R_L + \sqrt{C_2/L_2} R_2 R_L^2}
\]

\[
= V_{oc} \frac{R_L}{\sqrt{R_2^2 + (\sqrt{L_2/C_2} + \sqrt{C_2/L_2} R_2 R_L)^2}}.
\]

The load power is then,

\[
P_L = \frac{|V_L|^2}{2 R_L} = \frac{V_{oc}^2}{2} \frac{R_L}{R_2^2 + (\sqrt{L_2/C_2} + \sqrt{C_2/L_2} R_2 R_L)^2}.
\]  

(A-2)
Appendices

Appendix B  ADSR Resistive Losses

As current flows through two open switches, for example $P_1$ and $N_2$ in Figure A.1, the power lost in the switch resistance is $P_{\text{loss}}(t) = i(t)^2 R_S$.

![Active diode rectifier circuit diagram](image)

Figure A.1: Active diode rectifier circuit diagram.

Because $i(t)$ is time variant, the average current squared, $E[i(t)]^2$ is different from the average squared current, $E[i(t)^2]$. Hence, we cannot square the average current to calculate $P_{\text{loss}}$. The average squared current can be calculated over one half cycle,

$$E[i(t)^2] = \frac{\omega}{\pi} \int_{T_1}^{T_2} (V_i \sin(\omega t) - V_{DD})^2 / R_S^2 dt$$

$$I_{\text{ave}}^2 = \frac{\omega}{\pi} \int_{T_1}^{T_2} (V_i^2 \sin^2(\omega t) - 2V_iV_{DD}\sin(\omega t) + V_{DD}^2) / R_S^2 dt$$

$$= \frac{\omega}{\pi R_S^2} \frac{V_i^2}{2} \int_{T_1}^{T_2} 1 - \cos(2\omega t) dt - \int_{T_1}^{T_2} 2V_iV_{DD}\sin(\omega t) dt + \int_{T_1}^{T_2} V_{DD}^2 dt$$

The first term integrates to,

$$\frac{V_i^2 \omega}{2\pi R_S^2} \int_{T_1}^{T_2} 1 - \cos(2\omega t) dt = \frac{V_i^2}{2(T_2 - T_1)R_S} \left[ t - \frac{1}{2\omega}\sin(2\omega t) \right]_{T_1}^{T_2}$$

$$\quad = \frac{V_i^2 \omega}{2\pi R_S^2} \left[ \frac{\pi}{\omega} - \frac{1}{\omega} \arcsin \left( \frac{V_{DD}}{V_i} \right) - \frac{1}{2\omega} \sin \left( 2\omega \left( \pi - \arcsin \left( \frac{V_{DD}}{V_i} \right) \right) / \omega \right) - \frac{1}{\omega} \arcsin \left( \frac{V_{DD}}{V_i} \right) \right]$$

$$\quad + \frac{1}{2\omega} \sin \left( 2\omega \arcsin \left( \frac{V_{DD}}{V_i} \right) / \omega \right)$$

$$\quad = \frac{V_i^2 \omega}{2\pi R_S^2} \left[ \frac{\pi}{\omega} - \frac{2}{\omega} \arcsin \left( \frac{V_{DD}}{V_i} \right) + \frac{1}{2\omega} \sin \left( 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) \right) + \frac{1}{2\omega} \sin \left( 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) \right) \right]$$

$$\quad = \frac{V_i^2}{2\pi R_S^2} \left[ \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) + \sin \left( 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) \right) \right]$$

$$\quad = \frac{V_i^2}{2\pi R_S^2} \left[ \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) + 2 \sin \left( \arcsin \left( \frac{V_{DD}}{V_i} \right) \right) \cos \left( \arcsin \left( \frac{V_{DD}}{V_i} \right) \right) \right]$$

162
\[
\frac{V_i^2}{2\pi R_S^2} \left[ \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) + 2 \left( \frac{V_{DD}}{V_i} \right) \sqrt{1 - \left( \frac{V_{DD}}{V_i} \right)^2} \right].
\]

(A-3)

The second term becomes,
\[
- \frac{2V_i V_{DD} \omega}{\pi R_S^2} \int_{T_1}^{T_2} \sin(\omega t) \, dt = \frac{2V_i V_{DD}}{\pi R_S^2} \cos(\omega t) \bigg|_{T_1}^{T_2} = 2V_i V_{DD} \left( -2 \sqrt{1 - \left( \frac{V_{DD}}{V_i} \right)^2} \right).
\]

(A-4)

The third term integrates to,
\[
\frac{\omega}{\pi R_S^2} \int_{T_1}^{T_2} V_{DD}^2 \, dt = \frac{V_{DD}^2}{\pi R_S^2} \left[ \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) \right].
\]

(A-5)

The average squared current is thus,
\[
I_{ave}^2 = \frac{V_i^2}{2\pi R_S^2} \left[ \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) + 2 \left( \frac{V_{DD}}{V_i} \right) \sqrt{1 - \left( \frac{V_{DD}}{V_i} \right)^2} \right]
\]

- \frac{2V_i V_{DD}}{\pi R_S^2} \left( 2 \sqrt{1 - \left( \frac{V_{DD}}{V_i} \right)^2} \right) + \frac{V_{DD}^2}{\pi R_S^2} \left( \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) \right)

\[
I_{ave}^2 = \frac{V_i^2}{2\pi R_S^2} \left( \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) \right) - \frac{3V_i V_{DD}}{\pi R_S^2} \left( \sqrt{1 - \left( \frac{V_{DD}}{V_i} \right)^2} \right)
\]

+ \frac{V_{DD}^2}{\pi R_S^2} \left( \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) \right).
\]

(A-6)

And the average resistive power loss is,
\[
P_{\text{loss-ave}} = \frac{V_i^2}{2\pi R_S} \left( \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) \right) - \frac{3V_i V_{DD}}{\pi R_S} \left( \sqrt{1 - \left( \frac{V_{DD}}{V_i} \right)^2} \right)
\]

+ \frac{V_{DD}^2}{\pi R_S} \left( \pi - 2 \arcsin \left( \frac{V_{DD}}{V_i} \right) \right).
\]

(A-7)
Appendix C  Derivation of Comparator Design Equations

C.1  Threshold Voltages

The positive feedback latch consists of the transistors \(N_5\) through \(N_8\). The circuit has been repeated in Figure A.2 for clarity. The easiest way to analyse this circuit is by starting when \(V_{id}\) is positive making \(i_p > i_p\). Under this condition \(N_7\) and \(N_8\) are on and \(N_5\) and \(N_8\) are in or close to cut-off. The transistors are designed such that \(k_{N_5} = k_{N_6} = k_A\) and \(k_{N_6} = k_{N_7} = k_B\). The current in \(N_7\) tries to mirror the current in \(N_8\) hence,

\[
i_{DN7} = \frac{k_B}{k_A} i_{DN8}. \tag{A-8}
\]

Before the switching point, \(i_{DN8} = i_{p4}\), but \(i_{p3}\) is not large enough to fulfil the condition of (A-8). Therefore, \(N_7\) must be in triode, and \(v_{DSN7} < v_{DSN8}\). At the switching point, \(i_{p3} = (k_B/k_A) i_{p4}\), and (A-8) is met. Just after the switching point, \(i_{p3} > (k_B/k_A) i_{p4}\). From the small signal model, the voltage gain is \(v_{ds} = (i_{p3} - g_m v_{ov}) r_o = (i_{p3} - (k_B/k_A) i_{p4}) r_o\). As \(r_o\) is very large, \(v_{DSN7} = V_{A+}\) increases rapidly until \(N_5\) and \(N_6\) are no longer in cutoff whereupon \(N_6\) pulls \(V_{A-}\) low, and the latch switches. The currents \(i_{p3}\) and \(i_{p4}\) are,

\[
i_{p3} = I_B - (g_m v_{id}/2 + I_{SS}/2) \tag{A-9}
i_{p4} = I_B + (g_m v_{id}/2 - I_{SS}/2)
\]

Substituting (A-8) into (A-7) and rearranging gives the differential voltage required for switching to occur in the latch,

\[
v_{id} = V_{th+} = -V_{th-} = \hat{\beta} \left( \frac{(2I_B - I_{SS})}{g_m} \right) \tag{A-10}
\]

where \(\hat{\beta} = (k_B - k_A)/k_B + k_A\). To introduce offset, the design can be modified such that \(k_{N_5} = k_{N_6} = k_A\), \(k_{N_6} = M_1 k_A\) and \(k_{N_7} = M_2 k_A\). Thus,

\[
V_{th+} = \frac{(M_1 - 1)}{(M_1 + 1)} \left( \frac{(2I_B - I_{SS})}{g_m} \right) \tag{A-11}
\]

\[
V_{th-} = \frac{(M_2 - 1)}{(M_2 + 1)} \left( \frac{(2I_B - I_{SS})}{g_m} \right).
\]

Note that at the positive threshold, \(V_{id}\) is positive, \(V_{A+}\) is negative and \(V_{A-}\) is positive.
C.2 Effect of Device Mismatch on $\hat{\beta}$

If there is a deviation $\Delta$ in the matching between $\beta_A$ and $N \beta_B$ such that $\beta_A = \Delta N \beta$ then $\hat{\beta}_{\Delta}$ is,

$$
\hat{\beta}_{\Delta} = \frac{\Delta M k_A - k_A}{\Delta M k_A + k_A} = \frac{\Delta M - 1}{\Delta M + 1}
$$

The error in $\hat{\beta}$ is defined as, $\varepsilon = \left( k' - \hat{\beta}_{\Delta} \right) / \hat{\beta}$,

$$
\varepsilon = \left( \frac{M - 1}{M + 1} - \frac{\Delta M - 1}{\Delta M + 1} \right) \frac{M + 1}{M - 1} = 1 - \frac{\Delta M^2 + M (\Delta - 1) - 1}{\Delta M^2 + M (1 - \Delta) - 1}. \quad (A-12)
$$
References


References


References


References


References


References

2016].