Copyright Statement

The digital copy of this thesis is protected by the Copyright Act 1994 (New Zealand).

This thesis may be consulted by you, provided you comply with the provisions of the Act and the following conditions of use:

- Any use you make of these documents or images must be for research or private study purposes only, and you may not make them available to any other person.
- Authors control the copyright of their thesis. You will recognize the author's right to be identified as the author of this thesis, and due acknowledgement will be made to the author where appropriate.
- You will obtain the author's permission before publishing any material from their thesis.

General copyright and disclaimer

In addition to the above conditions, authors give their consent for the digital copy of their work to be used subject to the conditions specified on the Library Thesis Consent Form and Deposit Licence.
High-frequency Power Conversion and Variable Capacitor Control for IPT Systems

Jianlong Tian
High-frequency Power Conversion and Variable Capacitor Control for IPT Systems

By

Jianlong Tian

A thesis submitted in partial fulfilment of the requirements for the degree of

Doctor of Philosophy in Engineering

Department of Electrical and Computer Engineering
The University of Auckland

New Zealand
April 2017
Abstract

Wireless Power Transfer (WPT) technology can be dated back to more than 120 years ago with some early work by Tesla. However, practical modern WPT technologies only started in the late 19th century with the invention of high-frequency power electronic devices, which made possible the generation of high frequency voltages and currents efficiently with switch mode power converters. High frequency operation is a prominent feature and essential requirement of WPT systems compared to traditional tightly-coupled transformers and electric machines because of the loosely-coupled nature between the primary and secondary sides of WPT systems. To generate the high frequency voltages and currents for WPT systems, switch mode DC-AC power converters are usually employed, and they are preferably soft-switched for resonant operation in order to maximize the system efficiency and minimize EMI (Electromagnetic Interference).

This research aims to explore new methods to control the operating frequency of WPT systems. Based on the investigation of different types of high frequency resonant converters, including current-fed energy injection converters, Class E, and autonomous push pull converters, this thesis proposes a DC-voltage Controlled Variable Capacitors (DCVC) to dynamically control the zero voltage switching (ZVS) frequency of autonomous push-pull resonant converters for adjusting or stabilizing the operating frequency, and regulating the power flow to keep the output voltage constant.

The equivalent capacitances of DCVCs are varied by controlling the conduction period of a diode in parallel with part of the tuning capacitors of the proposed circuit. In this research the conduction period of the diode is controlled by a DC voltage through two different measures via a bias circuit including a resistor (R-DCVC), or a transistor (T-DCVC). Unlike conventional switch mode capacitors, the proposed DCVCs are controlled smoothly by a DC voltage, so they are more suitable for high frequency operation. In addition, because there are no active switching and related gate drive issues, the EMI (Electromagnetic Interference) of the system can be greatly reduced, and more accurate control can be achieved compared to full switch mode counterpart.

The proposed DCVC method and its detailed operation for different applications are fully analysed in theory, and verified by simulation and experimental results. Both the R-DCVC
and T-DCVC methods have been applied to adjust the ZVS frequency at the primary side of IPT systems. A PLL controller is designed to stabilize the operating frequency of an IPT system while maintaining soft switching conditions, which helps to simplify the pickup circuit design, particularly with multiple power pickups. It has demonstrated that using the proposed DCVC method the operating frequency of an IPT system can be varied or stabilized in the range of a few hundred kHz to tens of MHz. The T-DCVC is also applied at the secondary side of an IPT system as a series or parallel tuned variable capacitor to regulate the power flow to stabilize the output voltage against the magnetic coupling and load variations. A prototype circuit at about 10W has been built and the experimental results have shown that the output voltage can be stabilized in the range of 5V to 24V with an accuracy of 2%, which is sufficient for driving most low power consumer electronic devices.
Acknowledgments

Firstly, I’d like to thank my supervisor Dr. Patrick Hu, because without his introducing me into the field of wireless power transfer (WPT), I would not be able to conduct this research and complete my thesis. As my supervisor, his deep insight, wisdom and positive manner have influenced me greatly. He has always been helpful and encouraging. His valuable guidance has accompanied and escorted me throughout the course of my study, and this has been a key factor for me to succeed in this research.

Secondly, gratitude to my co-supervisor Associate Professor Partha Roop, and Professors John Boys, Grant Covic, Udaya K Madawala and Dr Duleepa Thrimawithana of the Department of Electrical and Computer Engineering, from whom I learnt a lot. Their work gave me inspiration and enlightened new ideas for the improvement of IPT technologies. Special thanks to PowerbyProxi Ltd. for the financial support provided for this research. All the help received is greatly appreciated. Thank you should also go to the Power Electronic (PE) lab technician and manager, Mr. Howard Lu and Mr. Rob Champion. They have helped constantly, in many and various ways. Without their continual support my experiments in the PE lab would not have gone so smoothly.

Thirdly, I would like to thank my friends and classmates Dr. Ali Abdolkhani, Dr. Frank Hao, Dr. Adeel Zaheer, Mr. Liang Huang, Mr. Ermeey Abd Kadir, Ms. Dulsha Abeywardana, Ms. Hoda Rezaie, Mr. Yuan Song, Ms. Yuan liu, Mr. Rong Hua, Mr. Andy Leung, Ms. Jackie Zou, Mr. Lei Zhao, Mr. Zhijia Wang and Ms. Su Zhang for their company, friendship, and various help. Their advice and assistance are highly appreciated. The friendly academic discussions between us have made my study more productive and interesting.

Last but not least, I would like to take this limited space to express my gratitude to my family especially my parents. Without their consistent help and support, it would be difficult to imagine how I could have finished my PhD study.

Jianlong Tian

15 August 2016, Auckland
# Table of Contents

**Abstract** ................................................................................................................................. i

**Acknowledgments** ................................................................................................................ iii

**List of Tables** .......................................................................................................................... xv

**Nomenclature** ............................................................................................................................ xvi

**Chapter 1: Introduction** ........................................................................................................ 1

1.1 Background Development of Wireless Power Transfer Technology ............................... 1

1.2 Traditional Methods for Adjusting the Resonant Frequencies ....................................... 6

1.2.1 Switch Mode Capacitors ................................................................................................. 6

1.2.2 Switch Mode Inductors .................................................................................................. 6

1.3 Objectives and Scope of this Research ............................................................................ 7

1.3.1 High-frequency Resonant Operation ............................................................................. 7

1.3.2 Dynamic Frequency Adjustment and Stabilization ....................................................... 7

1.3.3 Power Flow Control and Output Voltage Regulation .................................................. 8

1.4 Outline of the Thesis .......................................................................................................... 8

**Chapter 2: An Overview of High Frequency IPT Systems** .................................................. 10

2.1 Introduction ......................................................................................................................... 10

2.2 Basic Structure and Operating Principle of an IPT System .......................................... 10

2.3 Traditional Converters ...................................................................................................... 12

2.4 Coupling Approaches ...................................................................................................... 17

2.5 Resonance and Compensation ......................................................................................... 18

2.6 Power Flow Control ......................................................................................................... 20

**Chapter 3: Investigation of High-frequency Power Converters** ........................................ 22

3.1 A New Perspective in Designing High-frequency DC-AC Converters ......................... 22

3.2 Single Side Current-fed Energy Injection Converter ...................................................... 24

3.2.1 The Main Circuit and Basic Operating Principle ......................................................... 25

3.2.2 Zero Voltage Switching Control Method ..................................................................... 26

3.2.3 Circuit Analysis and Simulation .................................................................................. 28
3.2.4 Experimental Results and Discussion ................................................................. 32

3.3 Double Side Current-fed Energy Injection Converters ........................................ 34

3.4 Analysis of Current-fed Energy Injection Converters ........................................ 44
   3.4.1 Basic Principles for Designing Current-fed Energy Injection Converters .......... 44
   3.4.2 Analysis of a few Traditional Converters from the Perspective of Energy Injection .... 45
   3.4.3 Obstacles in Realizing High-frequency Converters and Possible Solutions ........ 47

3.5 A High-frequency (Tens of MHz) Autonomous Push Pull Converter .................. 52

3.6 Summary ............................................................................................................. 53

Chapter 4: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Gate Side DC Voltage Control ................................................................. 55

4.1 Introduction ........................................................................................................ 55

4.2 The Proposed Method and Basic Operating Principle ....................................... 55

4.3 Equivalent Circuit Analysis ............................................................................. 56

4.4 Simulation Study ............................................................................................. 58

4.5 Theoretical Modelling ...................................................................................... 61
   4.5.1 The Instant Capacitances When S1 is Closed and S2 Open ......................... 61
   4.5.2 A Simplified Mathematical Model ............................................................. 65

4.6 Experimental Study ......................................................................................... 74

4.7 Other Methods to Adjust the Gate Voltage .................................................... 79

4.8 Summary ......................................................................................................... 81

Chapter 5: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Resistor-controlled DCVC ................................................................. 82

5.1 Introduction .................................................................................................... 82

5.2 The Proposed Method and Basic Operating Principle .................................... 83

5.3 Theoretical Modelling .................................................................................... 85
   5.3.1 Determination of the Moment When the Diode Stops to Conduct .............. 87
   5.3.2 Determination of the Moment When the Diode Starts to Conduct .............. 87
   5.3.3 The Relationship between $T_{con}$ and $V_c$ .................................................. 89
   5.3.4 The Relationship between $C_e$ and $V_c$ ...................................................... 90
   5.3.5 The Relationship between $f_c$ and $V_c$ ...................................................... 92
5.4 Simulation Study ............................................................................................................ 92
5.5 Experimental Results ................................................................................................. 94
5.6 Summary ................................................................................................................... 97

Chapter 6: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by
Transistor-controlled DCVC ........................................................................................... 98

6.1 Introduction .................................................................................................................. 98
6.2 The T-DCVC and Basic Operating Principle ................................................................. 99
6.3 Theoretical Modelling ................................................................................................ 101
  6.3.1 The Relationship between $T_{con}$ and $V_c$ .............................................................. 102
  6.3.2 The Relationship between $C_e$ and $T_{con}$ .............................................................. 105
  6.3.3 The Relationship between $C_e$ and $V_c$ ................................................................. 108
  6.3.4 The Relationship between $f$ and $V_c$ .................................................................... 108
6.4 Experimental Results ................................................................................................ 109
6.5 Alternative Ways to Control the Voltage on the Anode of the Diode ...................... 112
  6.5.1 Alternative Ways using BJT .................................................................................. 112
  6.5.2 Alternative Ways using MOSFET .......................................................................... 116
  6.5.3 The Situation When the Ground of the Control Voltage is Connected to One End of the
       Resonant Tank ............................................................................................................ 119
6.6 Summary ...................................................................................................................... 120

Chapter 7: Stabilizing the ZVS Frequency of Autonomous Push Pull Converter by PLL
Control ............................................................................................................................ 122

7.1 Introduction .................................................................................................................. 122
7.2 The Overall Strategy and Operating Principle ........................................................... 124
7.3 Circuit Design .............................................................................................................. 125
  7.3.1 The Voltage Matching Circuit before the PD ......................................................... 126
  7.3.2 The Voltage and Current Matching Circuits after the LF ..................................... 127
7.4 Experimental Results ................................................................................................ 132
  7.4.1 Low frequency experiments .................................................................................. 132
  7.4.2 High-frequency Experiments .............................................................................. 136
7.5 Summary ...................................................................................................................... 141

Chapter 8: Output Voltage Regulation of Wireless Power Pick-ups by T-DCVC............. 143
8.1 Introduction .................................................................................................................. 143

8.2 The Parallel Tuning Method ....................................................................................... 143
  8.2.1 Basic Operating Principle of the Parallel Tuning Method .................................. 144
  8.2.2 Theoretical Analysis and Simulation Study ....................................................... 145
  8.2.3 Experimental Results ....................................................................................... 146

8.3 The Serial Tuning Method ......................................................................................... 148
  8.3.1 Basic Operating Principle of the Serial Tuning Method ................................... 148
  8.3.2 Theoretical Modelling and Analysis ................................................................. 150
  8.3.3 Simulation Study ............................................................................................. 153
  8.3.4 Experimental Results ....................................................................................... 156

8.4 Summary .................................................................................................................... 158

Chapter 9: Conclusions and Suggestions for Future Work .............................................. 160
  9.1 General Conclusions .............................................................................................. 160
  9.2 Contributions of this Thesis .................................................................................. 164
  9.3 Suggestions for Future Work ................................................................................ 166

Appendix A ..................................................................................................................... 169

Method to calculate the absolute value of electric charge of a capacitor .......................................................... 169

Appendix B ..................................................................................................................... 172

Detailed derivative process for the relationship between the diode conduction period $T_{con}$ and the equivalent resistance $R_c$ of the controlling MOSFET ...................................................... 172

Appendix C ..................................................................................................................... 182

The detailed derivative process for the equivalent capacitance of a switching mode capacitor from the perspective of its effect on frequency .......................................................... 182
List of Figures

Fig. 2-1. A typical wireless battery charging system for mobile phones [1].
Fig. 2-2. Traditional DC-AC resonant power converters.
Fig. 2-3. The autonomous push pull converter.
Fig. 2-4. The voltage-fed energy injection converter.
Fig. 2-5. The class E converter.
Fig. 2-6. Typical coupling configurations between the track coil and the pick-up [2].
Fig. 2-7. Power flow control methods [2].
Fig. 2-8. Switched-mode controller.
Fig. 3-1. The main circuit of the current-fed energy injection converter.
Fig. 3-2. Establishing initial current for L_D at start up
Fig. 3-3. The energy stored in L_D and V_{DC} injecting into the resonant tank.
Fig. 3-4. The main circuit and its controller of the proposed converter.
Fig. 3-5. The waveform of \( V_{CP} \) and the driving signal for S_T.
Fig. 3-6. The positive reference directions of \( i_{L_1}, i_C \) and \( i_D \)
Fig. 3-7. The waveforms of \( i_{LD}, i_{LP}, i_{CP} \) and the driving signal for S_T (S_TDr).
Fig. 3-8. The currents \( i_{LD}, i_{LP} \) and \( i_{CP} \) during the period S_T is off and S_D is on.
Fig. 3-9. The current directions of \( i_{LD}, i_{LP} \) and \( i_{CP} \) when the energy is being injected into the resonant tank.
Fig. 3-10. The change of the direction of the currents \( i_{CP} \) and \( i_{LP} \) when \( i_{LD} \) is zero.
Fig. 3-11. The waveforms of V_c+ (bottom) and the driving signal for S_T (top).
Fig. 3-12. The waveforms of V_c- (bottom) and the driving signal for S_D (top) at higher frequency.
Fig. 3-13. The waveforms of the current in L_P (bottom) and the driving signal for S_T (top).
Fig. 3-14. The waveform of \( i_{LP}, V_{CP} \) and the driving signal for S_T (S_TDr) when the load is heavy.
Fig. 3-15. Main circuit of the double side energy injection converter.
Fig. 3-16. Control circuit for the double side energy injection converter.
Fig. 3-17. The symmetric waveform of \( i_L, V_c \) and the driving signal for S_2 (S_2_Dr) of the double side energy injection converter as shown in Fig. 3-15.
Fig. 3-18. The main circuit of the discontinuous push pull converter.
Fig. 3-19. The situation when the switches open and close normally.
Fig. 3-20. The situation the switch S2 closes immediately when the current in L2 drops to zero.

Fig. 3-21. The process to generate the signal S2_Dr for driving the switch S2.

Fig. 3-22. The equivalent circuits when the energy is injected from the right side (a), drops to zero (b) and injected from the left side (c).

Fig. 3-23. The periodical process of energy injection and free oscillation.

Fig. 3-24. The control circuit for generating the switch driving signals.

Fig. 3-25. The circuit to delay a square waveform.

Fig. 3-26. The waveforms of $V_{\text{in}}$, $V_{\text{out}}$, $V_c$ and $V_{\text{ref}}$ of the circuit as shown in Fig. 3-25.

Fig. 3-27. ZVS can be achieved for Class E converters during a long period of roughly half a cycle.

Fig. 3-28. The non-ZVS of Class E converters.

Fig. 3-29. Delays caused by the detection and feedback circuitry.

Fig. 3-30. The detection delay problem when the frequency goes up to 10MHz.

Fig. 3-31. The strategy of detecting ZCP in advance.

Fig. 3-32. The strategy of delaying the detected ZCP.

Fig. 3-33. The circuit block diagram to detect the ZCP in advance.

Fig. 3-34. The circuit block diagram to delay the ZCP signal.

Fig. 3-35. Basic circuit structure of the MHz level autonomous push pull converter.

Fig. 3-36. Experimental waveforms of the resonant tank (top) and gate (bottom) voltages of the high-frequency autonomous push pull converter shown in Fig. 3-35.

Fig. 4-1. The basic circuit structure to adjust the frequency of the autonomous push pull converter through parasitic capacitance modulation.

Fig. 4-2. The equivalent circuit when S1 is closed and S2 open.

Fig. 4-3. The equivalent circuit when D1 is open and D2 is short-circuited.

Fig. 4-4. The equivalent circuit when $C_{gd1}$ and $C_{ds1}$ are replaced by $C_2$.

Fig. 4-5. Simulation result of the relationship between the frequency and equivalent capacitance of the converter against the control voltage $V_c$.

Fig. 4-6. Simulation result of the relationship between the peak gate voltage and the control voltage $V_c$.

Fig. 4-7. Simulation result of the relationship between the equivalent capacitance and the peak gate voltage, and the conduction period of the diode and the peak gate voltage.

Fig. 4-8. The coincidence of the relationship between the frequency of the converter and the peak gate voltage when $R_{b1}=R_{b2}=10k\Omega$ and $R_{b1}=R_{b2}=100k\Omega$, respectively.
Fig. 4-9. The coincidence of the relationship between the equivalent capacitance of the converter and the peak gate voltage when Rb1=Rb2=10kΩ and Rb1=Rb2=100kΩ, respectively.

Fig. 4-10. The equivalent circuit of Case 1- D1 conducts and D2 open.

Fig. 4-11. The equivalent circuit of Case 2- D2 conducts and D1 open.

Fig. 4-12. The equivalent circuit of Case 3- both D1 and D2 open.

Fig. 4-13. The equivalent circuit of Case 4- both D1 and D2 conduct.

Fig. 4-14. D1 and D2 conduct during both the period S1 is closed and open.

Fig. 4-15. D1 and D2 close at exactly the moments S1 opens and closes respectively.

Fig. 4-16. D1 and D2 close during the period S1 opens and closes respectively.

Fig. 4-17. The waveforms of V_A, V_B, T_D1 and T_D2.

Fig. 4-18. The circuit used in the simulation to prove that there is not much difference between the frequencies of the transient and steady state responses.

Fig.4-19. The simulated wave of the voltage of the resonant tank (green, top) and the driving signal for the switch S_R (red, bottom).

Fig. 4-20. The situation when the frequency changes from low to high.

Fig. 4-21. The situation when the frequency changes from high to low.

Fig. 4-22. The zoomed-in view of the high-frequency period.

Fig. 4-23. The zoomed-in view of the low frequency period.

Fig. 4-24. The strategy to derive the approximate equivalent capacitance through the concept of input admittance.

Fig. 4-25. The relationship curve between Ce and R1 got from formula (2-10) and simulation.

Fig. 4-26. The relationship curve between f_e and R1 got from formula (2-11) and simulation.

Fig. 4-27. Experimental relationship between the controlling voltage Vc and the frequency of the converter.

Fig. 4-28. Experimental relationship between the control voltage Vc and the peak gate voltage.

Fig. 4-29. Experimental relationship between the peak gate voltage and the calculated parasitic capacitor of the circuit.

Fig. 4-30. Practical circuit experimental waveforms of the controlling voltage Vc (green at the bottom) and the voltage of the resonant tank (yellow on the top) showing the frequency of the converter.

Fig. 4-31. Experimental waveforms of the controlling voltage Vc (green, bottom) and the gate voltage (yellow, top).
Fig. 4-32. The first alternative way to control the voltage on the gates of the two switches S1 and S2.

Fig. 4-33. The second alternative way to control the voltage on the gates of the two switches S1 and S2.

Fig. 5-1 (a). The proposed R-DCVC applied to the autonomous push pull converter.

Fig. 5-1 (b). The double-sided balanced version of R-DCVC applied to the autonomous push pull converter.

Fig. 5-2. The simplified circuit for theoretical analysis of the R-DCVC.

Fig. 5-3. Typical waveforms of the circuit: $V_{\text{cath}}$ (a), $V_{\text{anod}}$ (b) and the period the diode conducts (c).

Fig. 5-4. The equivalent circuit when the diode is conducting.

Fig. 5-5. The equivalent circuit when the diode is not conducting.

Fig. 5-6. Simulation and theoretical analysis results of the relationship between $T_{\text{con}}$ and $V_c$.

Fig. 5-7. Simulation and theoretical analysis results of the relationship between $C_e$ and $V_c$.

Fig. 5-8. Simulation and theoretical analysis results for the relationship between $f_e$ and $V_c$.

Fig. 5-9. Experimental result of the relationship between $f_e$ and $V_c$.

Fig. 5-10. Practical experimental results showing the higher the control voltage is, the lower the frequency.

Fig. 5-11. Practical experimental waveforms at about 10 MHz.

Fig. 6-1 (a). The proposed $T-$DCVC applied to the autonomous push pull converter.

Fig. 6-1 (b). The double-sided balanced version of $T-$DCVC applied to the autonomous push pull converter.

Fig. 6-2. The simplified circuit for theoretical analysis and derivation of approximate equivalent capacitance of the $T-$DCVC.

Fig. 6-3. Typical waveforms of the $T-$DCVC: $v_s$, $V_{\text{cup}}$, $i_D$ and $i_{\text{cup}}$.

Fig. 6-4. The equivalent circuit when the diode is conducting.

Fig. 6-5. The equivalent circuit when the diode is not conducting and the transistor is modelled as a current source.

Fig. 6-6. Theoretical relationship between the diode conduction period $T_{\text{con}}$ and the control voltage $V_c$.

Fig. 6-7. Theoretical relationship between the equivalent capacitance $C_e$ and the diode conduction period $T_{\text{con}}$.

Fig. 6-8. The experimental setup.

Fig. 6-9. Experimental and theoretical relationship between the operating frequency of the converter and the control voltage.
Fig. 6-10. Experimental relationships of the output power $P_{\text{out}}$ (W) and efficiency $\eta$ (%) vs. the control voltage $V_c$.

Fig. 6-11. Experimental waveforms of $v_a$, $\text{COMP\_IN}$, $\text{SIG\_IN}$ and $V_c$ when the reference frequency is set at 1.65MHz.

Fig. 6-12. The situation when the ground of the control voltage $V_c$ is connected to the emitter of $Q_c$.

Fig. 6-13. Simulation results of the two circuits as shown in Fig. 6-1 (a) and Fig. 6-12, respectively.

Fig. 6-14. Experimental results of the two circuits as shown in Fig. 6-1 (a) and Fig. 6-12 respectively.

Fig. 6-15. Simulation and experiment result when the ground of the control voltage is connected to that of the push pull converter.

Fig. 6-16. Simulation and experiment result when the ground of the control voltage is connected to the emitter of the control transistor $Q_{\text{Re}}$.

Fig. 6-17. The circuit structure when a MOSFET instead of a BJT is used and the ground of the control voltage is connected to that of the push pull converter.

Fig. 6-18. The circuit structure when a MOSFET instead of a BJT is used and the ground of the control voltage is connected to the source of the MOSFET.

Fig. 6-19. Simulation results of the two circuits as shown in Fig. 6-17 and Fig. 6-18, respectively.

Fig. 6-20. Practical circuit experimental results of the two circuits as shown in Fig. 6-17 and Fig. 6-18 respectively.

Fig. 6-21. Simulation and experiment result for the circuit as shown in Fig. 6-17.

Fig. 6-22. Simulation and experiment result for the circuit as shown in Fig. 6-18.

Fig. 6-23. The circuit topology using a BJT and with the ground of the control voltage connected to one end of the resonant tank.

Fig. 6-24. The circuit topology using a MOSFET and with the ground of the control voltage connected to one end of the resonant tank.

Fig. 7-1. The three standard components of a normal PLL controller.

Fig. 7-2. Comparison between the proposed method and a PLL control loop.

Fig. 7-3. The voltage matching circuit numbered $\text{①}$ in Fig. 7-2.

Fig. 7-4. The first realization of the voltage and current matching circuit numbered $\text{④}$ in Fig. 7-2.

Fig. 7-5. The second realization of the voltage and current matching circuit numbered $\text{④}$ in Fig. 7-2.

Fig. 7-6. One application example of TL431.
Fig. 7-7. The third realization of the voltage and current matching circuit numbered ④ in Fig. 7-2.

Fig. 7-8. The input and output waveforms of the circuit as shown in Fig. 7-7.

Fig. 7-9. The fourth realization of the voltage and current matching circuit numbered ④ in Fig. 7-2.

Fig. 7-10. The waveforms of $v_a$ (yellow on the top), $V_C$ (green in the middle) and $f_{ref}$ (purple at the bottom) when $f_{ref}$ is set at 230kHz, 235kHz and 242kHz, respectively.

Fig. 7-11. The waveforms of $v_a$ (yellow on the top), $V_C$ (green in the middle) and $f_{ref}$ (purple at the bottom) when $f_{ref}$ is set at a fixed value of 240kHz but the coupling coefficient between the primary and secondary coil changes.

Fig. 7-12. The circuit topology for high-frequency experiments.

Fig. 7-13. The waveforms of $v_A$ (yellow, on the top), $V_C$ (green, in the middle) and $f_{ref}$ (purple, at the bottom) when $f_{ref}$ is set at 10MHz, 9MHz, 8MHz, 7.4MHz and 7MHz, respectively.

Fig. 7-14. The waveforms of $v_A$ (yellow, on the top), $V_C$ (green, in the middle) and $f_{ref}$ (purple, at the bottom) when $f_{ref}$ is set at a fixed value of 6.8MHz but the coupling coefficient between the primary and secondary coil changes.

Fig. 8-1. The parallel tuning method to regulate the output voltage.

Fig. 8-2. Typical waveforms $v_{De}$, $i_c$ and $i_{De}$ when the control voltage is 1V and 10V respectively.

Fig. 8-3. The experimental setup.

Fig. 8-4. Experimental relationships between $V_{out}$ and $V_c$ with $R_b$ at different values.

Fig. 8-5. The transient waveforms of $V_{out}$ (top) and $V_c$ (bottom) when the load resistance changes suddenly from 3.3Ω to 5.3Ω.

Fig. 8-6. The serial tuning method to regulate the output voltage.

Fig. 8-7. The simplified equivalent circuit when the diode is on (a) and off (b), respectively.

Fig. 8-8. The typical wave forms of $v_{ss}$, $i_s$, $v_{CdW}$ and $i_{De}$.

Fig. 8-9. Typical waveforms $i_c$, $v_{CdW}$ and $i_{De}$ when the control voltage $V_c$ is set at 5V and 20V, respectively, and when the diode and transistor are removed from the circuit.

Fig. 8-10. The simulated relationships between $T_{con}$ and $V_c$ under different values of $R_b$.

Fig. 8-11. The simulated relationship between $V_{out}$ and $V_c$ under different values of $R_b$.

Fig. 8-12. The simulated waveforms of $V_{out}$, $V_c$ and the switching signal with which the load resistance $R_{load}$ is changed periodically between 50Ω and 100Ω.

Fig. 8-13. The experimental setup.

Fig. 8-14. Experimental relationships between $V_{out}$ and $V_c$ with $R_b$ at different values.
Fig. 8-15. The transient waveforms of \( V_{out} \) (up) and \( V_c \) (down) when the load changes suddenly from 50\( \Omega \) to 100\( \Omega \).

Fig. A-1. The voltage \( v \) across the capacitor.

Fig. B-1. The objective circuit to be analyzed in appendix B.

Fig. B-2. Typical wave forms of \( v_s \), \( v_{Cup} \) and \( T_{con} \).

Fig. B-3. The equivalent circuit when the diode is conducting.

Fig. B-4. The phase of \( i_s \) is \( \pi/2 \) ahead of that of \( v_s \).

Fig. B-5. The equivalent circuit when the diode is not conducting.

Fig. B-6. The relationship curve between \( T_{con} \) and \( R_c \) got from (B-34), (B-35) and simulation.

Fig. C-1. The scheme to derive the duty cycle \( T_e \).

Fig. C-2. The situation when \( 0 \leq \omega_{on} \cdot T_{on} < \pi \).

Fig. C-3. How the Y-coordinates of two sinusoidal curves with different frequencies equal each other.

Fig. C-4. The situation when \( \pi \leq \omega_{on} \cdot T_{on} < 3\pi/2 \).

Fig. C-5. The situation when \( 3\pi/2 \leq \omega_{on} \cdot T_{on} < 2\pi \).
List of Tables

Table 2-1. Combination of different compensation methods [3].
Table 3-1. Values of the parameters used in the practical experiment.
Table 4-1. The parameters of the components used in the simulation.
Table 4-2. The parameters of the components used in the simulation.
Table 4-3. Parameters used in theoretical calculation.
Table 4-4. Parameters and devices used in the simulation.
Table 4-5. The devices and parameters used in the experiment.
Table 5-1. Major circuit parameters used in simulation and theoretical analysis
Table 6-1. Parameters and components of the primary and secondary side circuits.
Table 6-2. Parameters of the primary and secondary side coils $L_P$ and $L_S$.
Table 6-3. Components and parameters used in the simulation.
Table 6-4. Components and parameters used in the practical experiments.
Table 6-5. Comparison between the results of simulation and practical experiments for the adjustable range of the frequency when the ground of the control voltage is connected to that of the push pull converter and the emitter of the control transistor, respectively.
Table 6-6. Components and parameters used in the simulation and practical circuit experiments for the two circuits as shown in Fig. 5-17 and Fig. 5-18.
Table 7-1. Parameters and components used in the experiments.
Table 8-1. Components and parameters of the circuit used in the experiment.
Table 8-2. Components and parameters of the circuit used in the simulation and experiments.
# Nomenclature

## Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating current</td>
</tr>
<tr>
<td>AVECD</td>
<td>The absolute value of electric charge and discharge of a capacitor</td>
</tr>
<tr>
<td>CLC</td>
<td>Capacitor-inductor–capacitor connection</td>
</tr>
<tr>
<td>CPT</td>
<td>Capacitive power transfer</td>
</tr>
<tr>
<td>DC</td>
<td>Direct current</td>
</tr>
<tr>
<td>DCVC</td>
<td>DC-voltage Controlled Variable Capacitor</td>
</tr>
<tr>
<td>EMC</td>
<td>Electro-magnetic compatibility</td>
</tr>
<tr>
<td>emf</td>
<td>Electro-motive force</td>
</tr>
<tr>
<td>EMI</td>
<td>Electro-magnetic interference</td>
</tr>
<tr>
<td>EMS</td>
<td>Electro-magnetic susceptibility</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent series resistance</td>
</tr>
<tr>
<td>EV’s</td>
<td>Electric vehicles</td>
</tr>
<tr>
<td>ICPT</td>
<td>Inductively coupled power transfer</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated gate bipolar transistor</td>
</tr>
<tr>
<td>IPT</td>
<td>Inductive power transfer</td>
</tr>
<tr>
<td>LCL</td>
<td>Inductor–capacitor-capacitor connection</td>
</tr>
<tr>
<td>LF</td>
<td>Low-pass Filter</td>
</tr>
<tr>
<td>NC</td>
<td>Numerical control</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal oxide silicon field effect transistor</td>
</tr>
<tr>
<td>ms</td>
<td>Milliseconds</td>
</tr>
<tr>
<td>PD</td>
<td>Phase Detector</td>
</tr>
<tr>
<td>PI</td>
<td>Proportional and integral control</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase locked loop</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse width modulation</td>
</tr>
<tr>
<td>Q</td>
<td>Quality factor</td>
</tr>
<tr>
<td>R-DCVC</td>
<td>Resistor-controlled DCVC</td>
</tr>
</tbody>
</table>
RF - Radio frequency
RFI - Radio frequency interference
rms - Root mean square
s - Seconds
T-DCVC - Transistor-controlled DCVC
VCO - Voltage controlled oscillator
VCVCS - Voltage Controlled Variable Capacitor Structure
WPT - Wireless power transfer
ZCP - Zero crossing points
ZCS - Zero current switching
ZVD - Zero voltage detection
ZVS - Zero voltage switching

Symbols

C - Capacitor (Farads)
C_{off} - The instant capacitance when the diode is off (Farads)
C_{on} - The instant capacitance when the diode is on (Farads)
E - Electro-motive force (Voltages)
F - Frequency (Hz)
f_{0} - Undamped natural frequency (Hz)
f_{r} - Zero phase angle resonant frequency (Hz)
f_{fr} - Natural (free ringing) frequency (Hz)
f_{vcm} - Maximum capacitor voltage frequency (Hz)
f_{Lm} - Maximum inductor current frequency (Hz)
f_{zvs} - Zero voltage switching frequency (Hz)
\omega - Angular frequency (radians/s)
i - Instantaneous current (Amperes)
I - Current magnitude (Amperes)
k - Magnetic coupling coefficient
L - Self inductance (Henrys)
M  - Mutual inductance (Henrys)
R  - Resistance (\(\Omega\))
v  - Instantaneous voltage (Volts)
V  - Voltage magnitude (Volts)
\(V_{\text{anod}}\)  - The voltage at the anode of the diode (Volts)
\(V_{\text{cath}}\)  - The voltage at the cathode of the diode (Volts)
\(V_c\)  - The control voltage (Volts)
T  - Time constant (seconds)
\(\phi\)  - Phase angle (radian)
t  - time (seconds)

**Algebraic Notations**

d/dt  - Differential operator
Im  - Imaginary part of a complex expression
Re  - Real part of a complex expression

**Subscripts**

ac  - AC value
dc  - DC value
m  - Maximum value
oc  - Open circuit
p  - Primary track
s  - Secondary pick-ups
sc  - Short circuit
Chapter 1:

Introduction

1.1 Background Development of Wireless Power Transfer Technology

With the rapid development of power electronics, transferring power wirelessly is now possible and has been gaining increasing interest. Traditionally, power is transferred through electric cables, which have drawbacks such as transmission loss, line aging, electric sparks caused by point discharges, the inconvenience brought about by too many wires, etc. The reliability and safety of power supply equipment are weakened by these factors [4, 5]. In special circumstances such as in mines or under water [6], explosion, fire, or electric shock may occur because of the connections in the traditional power transfer circuits. Sliding contacts are usually used for powering moving objects, which can cause problems such as abrasion, sparks, carbon deposition, as well as safety concerns due to the existence of bare current-carrying wires [7-10]. Too many direct wire connections also cause inconvenience in people’s daily life. Therefore, it would be desirable to be able to transfer power wirelessly.

The technique of Wireless Power Transfer (WPT) can be dated back to more than 120 years [11]. In the 1830s, Michael Faraday found that current could be generated in electric wires when the magnetic field around the electric wire changes [11]. In 1888, physicist Hertz demonstrated the generation and transmission of 500MHz pulse energy [11]. Two years later, the first attempt to transfer power wirelessly was made by Nikola Tesla [12]. He tried to build an 8MHz resonant system between the ground and the ionized stratum for transferring power wirelessly via the earth surface. Although this great idea was not realized at the time because of the limitations of early technologies and the lack of financial resources, it has encouraged people to continue the research and development of WPT technologies.
Chapter 1: Introduction

In contrast to the challenges faced by wireless power transfer technology, wireless signal transfer technology developed quickly and became a very mature technique a long time ago. The basic reason for this is that the requirements for transferring power and transferring signals are quite different. What is important in signal transmission is its integrity, which means that how correctly the signal is finally received is the primary concern. However in power transfer, the transfer capability and efficiency are of the primary interest. Consequently, although wireless signal transmission has long been a well-established technology, wireless power transfer achieved little success until recently when high-frequency power semiconductor devices were invented. These devices made possible the generation of high magnitude and high-frequency AC currents and voltages, which are required by modern wireless power transfer systems [2].

Transferring power wirelessly over a long distance is still very challenging today because magnetic fields tend to decay quickly with distance [13], and electromagnetic waves tend to radiate in all directions leading to high power loss in free space [14]. However, it is possible to transfer power across short distances, for example from a few centimetres to tens of centimetres, with the development of modern power electronic technologies [15].

Modern investigation of wireless power transfer technologies can be traced back to the early 1960s, when the research focused mainly on powering electric devices implanted in human bodies [16, 17]. After the 1980s, reports of contactless battery charging for electric vehicles began to appear [18-20]. Since the 1990s, the Power Electronics Research Group at the University of Auckland, New Zealand, led by J. T. Boys, has carried out extensive research on this topic [2], proposing the concept of inductively coupled power transmission (ICPT) systems, and a series of outstanding achievements and breakthroughs have been made [1, 9, 21-24]. The outcomes have been mainly in powering moving equipment in harsh environments such as electric cars, cranes, and material handling equipment or equipment operating under water or in underground mines. The maximum power transmitted has increased to 200kw and efficiency to more than 95% [3]. Due to its unique advantages, Inductive Power Transfer (IPT) – one of the most promising techniques of wireless power transfer technology – has drawn great attention and won extensive acceptance from researchers all over the world. A large amount of research and investigation has been carried out on this topic [2, 25-34] and the outcomes applied to a variety of areas such as wireless battery charging for portable electronic devices like mobile phones [25, 28], electric vehicles [35], and material handling equipment in factories [36, 37]. In 2007, Professor Marin Soljacic
and his team at the Massachusetts Institute of Technology successfully lit up a 60W lamp bulb located 1.9 meters away through electromagnetic resonance from two coils, 30 centimetres in radius [26]. They not only increased the distance of power transferred to meters, but also lowered the effect of the magnetic field on the environment.

Due to the problems of electromagnetic interference and pollution posed by the use of inductive power transfer technology in some cases, researchers are looking for alternative methods of IPT such as transferring power through ultrasonic waves or electric fields. WPT technology can be grouped roughly into the following categories [38]:

- **Inductive Power Transfer (IPT)** [39-43]. IPT is the most developed mature and commonly used technology for WPT. It can transfer power with relatively high efficiencies at close range, and the theory is comparatively simple. However, as magnetic field drops off sharply with distance, IPT technology can only transfer energy from a few millimetres to tens of centimetres [26].

- **Non-radiative Resonant Inductive Power Transfer** [14, 26, 44, 45]. The basic theory of this technique is also non-radiative inductive coupling. However, by making use of the principle of resonance (the fact that two same-frequency resonant objects tend to couple) to generate "strong coupling", the transmission distance can be increased to a few centimetres or even a few meters while maintaining efficiency at 40% to 60%. In addition, there is greater freedom in the positioning of the receiver.

- **Capacitive Power Transfer (CPT)** [46-54]. Unlike IPT which transfers power by inductors through magnetic fields, CPT transfers power by capacitors through electric fields. Compared to IPT, CPT has three advantages. Firstly, there is more freedom in the positioning of the transmitter and the receiver. Secondly, the electrodes can be made very thin, for example a 5 micron copper or aluminium foil, and can be of any shape. These features are very advantageous for fitting them into smart phones which are becoming thinner and thinner. Thirdly, the temperature of the electrodes does not rise because of the high voltage and low current nature of the circuit. This is in contrast to deterioration and reduced life expectancy of batteries situated close to electrodes or coils caused by heating, which is a big problem plaguing other wireless power transfer technologies. In addition to the above strengths, CPT also has the advantage of being able to penetrate through metals, and lower EMI because most of the electric fields can
be confined between the two electrodes of the capacitor [49, 55]. There is relatively less research and development in this field. Currently, Murata is leading this technology [36].

- Resonant Microwave [56-59]. Microwaves are electromagnetic waves between the frequencies of 300 MHz – 300 GHz. The power transfer ability of microwaves is very strong. One example of this is the microwave oven that utilizes the thermal effect of microwaves. However, although microwaves have the potential to be used as a medium to transfer power, one major problem is low efficiency because microwaves generally radiate in all directions and therefore most of its energy will be lost in the free space [14]. In spite of this, Intel is a firm supporter of this technology [38]. An overview of the history of power transmission by radio waves is given by Brown [60].

- Ultrasonic Power Transfer [61-65]. This technology transfers power through ultrasonic waves. The fundamental principle is to transfer electric energy into ultrasonic waves first through piezoelectric material, then receive and transfer it back to electric energy at the receiving end. Compared to other WPT methods, this is a relatively new technology. However, it has many unique advantages such as good directionality, the energy is easy to focus, long transmission distances, the energy can be transferred by various media, no EMI problems, and so on.

Wireless power transfer technology has been applied far and wide. Below is a brief summary of the current hot application and research areas for WPT technology:

- Battery Charging of Electric Vehicles [66-69]: With growing environmental awareness and the serious depletion of natural resources such as coal and oil, electric vehicles are becoming increasingly popular. One major issue facing electric vehicles is that of battery charging. The traditional way of charging the batteries of electric vehicles using plugs and sockets has many disadvantages. The major one is the safety issue created by the bare current-carrying metals of the plugs and sockets. Other problems include electric sparks, dust and carbon deposition, wear and tear, unsuitability for use in hostile environment and weather conditions. Wireless battery charging can overcome the above problems. Further, the weight and size of the electric vehicle batteries can be greatly reduced through convenient frequent recharging and by placing the primary site of the transformer for the battery charging system outside the vehicle.
Chapter 1: Introduction

• Battery Charging of Portable Devices [26, 70-74]. One hot research and application area for wireless power transfer technology is the battery charging of mobile phones. By getting rid of the restriction of electric wires, WPT technology can bring great convenience to people’s daily lives. WPT can also be applied to many other domestic appliances such as electric shavers, electric toothbrushes, etc. As some of these appliances are often used in moist environments, electric connections can create safety issues. By charging the batteries of these appliances wirelessly, the reliability and safety of the appliances is greatly increased.

• Battery Charging of Implants [75-84]. Wireless battery charging of medical implants is one of the most important and traditional applications of wireless power transfer technology. With the development of science and technology, various electric devices have been invented to remedy defects in human organs such as the kidney, liver, heart, eye, cochlea, heart, etc. To do their job, the devices need power which is often provided by batteries. Traditionally, surgery is needed to replace the batteries when they are depleted, or electric wires are connected from outside the body through the skin to the artificial implants to provide the power needed. This not only brings pain and inconvenience to the patient, but also risks infection. In contrast, wireless battery charging overcomes all the above problems so that the quality of life of patients can be greatly improved.

• Industrial Application [85-96]. The unique advantages of wireless power transfer technology have been widely applied in industry such as powering movable objects including monorail trolleys; AGVs (Automatic Guided Vehicles); moving parts within machine tools; for equipment working in areas with special safety requirements such as painting workshops and underground coalmines; or equipment operating in harsh environments such as under water, in the rain, under snow, and other environments where dirt, dust, and chemicals may be present. One of the most important industrial applications of wireless power transfer technology is in robots. As is well known, robots need to be able to move, and too much wire between the moving parts is a great disadvantage. It is not hard to imagine how wireless power transfer technology greatly frees moving parts in robots. There are no concerns about breaking wires. Maintenance costs and operational errors are reduced and the reliability of the whole system significantly increased as a result.
1.2 Traditional Methods for Adjusting the Resonant Frequencies

Methods for adjusting the resonant frequency of IPT systems to make the operating (or driving) frequency and the resonant frequency match each other are very important for maintaining resonant operation. Traditionally this is through switch mode capacitors or inductors, as detailed below.

1.2.1 Switch Mode Capacitors

Capacitors are usually preferred whenever possible because of the bulkiness of inductors. According to the findings of this research, there are two kinds of electrically variable capacitors; the Varactor and Electronically Programmable Capacitors [97-100]. However, the voltage and current ratings of these two kinds of capacitor are not high enough to be used in high power circuits. Ways of overcoming this problem so that they can be used in the dynamic tuning circuits of high power converters are still needed. The most commonly used variable capacitors for WPT applications are switch mode capacitors [21, 75, 101, 102]. It is a simple and straightforward method when soft-switching of the switch in switch mode capacitors is ignored. However, hard-switched switch mode capacitors can cause big problems. It is not only a matter of switching losses, or large EMIs. Sometimes they may seriously influence the normal operation of the main circuit. The realization of soft-switching for switch mode capacitors, however, is usually not easy, increases the complexity of the circuit and has some limitations in its application. Some soft-switched switch mode capacitors have been proposed in other research [103-106].

1.2.2 Switch Mode Inductors

The alternative to capacitors is inductors. There are a number of different kinds of electrically variable inductors. James and colleagues [107] proposed a switching mode inductor working at 38.4 kHz. The frequency of the resonant tank is kept constant by adjusting the current in the switch mode tuning inductor through switches. A “NC (numerical control) variable inductance” is proposed in reference [108]. It consists of two inductors mutually coupled to each other. The inductance of the main inductor can be adjusted by changing the voltage of the auxiliary inductor proportionally to the voltage of the main inductor. Some other strategies to realize electrically variable inductors are presented in references [109-114]. Similar to soft-switched switch mode capacitors, Harada et al. and Chin et al. [103, 104]
proposed some soft-switched switch mode inductors. Although inductors have the disadvantage of being bulky, they have the advantage of high voltage and current ratings lacked by electrically variable capacitors.

1.3 Objectives and Scope of this Research

This research is to propose and develop new methods to control the resonant frequencies of high-frequency IPT systems. New DC-voltage Controlled Variable Capacitors (DCVCs) are developed to adjust and stabilize the soft switching frequencies from the primary side of IPT systems, and to regulate the power flow to keep the output voltage constant at the secondary side power pickups while maintaining the resonant operation. The detailed research tasks include the following aspects.

1.3.1 High-frequency Resonant Operation

The proposed research is based on high frequency resonance of switch mode power converters. Different types of existing resonant converter topologies such as the autonomous push-pull converter, the Class E converter, and the voltage-fed energy injection converter will be investigated first. New converter topologies such as current-fed energy injection converters will be investigated to find their advantages, disadvantages and the suitability for high-frequency operation. The obstacles preventing them from running at high frequencies and ways to overcome these obstacles will be examined carefully. In view of the importance of soft switching and full resonance in realizing high-frequency converters, advanced gate drive control strategies will be evaluated. As the detection and gate driving delays pose major obstacles to realizing soft switching for energy injection and other resonant converters for high frequency operation, autonomous push pull converters with improved gate driving circuits is chosen as the main converter type in this research.

1.3.2 Dynamic Frequency Adjustment and Stabilization

As the frequencies of high-frequency converters tend to vary, and traditional switch mode capacitors may not work at very high frequencies, the major focus of this research is to investigate new methods for adjusting or stabilizing the resonant operating frequency of DC-AC power converters. Various dynamic tuning/detuning methods will be investigated for high-frequency operation. The main focus of this research will be on proposal and development of DC-voltage Controlled Variable Capacitors (DCVCs).
1.3.3 Power Flow Control and Output Voltage Regulation

In addition to applying the DCVCs at the primary side of IPT systems to adjust or stabilize the operating frequencies, this research will also apply the DCVCs at the secondary side of IPT systems for regulating the power flow to keep the output voltage constant by tuning/detuning of the power pickups.

1.4 Outline of the Thesis

This research will focus on low power and high frequency operation of resonant converters, for adjusting and controlling the soft switching frequencies of IPT systems. The thesis chapters are organized as follows.

Chapter 1 conducts the literature review and introduces the overall background, development and current situations of the wireless power transfer (WPT) technology, especially the inductive power transfer (IPT) technology. The characteristics of various traditional DC-AC resonant power converters and traditional methods to adjust the resonant frequency of switch mode converters are the two main focuses of the literature review of this chapter.

Chapter 2 presents a comprehensive literature survey of high frequency IPT systems including the basic structure and operating principle of an IPT system, traditional converters, coupling approaches, resonance, compensation and power flow control techniques, etc.

Chapter 3 presents the results of investigation of new converter topologies and methods for high frequency operation of IPT systems.

Chapter 4 presents the methods to adjust the operating frequency of the high-frequency resonant power converter realized in Chapter 2 with a DC voltage, which is the foundation for the two most important findings of this research, the R-DCVC (Resistor-controlled DCVC) and the T-DCVC (Transistor-controlled DCVC) as will be presented in Chapters 4 and 5.

Chapter 5 presents the R-DCVC realized by controlling the conduction period of a diode directly with a resistor with detailed theoretical analysis and practical experimentation results.

Chapter 6 presents the T-DCVC realized by controlling the conduction period of the diode through a transistor with detailed theoretical analysis and practical experimentation results.
Chapter 1: Introduction

Chapter 7 presents the application of the DCVCs at the primary side of IPT systems for stabilizing the resonant frequency when combined with PLL technology.

Chapter 8 presents the application of the T-DCVC at the secondary side of IPT systems for stabilizing the output voltage when combined with PI controllers.

Finally, Chapter 9 draws the general conclusions, gives the suggestions for future work and makes a summary for the main contributions of this research.
Chapter 2:

An Overview of High Frequency IPT Systems

2.1 Introduction

As mentioned in the last chapter, there are different ways to transfer power wirelessly and new approaches are emerging. However, among the different options, Inductive Power Transfer (IPT) is the most developed one so far, which transfers power from primary to secondary coil through the magnetic field coupling between them generated by the current in the primary coil. However compared to traditional ways of transmitting electricity using cables, the power transfer ability and efficiency of IPT is low [115, 116]. This is because there is usually a relatively large air gap between the primary and secondary coil of an IPT system and magnetic energy drops off sharply with distance [26]. As a result, the magnetic flux reaching the secondary coil from the primary coil is much weaker in IPT applications than in traditional tightly-coupled transformers and electric motors. Generally, this situation is improved from three aspects, i.e.:

- Increasing the frequency of the magnetic field.
- Improving the coupling degree between the primary and secondary coil.
- Making use of the principle of resonance [117].

2.2 Basic Structure and Operating Principle of an IPT System

Fig. 2-1 shows an example IPT system for wireless battery charging of mobile phones [1]. As can be seen, it consists of mainly three parts: the transmitter, the receiver and the communication system between them. The major function of the transmitter is to generate high-frequency current in the primary coil which in turn produces a high-frequency
Chapter 2: An Overview of High Frequency IPT Systems

alternating magnetic field. When the secondary coil comes close to the primary coil, the high-frequency alternating magnetic field generated by the primary coil can induce an electromotive force in the secondary coil according to Faraday’s law of electromagnetic induction as expressed by (1-1):

$$\varepsilon = -\frac{d\Phi_B}{dt}$$  \hspace{1cm} (1-1)

---

Fig. 2-1. A typical wireless battery charging system for mobile phones [1].

Where $\varepsilon$ represents the electromotive force induced in the secondary coil, $\Phi_B$ the magnetic flux through the coil and $\frac{d\Phi_B}{dt}$ the rate of change of the magnetic flux. It can be seen from (1-1) that there are two ways to increase the electromotive force $\varepsilon$ generated in the secondary coil:

- By increasing $\Phi_B$, i.e. the absolute value of the magnetic flux through the secondary coil.
- By increasing the frequency of the alternating magnetic field so that the rate of change of the magnetic flux through the secondary coil $\frac{d\Phi_B}{dt}$ increases.

For IPT applications, the second approach, i.e. increasing the frequency of the alternating magnetic flux is especially important because unlike traditional transformers and electric motors which are tightly-coupled, IPT systems are usually loosely-coupled caused by the relatively larger air gap which always exists in an IPT system (otherwise it cannot be called wireless power transfer). As a result, the magnetic flux reaching the secondary coil from the primary coil is much less in IPT applications than in traditional transformers under the same current intensity in the primary coil because magnetic fields drop off sharply with distance [12]. Therefore, it is hard to get higher electromotive forces by simply increasing the

---
magnetic flux through the secondary coil in IPT applications. This is why wireless power transfer was almost impossible in the past. However, with the development of modern power electronics, power semiconductor devices can work at higher and higher frequencies. Getting a high enough electromotive force in the secondary coil becomes possible nowadays by the second approach, i.e. through increasing the frequency of the alternating magnetic flux through the coil. This is just what has been happening in modern IPT technology [118]. In short, one of the most prominent features of IPT systems is its high frequency. Briefly speaking, IPT systems transfer power from the primary to the secondary coils through the high-frequency alternating magnetic field generated by the high-frequency AC current in the primary coil, which in turn is generated by the converter of the transmitter as shown in Fig. 2-1. Therefore, the design of high-frequency converters plays a very important role in the design of a whole IPT system [118].

2.3 Traditional Converters

Theoretically, there are two approaches to generate the high-frequency AC current in the primary coil of an IPT system. One is through linear amplification. The other is by switching mode power conversion [2]. Being able to generate high quality sine waves is the advantage of linear amplification. However, as the semiconductor devices of this method work in the linear mode, their power consumption is very high. As a result, linear amplification approach is only suitable for low power applications where high quality sine waveform is of primary concern [119]. In contrast, as the semiconductor devices of switch mode power converters work in switching mode, their power consumption is low. As a result, the efficiency of switch mode power converters is high and therefore dominates high power applications such as the IPT system [2].

Theoretically, the input of the switching mode converters can either be AC or DC [2]. However, owning to not being able to produce very high-frequency AC outputs compared to their inputs [120], the existing AC-AC converters are not suitable for IPT applications [2]. The converters used in IPT applications are mostly DC-AC converters [2]. According to the difference of the operation mode, DC-AC converters can be grouped into two categories: PWM converter and resonant converter [3]. Having the advantages of high quality sine waveform (therefore low EMI) and the easiness in realizing soft switching (therefore low switching loss), resonant converters are the most commonly used in IPT systems [3]. Traditional DC-AC resonant converters have four basic structures: voltage-fed full bridge
Chapter 2: An Overview of High Frequency IPT Systems

A converter, voltage-fed half bridge converter, current-fed full bridge converter and current-fed half bridge converter (i.e. push pull converter), as shown in Fig. 2-2 (a), (b), (c), (d), respectively [2]. One issue worth attention in designing the above converters is that the type of the input source and resonant tank should match with each other. Voltage-fed converters must connect to serial resonant tanks because if they are connected to parallel resonant tanks, the voltage source will be short-circuited through the capacitor in the resonant tank when the switches close.

![Fig. 2-2. Traditional DC-AC resonant power converters.](image)

Similarly, current-fed converters must be connected to parallel resonant tanks because if they are connected to serial resonant tanks, the two inductors in the source side and resonant tank will be connected in series, which can cause dangerously high over voltage problems when the switches are closed suddenly because the currents of the two inductors may be different [2]. Another issue that worth mentioning is the unique advantage of the current-fed half bridge structure (the push pull converter) as it does not need high-side gate drivers [2]. [121, 122] propose Push Pull converters working at 30MHz.

In addition to the above four basic structures, there are still some improved topologies and types of converters based on completely new or different design principles, such as the
Chapter 2: An Overview of High Frequency IPT Systems

autonomous push pull converter, the voltage-fed energy injection converter, the class E converters, etc. as shown in Fig. 2-3, Fig. 2-4 and Fig. 2-5 respectively.

Fig. 2-3 shows the autonomous push pull converter. The most prominent advantage of this converter is its simplicity and the ability to realize soft-switching. It can start to oscillate automatically after the power is turned on without the need of any external controllers, and can follow the natural ZVS frequency of the system automatically so that soft-switching is realized [2]. However, the autonomous push pull converter has also some disadvantages such as the gate driving signal being unstable, the operating frequency tending to bifurcate at high frequencies, not suitable for high power applications, etc.

![Fig. 2-3. The autonomous push pull converter.](image)

The disadvantage of the autonomous push pull converter is that its two switches cannot be driven with standard gate drivers so that its gate driving signals are not sharp square waves, and are unstable because the gate driving signals of the autonomous push pull converter depend heavily upon the parameters and working conditions of the circuit, such as the voltage of the source, the coupling coefficient between the primary and secondary coils, the load, etc.. Whenever the above parameters change, the gate driving signals change along so that the circuit may need to be redesigned, otherwise, the circuit may not be started to oscillate automatically at all, or the amplitude of the gate driving signals may be too low or too high, which brings a lot of troubles and is very inconvenient. In fact, stable gate driving signals are very important for switch mode converters to work properly and stably because the behaviour of the circuit is determined by these gate driving signals. For the autonomous push pull converter, however, as standard gate drivers cannot be used, its gate driving signals are not stable sharp square waves. As a means to improve the gate driving signal for the autonomous push pull converter and protect the switches from being driven overvoltage, Zener is often
used at the gates of the autonomous push pull converter. However, as Zener is designed for
and normally used in DC circuits, it is found in the experiments that instead of improving the
gate driving signal, Zener often brings a lot of noise and makes the gate driving signals
worse. This may be because that the behaviour of Zener is different from normal diodes.
Zener is not designed for and suitable to be used at AC circuits, for example at the gates of
the autonomous push pull converter, to solve the gate driving problem. In addition, there
should be a current flowing through the Zener for its normal operation, which adds to the
power losses of the circuit. Also it is proven by experiments that not only gate drivers cannot
be used to improve the gate driving signals of the autonomous push pull converter, even
comparators cannot be used for this purpose neither. It seems that whatever the means used,
as long as the gate driving signals become sharp square waves (not chopped sinusoidal
waves), the autonomous push pull converter cannot be started to oscillate automatically.

In addition to unstable gate driving signals, the frequency of autonomous push pull converter
is unstable either and tends to bifurcate at high frequencies, especially when the primary and
secondary sides are tightly coupled, because the operating frequency of the autonomous push
pull converter follows the frequency of the IPT system, which is unstable at high frequencies
because there may be different resonant frequencies for a high order system, especially at
high frequencies when parasitic parameters (mainly parasitic capacitors) of the circuit cannot
be ignored anymore, which is unstable.

Another big disadvantage of the autonomous push pull converter is that it is not suitable for
high power applications, because at high voltage levels, the resistance of the two resistors $R_A$
and $R_B$ (refer to Fig. 2-3) in the gate driving pass has to be high to limit the current through
the Zener diode. However, when the resistances of $R_A$ and $R_B$ are too large, it can bring some
problems. For example, at the initial period of the zero voltage crossing, the gate driving
voltage will rise very slowly because of the low voltage at the resonant tank and the big
resistances of $R_A$ and $R_B$, which lowers the turn-on speed of the switching devices. The same
is true when the switches are turned off because the big resistances of $R_A$ and $R_B$ make the
discharge of the input capacitor very slow and this can cause turn-off failure. Especially, for
high power applications, high VA rated MOSFETs and IGBTs need to be used. However, the
Miller capacitors of high VA rated MOSFETs and IGBTs are usually also larger which
makes the discharge problem when the switches are turning off more serious. One method to
solve the switch turning on problem is to use speed-up capacitors in parallel with the two
current limiting resistors $R_A$ and $R_B$ as shown in Fig. 2-3. The two speed-up capacitors $C_A$
and $C_B$ can provide a phase advance, therefore accelerate the turn-on speed of the switches. However, they do not have much effect on the turn-off speed of the switches.

Traditional DC-AC converters are mostly designed based on the idea of forced switching. To achieve soft-switching operations, the forced driving frequency of the switches should be equal to the actual system natural ZVS frequency [2], which is not easy when the load changes, especially at start-up. The circuit transient processes during start-up and load transients are usually very complex and difficult to analyse. Unpredicted voltage and current overshoots during start-up and load transients can happen which may lead to the damage of the switching devices or other components [2]. To solve this problem, means for the gate driving frequency to follow and adept to the natural ZVS frequency of the converter are needed.

Fig. 2-4 shows a voltage-fed energy injection converter [2]. It is designed based on the idea of energy injection instead of forced-switching. The components of $C$, $L$, $R$ and $S_2$ as shown in the circuit of Fig. 2-4 constitute a resonant tank. As long as there is enough energy in this resonant tank, it will oscillate at its own natural oscillating frequency. However, as there are always losses in the circuit such as those from the load, it will be an attenuating oscillation. Nevertheless, if the losses of the circuit can be compensated timely, the oscillation can keep going on. In short, the oscillation of the circuit could be maintained by properly controlled energy injection. The voltage-fed energy injection converter as shown in Fig. 2-4 is designed based on this concept. As long as the energy is injected at the zero voltage or current crossing points, soft-switching can be achieved at the same time. Another advantage of this converter is that a high frequency, high magnitude current can be generated with a lower switching frequency and lower magnitude voltage source [2] as long as the energy loss of the circuit can be compensated timely.
Fig. 2-5 shows the typical topology of a Class E converter. The most prominent feature of the Class E converter is its simple structure with only one switch that makes it very suitable for high-frequency operations [60, 103-106, 123-166], high up even to 10MHz [143, 149, 151, 157], 100MHz [146, 147, 150, 155], or several GHz [153, 158-166], because there is no concern about the dead time problem between different switches, and ZVS can be achieved within roughly the period of half a cycle instead of only at an exact point for other types of DC-AC converters such as the push pull converter. Another advantage of the Class E converter is that it can be driven with a fixed frequency while achieving soft switching within a certain range of the variation of the circuit parameters. However, this range is limited and the higher the frequency is, the smaller this range becomes. As a result, class E converters are only suitable for situations where the system has a very stable operating condition especially at high frequencies.

Some modified circuit topologies based on Class E converter are proposed in [130, 145, 167] to enlarge the frequency range in which ZVS can be achieved by increasing the order of the circuits. [104-106] propose methods to adjust the resonant frequency of the converter and [136, 139] propose auto-tuning control methods to guarantee the ZVS condition by detecting the phase difference between the gate driving and the load current signals, and feedback to adjust the gate driving frequency of the converter. [134] make theoretical analyses about the ZVS condition of Class E converters when parameters of the circuit vary.

Some new high-frequency (MHz level) ZVS resonant converter topologies, methods and analyses are proposed in [150, 155, 168-171].

2.4 Coupling Approaches

Fig. 2-6 shows three typical coupling strategies when the primary coil is a long track along which the secondary coil can move [2].
Chapter 2: An Overview of High Frequency IPT Systems

Fig. 2-6. Typical coupling configurations between the track coil and the pick-up [2].

As mentioned at the beginning of Section 2.2, improving the coupling degree between the primary and secondary coils is one of the three approaches to increase the power transfer ability and efficiency of an IPT system. Poor coupling coefficient is often an important reason for undesirable performance of an IPT system. As a result, how to improve the coupling coefficient between the primary and the secondary coils has always been a hot spot research area of IPT technology. Depending on the situation, the coupling strategies differ greatly from case to case. Coupling strategies for other situations can be found in literatures [172-174].

2.5 Resonance and Compensation

Using capacitors to cancel or compensate the inductive impedance of the primary and secondary coils to improve the power factor of the primary side and get more real power output in the secondary side is a very important technique and a cornerstone for nonradioactive WPT such as the IPT technology since the late 19th century [175].

Different from common 50Hz power-frequency transformers, which run at low frequencies, have high coupling coefficients and therefore low reactance, loosely coupled transformers in IPT applications run at high frequencies, have low coupling coefficients and therefore high reactance [3]. This causes high reactive powers in both the primary and secondary sides [3]. With the decrease of the coupling coefficient and the increase of the frequency, the reactance of the primary and the secondary side circuits may multiply several or even several dozen times [3]. As a result, to get a certain level of output power, the voltage of the source must be increased greatly leading to low source utilization. To improve the efficiency of the system, the reactive powers in both the primary and secondary side circuits must be compensated,
which can improve the power factor of the primary side and the output power and efficiency of the secondary side [3].

Table 2-1. Combination of different compensation methods [3].

<table>
<thead>
<tr>
<th>Primary side</th>
<th>Secondary side</th>
</tr>
</thead>
<tbody>
<tr>
<td>No compensation</td>
<td>No compensation</td>
</tr>
<tr>
<td>Serial compensation</td>
<td>Serial compensation</td>
</tr>
<tr>
<td>Parallel compensation</td>
<td>Parallel compensation</td>
</tr>
</tbody>
</table>

As a means to solve the above problem, both the primary and the secondary side of an IPT system are usually compensated with a capacitor in parallel or serial with the primary or secondary side coil. Totally, there are eight combinations of compensation as shown in Table 2-1. When the primary side is compensated in serial, the voltage drops across the compensation capacitor and the primary coil cancel each other under resonant frequency, therefore lowering the voltage demand to the source. When parallel compensated, the currents flowing through the compensation capacitor and the primary coil cancel each other under resonant frequency, hence lowering the current demand to the source. In short, the primary side compensation can improve the power factor and lower the apparent power of the source [3, 176, 177].

When the secondary side is compensated in serial, the voltage drops across the compensation capacitor and the secondary coil cancel each other under resonant frequency, therefore yielding an equivalent pure voltage source on the secondary side [3, 178]. When parallel compensated and under resonant frequency, the current flowing through the compensation capacitor and the reactive part of the current flowing through the secondary admittance cancel each other out, therefore yielding an equivalent pure current source on the secondary side [3, 178]. In both cases, the output power can be increased greatly [3, 176, 177]. However, the increase rate is different depending on the amplitude of the load. When serial compensated, the bigger the load (the smaller the resistance), the higher the output power will be increased; when parallel compensated, the smaller the load (the bigger the resistance), the higher the output power will be [3]. When the load is of medium magnitude, the combination of serial and parallel compensation will yield better results [3].
2.6 Power Flow Control

Basically, there are four ways to stop the power flowing from the primary side to the secondary side as shown in Fig. 2-7 \([2, 179]\).

![Power flow control methods](image)

Moving the secondary coil away or shielding it with a metal plate as shown in Fig. 2-7 (a) and (b), respectively, to decouple the two systems are apparently direct ways to stop the power flow \([2]\). However, as mechanical movements are involved, these two methods are inconvenient \([2]\). An alternative way is to short the secondary coil as shown in Fig. 2-7 (c). When the secondary coil is shorted, the magnetic flux produced by the short circuit current in the secondary coil cancels the magnetic flux produced by the primary coil coupled to the secondary coil, thus the total magnetic flux passing through the secondary coil becomes zero and therefore the power flow ceases \([2, 179]\). Another approach is shown in Fig. 2-7 (d). Obviously no power can be transferred because there is no current in the circuit \([2]\). It should be noted however that this strategy is not suitable for parallel compensated circuits because of their current source nature which does not allow an open circuit \([2]\).

In addition to stopping the power flow completely, often, the magnitude of the power transferred from the primary side to the secondary side needs to be adjusted continuously on a real-time basis. There are basically two ways to realize this when the shape, structure (therefore the mutual inductance of the loosely-coupled transformer) have been fixed. One is by adjusting the current in the primary coil which will influence the electromotive force induced in the secondary coil and therefore the output power of the load \([15]\). The other is through the power flow control circuit in the secondary side. There are basically three approaches to adjust the primary coil current, i.e. frequency control, duty cycle control and voltage control \([172]\).

Fig. 2-8 shows one example to control the power flow in the secondary side \([118]\).
Fig. 2-8. Switched-mode controller.

In this circuit, the voltage induced in inductance $L_2$ is resonated with capacitor $C_2$ to give a higher AC voltage, which is rectified with a bridge rectifier and used as the input to the rest of the circuit [118]. The inductor $L_3$, power diode $D_3$ and power switch $S_3$ constitute a switch mode "Boost" converter. By controlling $S_3$ to work in different switching mode, the voltage and power of the load can be controlled [118]. The disadvantage of this strategy is that the switching loss of $S_3$ will be high when working at high frequencies [15]. Relatively, the strategy to adjust the primary coil current does not have this problem. However, all the secondary pick-ups will be influenced by the primary coil current if it is a multi-load system [15].

In addition to the above approaches, Chapter 8 of this thesis proposes some new methods to adjust and stabilize the output voltage directly at the secondary side by tuning/detuning.
Chapter 3:
Investigation of High-frequency Power Converters

3.1 A New Perspective in Designing High-frequency DC-AC Converters

Modern wireless power transfer (WPT) technology has emerged and advanced with the advent of high-frequency power electronic devices. However, the circuit topologies used in these devices to generate high-frequency currents or voltages have remained much the same over the years. Fundamentally there are two ways of generating the high-frequency currents or voltages for wireless power transfer. One is by linear amplification; the other through switching mode power conversion \[2\]. Linear amplification is not often used for WPT because of the low efficiencies caused by the linear operation of the semiconductor devices \[2\]. The second converter type can be further grouped into two categories: hard switched PWM converters and soft switched resonant converters [3, 180]. Resonant converters have the advantage of being able to generate high quality sinusoidal voltages and currents (thereby low EMI) and simplicity in realizing soft switching (thus low switching loss), and are the most commonly used for WPT [2, 3]. Traditionally, converters are designed from the perspective of conversion - a key concept in power electronics, such as DC-DC conversion, AC-AC conversion, DC-AC conversion and AC-DC conversion [2]. The type of converters used for generating high-frequency currents or voltages needed for WPT are mostly DC-AC converters, which have four basic topologies [2]: voltage-fed full bridge converters, voltage-fed half bridge converters, current-fed full bridge converters, and current-fed half bridge converters or push pull converters, as mentioned in Chapter 2. All of them are switching mode converters with resonant tanks.

A different type of converter, the voltage-fed energy injection converter has been proposed and studied in detail [2, 181-185]. This kind of converter is based on a completely different
concept, i.e. free oscillation and energy injection. As long as there is energy in the resonant tank of this type of converter, the circuit will oscillate automatically. However, as energy is consumed by the resonant components or the load of the circuit, the free oscillation of the resonant tank cannot last long if energy is not continually injected into the circuit. The circuit outside the resonant tank is to replenish the energy consumed so that the free oscillation can continue. Voltage-fed energy injection converters have a very simple structure but suffer from the dead time problem, so the maximum operating frequency is limited.

Class E converters are another type of DC-AC converter, which have been widely used as power amplifiers in radio frequency (RF) systems [124, 125]. A typical class E converter has only one switch and high power efficiency due to its soft switching operation [60, 123]. However, there is very limited operating range to ensure soft switching; otherwise the resonant capacitor may be short circuited causing failure. As a result, class E converters are only suitable for situations where the system has very stable operating conditions.

For high-frequency switch mode power conversion, the realization of soft switching and full resonance is crucial. To achieve these goals, this chapter proposes designing high-frequency switching mode resonant converters from the perspective of energy injection, instead of the traditional concept of forced conversion. The concept of forced conversion is more suitable for designing hard switched non-resonant converters working at low frequencies. Each of the four traditional basic converters used in the WPT systems mentioned above includes a resonant tank, which consists of at least one capacitor and one inductor. As mentioned, as long as there is enough energy in this resonant tank, the circuit will oscillate automatically [2]. There is no need for an external power source to force the energy in the resonant tank to oscillate. However, one problem with this free oscillation is that it cannot last long because there is always energy consumptions in the circuit caused by the load or the equivalent resistances of the circuit. It will be a damping oscillation if there is no new energy injected into the resonant tank. So, to maintain the oscillation, an energy injection is needed. However, the function or purpose of injecting new energy into the circuit is not to force it to oscillate but to keep or maintain the already existing oscillation. Of course, at the beginning, initial energy is needed to start up the oscillation because there is no energy stored in the resonant tank. Nevertheless, when initial energy is injected into the resonant tank and the oscillation has already started up, energy injection more precisely describes the process of injecting new energy into the resonant tank to continue the oscillation than the concept of forced conversion, whereby the natural oscillating of the circuit is not forced to change but
rather followed to fulfil soft switching and resonance. Conversion of energy from one form (DC) to the other (AC) is only the result of this energy injection process. More precisely, the result is obtained not by conversion but by energy injection. From the perspective of energy injection, the problem that needs to be studied is simply how to inject the energy, particularly at what time the energy should be injected. The exact moment when the energy is injected needs to be chosen very carefully, otherwise the energy already existing in the resonant tank will not be increased but cancelled by the injected energy. The differentiation between the concepts of energy injection and conversion is beneficial to the design of soft switching full resonance high-frequency converters. At high frequencies, switches can no longer be treated as ideal devices to convert energies at will without considering soft switching and the natural oscillating process of the resonant tank. At high frequencies, the natural oscillating process of the energy in the resonant tank should be carefully taken into consideration and not be ignored with the assumption that electric energy can be manipulated freely with switches. The use of the concept of energy injection offers a new perspective in designing soft switching full resonance high-frequency converters.

Based on the concept of free oscillation and energy injection, three basic current-fed energy injection converters are proposed in Sections 3.2 and 3.3 of this chapter. They can achieve full resonance and realize either zero voltage switching (ZVS) or zero current switching (ZCS) with no dead time requirements, so they have the potential to operate at much higher frequencies. As there are still no fully established theories for energy injection, some basic principles for the design of current-fed energy injection converters are summarized in Section 3.4. Based on these general principles, the two popular existing converters, the push-pull converter and class E converter are analysed from the perspective of energy injection. In addition, the advantages and disadvantages of voltage-fed and current-fed energy injection converters are compared in this section. Section 3.5 summarizes the major obstacles for designing high-frequency converters and possible solutions. Finally Section 3.6 summarizes the whole chapter.

3.2 Single Side Current-fed Energy Injection Converter

This section presents the single side current-fed energy injection converter which injects energy from only one side of its resonant tank. Section 3.2.1 introduces the main circuit and basic operating principle. Section 3.2.2 describes the zero voltage control method. Section
3.2.3 makes circuit analysis combined with simulation results. Finally, experimental results are presented in Section 3.2.4.

### 3.2.1 The Main Circuit and Basic Operating Principle

Fig. 3-1 shows the main circuit of the proposed current-fed energy injection converter. It consists of a quasi-current source (made up of the voltage source $V_{DC}$ and the inductor $L_D$), a parallel resonant tank (consisting of the capacitor $C_P$, the inductor $L_R$ and the resistor $R_{ESR}$—the equivalent series resistance (ESR) of the inductor $L_P$), and two switches $S_D$ and $S_T$, which are used to control the recharging of the inductor $L_D$ and the energy injection into the resonant tank. The driving signals for the two switches are complementary which means that when $S_D$ is on, $S_T$ is off, and vice versa.

![Fig. 3-1. The main circuit of the current-fed energy injection converter.](image)

At start-up, switch $S_D$ is controlled to be "on" and switch $S_T$ to be "off" for a short time to build the initial current for inductor $L_D$ as shown in Fig. 3-2.

![Fig. 3-2. Establishing initial current for $L_D$ at start up](image)

![Fig. 3-3. The energy stored in $L_D$ and $V_{DC}$ injecting into the resonant tank.](image)
Then the switch $S_T$ is controlled to be "on" and switch $S_D$ to be "off" so that the energy stored in $L_D$ and from the voltage source $V_{DC}$ is injected into the resonant tank through the switch $S_T$ as shown in Fig. 3-3. If sufficient energy is injected, the circuit will oscillate with an approximate sine waveform at an innate ZVS frequency of the resonant tank. Subsequently, the switches $S_D$ and $S_T$ are controlled to be on and off alternately according to the sign of the voltage across the capacitor $C_P$ ($V_{CP}$) of the resonant tank. During the positive half cycles of $V_{CP}$ and at the exact moment when it changes from the negative half cycle to the positive half cycle (so that ZVS can be achieved), switch $S_T$ is be controlled to be "on" and switch $S_D$ to be "off", when the energy stored in $L_D$ and from the voltage source $V_{DC}$ is injected into the resonant tank. During the negative half cycles of $V_{CP}$ and precisely when it changes from the positive half cycle to the negative half cycle, switch $S_D$ is controlled to be "on" and switch $S_T$ to be "off", when the inductor $L_D$ is recharged preparing the energy to be injected into the resonant tank in the next cycle. Full resonance can be maintained by making the switching frequency of the switches $S_D$ and $S_T$ follow the zero voltage crossing (ZVC) points of the resonant voltage $V_{CP}$.

### 3.2.2 Zero Voltage Switching Control Method

Fig. 3-4 shows the schematic to control the current-fed energy injection converter shown in Fig. 3-1.

![Fig. 3-4. The main circuit and its controller of the proposed converter.](image)

As can be seen, it consists of mainly two parts. One is the start-up circuit consisting of $V_{ST}$, $C_{ST}$ and $R_{ST}$, which needs to guarantee that enough energy is injected into the resonant tank at
start-up so that the circuit starts to oscillate and there exists ZVC points for the resonant voltage $V_{CP}$. The other is the ZVC points detection circuit consisting of U1, U2 and U3, which detects the ZVC points and control the on and off of the two switches $S_D$ and $S_T$ with the detected ZVC signal at steady state.

As shown in Fig. 3-4, $S_{DDr}$ and $S_{TDr}$ are the two gate driving signals for the two switches $S_D$ and $S_T$, respectively. As U3 is an inverter, these two signals are complementary meaning that when one is high, the other will be low, and vice versa. The part of the circuit consisting of $V_{ST}$, $C_{ST}$ and $R_{ST}$ constitutes the start-up circuit which generates a transient high voltage $V_{TRAN}$ through the capacitor $C_{ST}$ when the power is turned on. Through the OR gate U2, the two gate driving signals $S_{DDr}$ and $S_{TDr}$ for the two switches $S_D$ and $S_T$ are made high and low, respectively, for some time at start-up so that $S_D$ is closed and $S_T$ is open to build up an initial current in the inductor $L_D$. After start-up, the transient high voltage $V_{TRAN}$ is pulled down to zero by the resistor $R_{ST}$ so that the driving signals $S_{DDr}$ and $S_{TDr}$ for the two switches $S_D$ and $S_T$ become low and high, respectively, making $S_D$ open and $S_T$ close so that the energy built up in the inductor $L_D$ and from the voltage source $V_{DC}$ is injected into the resonant tank. If enough energy is built up in the inductor $L_D$ and injected into the resonant tank, the circuit will start to oscillate and there will be ZVC points in the resonant voltage $V_{CP}$, which can be detected by the comparator U1 and used to generate the gate driving signals for the two switches $S_D$ and $S_T$ as shown in Fig. 3-4. As $V_{TRAN}$ is low after the start-up period, the two gate driving signals $S_{DDr}$ and $S_{TDr}$ at the output of the OR gate U2 will follow the output signal of the comparator U1 at steady state without being influenced by the start-up circuit.

It can be seen from Fig. 3-4 that when the voltage on top side of the capacitor $C_P$ is bigger than the voltage on its bottom side, i.e. when $V_{CP}$ is on its positive half cycle, the output of the comparator U1 and therefore the gate driving signal for switch $S_D$ ($S_{DDr}$) will be low and that for the switch $S_T$ ($S_{TDr}$) high accordingly so that $S_D$ will be opened and $S_T$ closed, when energy will be injected into the resonant tank. This can be seen more clearly in the simulated waveforms of the voltage across the capacitor $C_P$ and the driving signal for the switch $S_T$ as shown in Fig. 3-5.

Similarly, when the voltage on the bottom of $C_P$ is bigger than that on its top, i.e. when $V_{CP}$ is at its negative half cycle, $S_D$ will be closed and $S_T$ open so that $L_D$ will be recharged and the energy in the resonant tank will oscillate freely.
Chapter 3: Investigation of High-frequency Power Converters

Fig. 3-5. The waveform of V_{CP} and the driving signal for S_T.

### 3.2.3 Circuit Analysis and Simulation

Fig. 3-6 shows the situation when the switch S_D opened and S_T closed, i.e. when energy is being injected into the resonant tank.

![Fig. 3-6. The positive reference directions of i_{L1}, i_C and i_D](image)

The differential equation governing $i_{L_P}$ can be expressed as:

$$C_P L_D L_P \frac{d^3 i_{L_P}}{dt^3} + R_{ESR} C_P L_D \frac{d^2 i_{L_P}}{dt^2} + (L_D + L_P) \frac{di_{L_P}}{dt} + R_{ESR} i_{L_P} = V_{DC} \quad (3-1)$$

Using superposition principle and treating capacitor $C_P$ as being charged by $L_D$ and $L_P$ independently, (3-1) can be simplified as:

$$L_P C_P \frac{d^2 i_{L_P}}{dt^2} + R_{ESR} C_P \frac{di_{L_P}}{dt} + i_{L_P} = K_1 \cos(\omega t) + K_2 \sin(\omega t) \quad (3-2)$$

Where: $\omega = \frac{1}{\sqrt{L_D C_P}}$, $K_1 = i_s1(0)$, $K_2 = \frac{V_{DC} + (L_D \alpha - R_L S_1(0) - u_C(0))}{L_D \omega_d}$

The general solution of (3-2) is:

$$i_{L_P}(t) = e^{-\alpha t} [K_3 \cos(\omega_d t) + K_4 \sin(\omega_d t)] + A \cos(\omega t) + B \sin(\omega t) \quad (3-3)$$

Where:
\[ \alpha = \frac{R_{ESR}}{2L_p}, \quad \omega_d = \sqrt{\frac{1}{L_p^2C_p^2} - \frac{R_{ESR}^2}{4L_p^2}}, \quad \omega = \sqrt{\frac{1}{L_d^2C_p^2} - \frac{R_{LD}^2}{4L_d^2}} \]

\[ A = \frac{(1 - \omega^2L_pC_p)K_1 - \omega R_{ESR}C_pK_2}{(1 - \omega^2L_pC_p)^2 - \omega^2R_{ESR}^2C_p^2} \]

\[ B = \frac{(1 - \omega^2L_pC_p)K_2 + \omega R_{ESR}C_pK_1}{(1 - \omega^2L_pC_p)^2 + \omega^2R_{ESR}^2C_p^2} \]

\[ K_3 = i_{L1}(0) - A \]

\[ K_4 = \frac{V_{CP}(0) - (R_{ESR} - \alpha L_p)(i_{LP}(0) - A) - (BL_p\omega + R_{ESR}A)}{L_p \omega_d} \]

Fig. 3-7 shows the simulated waveforms of the currents \(i_{LD}, i_{LP}, i_{CP}\) and the driving signal for \(S_T\) \((S_{TD})\). It can be seen from Fig. 3-7 (b) that \(i_{LP}\) and \(i_{CP}\) coincide almost completely except during the period from \(t_2\) to \(t_3\) when the energy stored in \(L_D\) and from the voltage source \(V_{DC}\) is injected into the resonant tank so that the absolute value of \(i_{CP}\) is bigger than \(i_{LP}\) as shown by the dashed curves at the bottom part of Fig. 3-7 (b).

According to the variation of \(i_{LD}\), the energy injection process during one cycle of \(S_{TD}\), specifically from \(t_0\) to \(t_5\) can be divided into three stages, i.e. when \(i_{LD}\) increases, when \(i_{LD}\) decreases and when \(i_{LD}\) is zero. From \(t_0\) to \(t_2\), the switch \(S_T\) is off and \(S_D\) is on. During this period, the inductor \(L_D\) is charged so that \(i_{LD}\) -the current in it increases almost linearly as shown in Fig. 3-7 (a). The mathematical model governing this charging process is:
Chapter 3: Investigation of High-frequency Power Converters

\[ L_D \frac{di_{LD}(t)}{dt} + R_{LD} \cdot i_{LD}(t) = V_{DC} \]  

(3-4)

Where \( R_{LD} \) is the equivalent serial resistance of the inductor \( L_D \). When the initial value of the current in \( L_D \) is zero, the solution of the equation (3-4) is:

\[ i_{LD}(t) = \frac{V_{DC}}{R_{LD}} \left( 1 - e^{-\frac{R_{LD} t}{L_D}} \right) \]  

(3-5)

By finding the differentiation of the equation (3-5), the current in the inductor \( L_D \) \( i_{LD}(t) \) within a short period of time from the start can be derived as:

\[ i_{LD}(t) \approx \frac{V_{DC}}{L_D} \cdot t \]  

(3-6)

It can be seen from (3-6) that within a short period of time from the start, \( i_{LD}(t) \) increases roughly linearly, which can also be seen clearly from the simulated waveform as shown in Fig. 3-7.

At the same time, the directions of the currents \( i_{LP} \) and \( i_{CP} \) change from positive to negative as shown in Fig. 3-7 (b) and Fig. 3-8 meaning that the energy in the resonant tank is oscillating freely.

![Diagram of the circuit](image)

Fig. 3-8. The currents \( i_{LD}, i_{LP} \) and \( i_{CP} \) during the period \( S_I \) is off and \( S_o \) is on.

The differential equation governing this free oscillation period is:

\[ L_p C_p \frac{d^2V_{CP}(t)}{dt^2} + R_{EST} C_p \frac{dV_{CP}(t)}{dt} + V_{CP}(t) = 0 \]  

(3-7)
Under the condition $R_{ESR} < 2\sqrt{\frac{L_p}{C_P}}$, the solution of equation (3-7) is:

$$V_{CP}(t) = e^{-\alpha t} [K_1 \cos(\omega_d t) + K_2 \sin(\omega_d t)] = Ke^{-\alpha t} \cos(\omega_d t + \varphi)$$  \hspace{1cm} (3-8)

Where:

$$\alpha = \frac{R_{ESR}}{2L_p}, \quad \omega_0 = \frac{1}{\sqrt{L_pC_p}}, \quad \omega_d = \sqrt{\omega_0^2 - \alpha^2}$$

$$K_1 = V_{CP}(0), \quad K_2 = \frac{i_{LP}(0)}{C_p\omega_d} + \frac{\alpha i_{CP}(0)}{\omega_d}$$

$$\varphi = \arctan\left(-\frac{K_2}{K_1}\right), \quad K = \frac{K_1}{\cos\varphi} = -\frac{K_2}{\sin\varphi}$$

As shown in Fig. 3-7, at the point $t_2$, the switch $S_T$ is turned on ($S_D$ is turned off accordingly). From $t_2$ to $t_3$, the energy stored in $L_D$ and from the voltage source $V_{DC}$ is injected into the resonant tank. During this period, the current $i_{LD}$ in the inductor $L_D$ decrease as shown in Fig. 3-7 (a). It can be seen from Fig. 3-7 (b) that this is the only period during which $i_{LP}$ and $i_{CP}$ are different. The dashed curves at the bottom of Fig. 3-7 (b) shows the current $i_{CP}$ while the solid curves show the current $i_{LP}$ and the part of $i_{CP}$ which coincides with $i_{LP}$, from which it can be seen that the absolute value of $i_{CP}$ is bigger than that of $i_{LP}$, which means that the current or energy from the inductor $L_D$ and the voltage source $V_{DC}$ is injected into and stored in the capacitor $C_P$ of the resonant tank.
current $i_{LD}$ remains roughly zero meaning that the energy stored in the inductor $L_D$ has been all injected into the resonant tank, or in other words there is no energy injection into the resonant tank during this period. However, the oscillation of the energy in the resonant tank continues indicated by the change of the direction of the currents $i_{CP}$ and $i_{LP}$ from negative to positive as can be seen from Fig. 3-7 (b). The change of the directions of the currents $i_{CP}$ and $i_{LP}$ during this period can also be seen in Fig. 3-10. It means that the voltage $V_c$ across the capacitor $C$ reaches its maximum at the point $t_4$ and then begins to drop down. Starting from the point 4, instead of being charged, the electric energy stored in the capacitor $C$ begins to discharge. At the end of this stage, specifically at the point $t_5$, the discharge current $i_C$ and $i_{L_1}$ reaches maximum, and then the energy injection process repeats starting from the point $t_0$.

![Diagram](image)

**Fig. 3-10.** The change of the direction of the currents $i_{CP}$ and $i_{LP}$ when $i_{LD}$ is zero.

### 3.2.4 Experimental Results and Discussion

The parameters used in the practical experiments are shown in table 3-1.

<table>
<thead>
<tr>
<th>$V_{DC}$ (V)</th>
<th>$L_D$ (mH)</th>
<th>$L_P$ (uH)</th>
<th>$C_P$ (uF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1</td>
<td>16.5</td>
<td>0.1 ~6</td>
</tr>
</tbody>
</table>

Table 3-1. Values of the parameters used in the practical experiment.

Fig. 3-11 shows the waveforms of the voltage on the top side of the capacitor $C_P$ ($V_{c+}$) and the driving signal for switch $S_T$ at about 6.58 kHz, from which it can be seen that when $S_T$ is closed, $V_{c+}$ is at its positive half cycles, and when $S_T$ is opened, $V_{c+}$ is zero because $S_D$ is closed at the time (Refer to Fig. 3-1). Energy is injected when $S_T$ is closed and $V_{c+}$ is...
positive. Another feature that can be seen from Fig. 3-11 is that switching happens when the voltage is zero meaning ZVS can be achieved.

![Fig. 3-11. The waveforms of Vc+ (bottom) and the driving signal for ST (top).](image)

Fig. 3-12 shows the waveforms of Vc- (at the bottom side of CP) and the driving signal for SD at about 49 kHz together, from which it can be seen that both the driving signal and the waveform of Vc- are a little distorted. The reason for the distortion of the driving signal is that the switches are driven directly by OR gates in the experiment instead of by driving chips. The glitches in the waveform of Vc- are caused by detection delays. The higher the frequency of the system, the more serious the problem caused by detection delays will be. Therefore for the circuit to work at high frequencies, the shorter the detection delay from the real ZVC points of the resonant tank to the rising and trailing edges of the driving signals of
the switches, the better. The detection delay is caused mainly by the propagation delay of the comparator and the OR gates.

Fig. 3-13 shows the waveform of the current in LP and the driving signal for ST. The current shown is about 0.5A. It can be increased further by increasing the voltage and driving ability of the source VDC.

**3.3 Double Side Current-fed Energy Injection Converters**

One problem with the single side energy injection approach is that the positive and negative half cycles of the voltages or current in the resonant tank are asymmetric when the load is heavy which can be seen clearly from Fig. 3-14.
The reason is that energy is injected only at half of the cycle. The amplitude of the voltage across the capacitor \(C_p\) at the half cycle when there is energy injected is bigger than that of the opposite half cycle when there is no energy injected as shown in Fig. 3-14 (b). This is undesirable because there are DC components in the output waveforms. The asymmetric problem can be solved by using topologies which can inject energy from both sides of the capacitor \(C\) in the resonant tank. Fig. 3-15 shows one example of this.

Fig. 3-15. Main circuit of the double side energy injection converter.

Fig. 3-16 shows the control circuit for the double side energy injection converter. It generates the four driving signals \(S1_{Dr}\), \(S2_{Dr}\), \(S3_{Dr}\) and \(S4_{Dr}\) for the four switches \(S1\), \(S2\), \(S3\) and \(S4\), respectively. The function of the four resistors \(R1\), \(R2\), \(R3\) and \(R4\) is to lower the voltage of the resonant tank (composed of \(C\) and \(L\)) so that it can be input into the comparator \(A1\). The output of the comparator \(A1\) is a square wave. Its rising and falling edges represent the ZVC points of the voltage of the resonant tank. \(A2\) and \(A4\) are two OR gates. Their outputs are guaranteed to be high at start-up by the part of the circuit composed of \(U1\), \(C1\) and \(R5\) which generates a pulse signal when the power is turned on. The purpose is to make the two driving signals \(S1_{Dr}\) and \(S3_{Dr}\) to be high at start-up so that the two switches \(S1\) and \(S3\) close for some time to build up an initial current in the two inductors \(L1\) and \(L3\). In this way, enough energy will be injected into the resonant tank after start-up so that the energy in the
resonant tank can oscillate across ZVC points. Only when there is ZVC point at start-up, can the comparator A1 output a continuous square wave to generate the driving signals for the four switches S1, S2, S3 and S4 so that the oscillation of the main circuit can start up and go on continuously.

Fig. 3-17. The symmetric waveform of $i_L$, $v_c$ and the driving signal for S2 (S2_Dr) of the double side energy injection converter as shown in Fig. 3-15.

Fig. 3-17 shows the simulated waveforms of the current of the inductor L, the voltage of the resonant tank $v_c$ and the driving signal for the switch S2, from which it can be seen that the asymmetrical phenomenon shown in Fig. 3-14 disappears. However, the drawback of the circuit topology shown in Fig. 3-15 is its complexity. Two voltage sources and four switches are used. Moreover, the switches S3 and S4 are high side driving switches which increase the complexity of the circuit.

Fig. 3-18. The main circuit of the discontinuous push pull converter.
Chapter 3: Investigation of High-frequency Power Converters

Fig. 3-18 shows another example of double side energy injection converters. It is similar to the push pull converter. The only difference is that two more switches S3 and S4 are added so that the resonant tank can be disconnected completely from the rest of the circuit and oscillate freely when there is no energy injected into it. At the same time, the rest of the circuit can be controlled flexibly as needed without interaction with the resonant tank. This brings some new features to the circuit as detailed below.

One feature is that the push pull converter can now work in discontinuous mode and the amount of energy injected into the resonant tank can be adjusted simply through controlling the duty cycles of the driving signals for the switches. As is well known, for the traditional push pull converter, the inductances of the two DC inductors L1 and L2 need to be large enough so that the currents in them are roughly constant. However there is no such a requirement for the circuit topology shown in Fig. 3-18. The currents in the two DC inductors L1 and L2 in the circuit as shown in Fig. 3-18 can drop to zero so that the circuit can work in discontinuous mode. There is no need for the currents in the two inductors L1 and L2 to keep constant for the circuit topology as shown in Fig. 3-18 because whenever the current in any of the two inductors L1 and L2 drops to zero after the energy in it has been injected into the resonant tank, it can be controlled to be disconnected from the resonant tank immediately by the two switches S3 and S4. After that, the energy in the resonant tank oscillates freely without being interfered by the rest of the circuit and the inductor in which the current has dropped to zero can be recharged immediately or at a later time as needed. The earlier the inductor is recharged, the more energy will be stored in it, and the more energy is stored in the inductor, the more energy will be injected into the resonant tank later. In this way, the amount of energy injected into the resonant tank can be controlled simply by adjusting how long the inductors are recharged.

![Fig. 3-19. The situation when the switches open and close normally.](image-url)
Fig. 3-19 shows the situation when the switches open and close normally which means that the on and off of the switches are controlled only by the voltage of the resonant tank, or in other words, the switches are turned on and off at the ZVC points of the voltage of the resonant tank which has nothing to do with the currents in the two DC inductors L1 and L2. Fig. 3-19 (a) shows the current in the inductor L2 and Fig. 3-19 (b) shows the driving signal for the switch S2, from which it can be seen that when switch S2 is off at the moment t0 (the switch S1 closes accordingly), the energy in the inductor L2 injects into the resonant tank and the current in it decreases quickly and drops to zero at the moment t1. After that, the current in L2 remains to be zero until the moment t2 when the switch S2 is turned on. The current in L2 goes up almost linearly during the period the switch S2 is on from the moment t2 to t3 because the inductor L2 is being recharged through the switch S2 during this period.

In fact, by detecting the currents in the two inductors L1 and L2, the corresponding switches can be controlled to close immediately after the currents in relevant inductors drop to zero without having to wait until the ZVC points of the voltage of the resonant tank so that maximum energy can be stored in the two DC inductors because of the longest recharging time. Although the voltage of the resonant tank is not zero at these moments so that ZVS cannot be achieved, zero current switching (ZCS) can be achieved at these moments because the currents in the relevant inductors are zero at the time. Fig. 3-20 shows the situation the switch S2 is closed immediately when the current in L2 drops to zero.

![Fig. 3-20. The situation the switch S2 closes immediately when the current in L2 drops to zero.](image)

In fact, as shown in Fig. 3-19, the switch can be chosen to be closed at any moment from t1 to t2 so that different amount energy can be stored in the relevant inductor as a result of different recharging time. In this way, the amount energy injected into the resonant tank can be controlled and adjusted flexibly.

Fig. 3-21 shows the process to generate the signal S2_Dr for driving the switch S2, which closes immediately when the current in the inductor L2 drops to zero. Fig. 3-21 (a) shows the
current in the inductor $L_2$. The falling edge of the signal shown in Fig. 3-21 (b) detects the moment when the current in the inductor $L_2$ drops to zero. Fig. 3-21 (c) shows the signal which detects the ZVC points of the voltage of the resonant tank. The signal shown in Fig. 3-21 (d) is the AND of $\text{sign}_1$ and $\text{sign}_2$ as shown in Fig. 3-21 (b) and (c), respectively. Finally, the signal $S_2\_Dr$ as shown in Fig. 3-21 (e) is the inverse of $\text{sign}_3$.

The rising edge of $\text{sign}_2$ represents the moment when the voltage at the point “b” ($v_b$) as shown in Fig. 3-22 becomes larger than the voltage at the point “a” ($v_a$). At this moment, the switches $S_1$, $S_3$ and $S_4$ close and the switch $S_2$ open so that the energy stored in the inductor $L_2$ injects into the resonant tank from the right side as shown in Fig. 3-22 (a).

The moment when the current in the inductor $L_2$ drops to zero is detected by the falling edge of $\text{sign}_1$ which controls the two switches $S_3$ and $S_4$ open through $\text{sign}_3$ so that the resonant tank is disconnected from the rest of the circuit and the energy in it oscillates freely while the...
The rest of the circuit can be controlled as needed without interfering with the free oscillation of the resonant tank. The on period of sign\text{3} is when the current in the inductor \( L_2 \) drops from its maximum value to zero. At the same time, the switch \( S_2 \) is controlled to close immediately to recharge the inductor \( L_2 \) by the signal \( S_2 \_D_r \) which is simply the inverse of sign\text{3}. The equivalent circuit at this stage is shown in Fig. 3-22 (b), from which it can be seen that while the energy in the resonant tank is oscillating freely, both of the two inductors \( L_1 \) and \( L_2 \) are being recharged.

The next turning point is the falling edge of sign\text{2} when the voltage at the point “a” \( (v_a) \) as shown in Fig. 3-22 (b) becomes larger than that at the point “b” with the free oscillation of the energy in the resonant tank. Similar to injecting energy into the resonant tank from the right side, the process of injecting energy into the resonant tank from the left side begins at the moment when \( v_a > v_b \). The switch \( S_1 \) is opened at the moment and the switches \( S_2, S_3 \) and \( S_4 \) closed as shown in Fig. 3-22 (c).

The process of injecting energy from the left side is similar and symmetrical to that of injecting energy from the right side. After the process starts, the current in \( L_1 \) begins to decline. When the current in \( L_1 \) drops to zero, the switches \( S_3 \) and \( S_4 \) are controlled to open and the switch \( S_1 \) closed immediately so that the energy in the resonant tank continues to oscillate freely and the inductor \( L_1 \) is recharged at once. The equivalent circuit at this stage is identical with the one shown in Fig. 3-22 (b). Then when the voltage at the point “b” becomes bigger than that at the point “a”, the whole process repeats starting from injecting energy from the right side again.

![Fig. 3-23. The periodical process of energy injection and free oscillation.](image-url)
The periodical process can be seen more clearly in Fig. 3-23. It can be regarded as starting from the top-left one, i.e. Fig. 3-22 (a). The condition is that the voltage at the point “b” becomes bigger than that at the point “a”, i.e. when \( v_a < v_b \). When the energy in the inductor \( L_2 \) has been injected into the resonant tank and the current in it becomes zero, i.e. when \( i_{L_2} = 0 \), the state of the circuit is changed into the bottom-left one, i.e. Fig. 3-22 (b). When the voltage at the point “a” becomes bigger than that at the point “b”, i.e. when \( v_a > v_b \), the state of the circuit changes into the bottom-right one, i.e. Fig. 3-22 (c). When the energy in the inductor \( L_1 \) is injected into the resonant tank and the current in \( L_1 \) drops to zero, i.e. when \( i_{L_1} = 0 \), the state of the circuit changes into the top-right one, i.e. Fig. 3-22 (b) again. Then when \( v_a < v_b \), the state of the circuit changes into the top-left one, i.e. Fig. 3-22 (a) and the whole process repeats again.

![Fig. 3-24. The control circuit for generating the switch driving signals.](image)

Fig. 3-24 shows the control circuit for generating the corresponding switch driving signals - \( S1\_Dr, S2\_Dr \) for switch S1 and S2, respectively, and \( S34\_Dr \) for the two switches S3 and S4. The two switches S3 and S4 are always turned on and off at the same time based on if there is still energy injecting into the resonant tank so that they use the same driving signal.
Chapter 3: Investigation of High-frequency Power Converters

S34_Dr. They are turned on simultaneously when there is energy injecting into the resonant tank and off together when there is not. Sign1, Sign2 and Sign3 (the same as shown in Fig. 3-21) in Fig. 3-24 govern the process when the energy is injected from the right side. Sign1’, Sign2’ and Sign3’ are their counterparts governing the process when the energy is injected from the left side. The major focus and difficulty of the control circuit is to generate the two signals Sign3 and Sign3’. Their on period represents the time when the currents in the two inductors decline from their maximum value to zero as shown in Fig. 3-21 (Sign3). Once Sign3 and Sign3’ are generated, all the control signals for the switches S1_Dr, S2_Dr and S34_Dr can be produced.

As Sign3’ is only the counterpart of Sign3, Sign3 will be used as an example to explain how these two signals are generated. As can be seen from Fig. 3-21 and Fig. 3-24, Sign3 is produced by Sign1 and Sign2, specifically Sign3 is the AND of Sign1 and Sign2. The reason to produce Sign3 in this way is that the rising and falling edges of Sign3 need to be produced separately.

The rising edge of Sign3 represents the moment when the voltage at the point “b” becomes bigger than that at the point “a” so that the energy stored in the inductor L2 begins to be injected into the resonant tank from the right side and the current in L2 starts to decline. This moment is detected by the rising edge of Sign2 which monitors the zero crossing points of the voltage of the resonant tank as can be seen in Fig. 3-24, where $v_a$ and $v_b$ represent the voltage at the point “a” and “b” of the main circuit, respectively. The four resistors R7, R8, R9 and R10 serve only to scale down the voltage $v_a$ and $v_b$ so that they become low enough to be input into the comparator U3. The output of U3 is a square waveform. Its rising and falling edges represent the zero crossing points of the voltage of the resonant tank.

The falling edge of Sign3 represents the moment when the current in the inductor L2 becomes zero, which is detected by the falling edge of Sign1. As can be seen in Fig. 3-24, Sign1 is generated by the hysteresis comparator U2. The negative input of U2 represents the current signal of the inductor L2. L2’ is an inductor coupled with the inductor L2 to detect the current in it. The detected current signal is transformed into voltage signal through the resistor R2 so that it can be input into the comparator U2. By adjusting the value and ratio of the two resistors R5 and R6, the falling edge of the output of the hysteresis comparator U2 can be adjusted to the point when the current in L2 drops to zero.
Finally, Sign3 can be produced by Sign1 and Sign2 representing the falling and rising edges of Sign3 respectively. The situation of Sign3’ is similar to that of Sign3.

Fig. 3-24 shows the control strategy to make relevant switches close immediately to recharge the corresponding inductors when the currents in them drop to zero. As having been mentioned and shown in Fig. 3-19, it is possible to delay the close of relevant switches to any moment between t1 and t2 as shown in Fig. 3-19. In this way, the relevant inductors can be recharged with different time so that the energy stored in them will be different. As a result, the energy injected into the resonant tank later will also be different so as to realize the goal of adjusting the amount of energy injected into the resonant tank flexibly through changing the duty cycles of relevant switch driving signals.

Fig. 3-25 shows one solution to delay the rising and falling edges of a square waveform. The input signal $V_{in}$ is a square waveform. At the rising edge of $V_{in}$, the transistor Q1 is on and Q2 and Q3 off. As a result, the capacitor C begins to be charged. Assume that the initial value of $V_c$ is smaller than the reference voltage $V_{ref}$, the initial value of the output voltage of the comparator U1 is low. With the charging process going on, the voltage $V_c$ on the capacitor C increases continuously. When the voltage $V_c$ becomes bigger than the reference voltage $V_{ref}$, the output of the comparator U1 becomes high, which means that a rising edge at the output of the comparator U1 is generated some time after the rising edge of the input signal $V_{in}$, or the rising edge of $V_{in}$ is delayed at the output of the comparator U1.

![Fig. 3-25. The circuit to delay a square waveform.](image)

At the falling edge of $V_{in}$, the transistor Q1 is off and Q2, Q3 on, leading to the capacitor C begins to be discharged. When the voltage $V_c$ on the capacitor C declines below the reference voltage $V_{ref}$, the output of the comparator U1 becomes low meaning that a falling edge is
generated some time after the falling edge of $V_{in}$, or the falling edge of $V_{in}$ has been delayed at the output of the comparator U1. The waveforms of $V_{in}$, $V_{out}$, $V_c$ and $V_{ref}$ are shown in Fig. 3-26.

The two transistors Q2 and Q3 constitute a Darlington transistor so that the capacitor C is discharged more quickly than being charged as shown in Fig. 3-26, which leads to the falling edge of $V_{in}$ is delayed less than its rising edge. The value of the resistor $R_2$ in Fig. 3-25 also influences the speed the capacitor C is discharged. The smaller the value of the resistor $R_2$ is, the quicker the capacitor C will be discharged and as a result, the less the falling edge of the signal $V_{in}$ will be delayed. The major means to adjust the delay time of the rising and falling edges of the input signal $V_{in}$ is by changing the value of the reference voltage $V_{ref}$. The higher $V_{ref}$ is, the longer the rising edge of and the shorter the falling edge of $V_{in}$ will be delayed, which can be seen from Fig. 3-26.

**3.4 Analysis of Current-fed Energy Injection Converters**

Investigation of the current-fed energy injection converters is the initial part work of this research, from which some basic principles for designing current-fed energy injection converters, obstacles and possible solutions for realizing high-frequency operation are summarized in this section. Based on these principles, a practical high-frequency autonomous push pull converter is realized in Section 3.5.

**3.4.1 Basic Principles for Designing Current-fed Energy Injection Converters**

Below are some basic principles summarized for designing current-fed energy injection converters.
The main circuit of current-fed energy injection converters consists of three parts: the source part (consists of a DC voltage source and an inductor), the switching network and a parallel resonant tank.

At start up, the inductor of the source part needs to be charged first so that ZVC points in the resonant tank can be detected when the energy stored in this inductor is injected into the resonant tank.

After energy is injected into the resonant tank, the source and the resonant tank should be separated from each other so that the recharging of the inductor of the source part and the oscillation of the resonant tank can go on independently. Otherwise, the oscillation process of the resonant tank will be affected by the inductor of the source side, become very complicated, tend to be unstable and hard to analyse. Alternatively, a very big inductor in the source side or a diode between the source and the resonant tank is needed to stop the energy injected into the resonant tank from flowing back to the source side again. When a diode is inserted between the source and the resonant tank, the selection of the value of the inductor of the source side becomes flexible so that the size and weight of the source inductor can be reduced.

Energy can be injected from just one side of the capacitor of the resonant tank or from both sides. To realize ZVS, energy should be injected at the zero crossing points of the voltage across the capacitor during the positive half cycle of the corresponding side.

When the injecting current drops to zero, the resonant tank and the source can be controlled to separate from each other immediately so that the inductor of the source can be recharged at once and the diode needed for blocking the energy in the resonant tank from flowing back to the source side can be removed. Zero current switching (ZCS) can be achieved if the switches are turned on and off at this moment, i.e. when the current in the inductor of the source side drops to zero.

3.4.2 Analysis of a few Traditional Converters from the Perspective of Energy Injection

Fig. 2-3 and 2-5 in Chapter 2 show the circuit topologies of the autonomous push-pull and class E converters, respectively. Viewed from the point of the basic principles for designing current-fed energy injection converters mentioned above, both of them can be regarded as current-fed energy injection converters because both of them have a quasi-current source.
composed of a DC voltage source in series with a big inductor, which inject energy into a parallel resonant tank on the positive half cycles of the voltage across the capacitor of the resonant tank through certain switch network. The most prominent advantage of these two converters is their simplicity in structure. The push-pull converter uses only two switches to realize double side energy injection compared to four switches used in the topologies as shown in Fig. 3-15 and Fig. 3-18, while the class E converter uses only one switch to achieve single side energy injection in contrast to two switches used in the topology shown in Fig. 3-1. This simplicity, however, introduces a common problem for them, i.e. the source parts of them cannot be separated from their resonant tanks after energy is injected, which, as a result, requires big inductors used in their source sides [2, 123-125] to prevent the energy in their resonant tank from flowing back to the source. Otherwise, oscillation can occur between the inductors of the source side and the capacitor in the resonant tank, which makes the whole oscillation process much more complicated, difficult to analyse and control. Therefore, to some extent, these two converters are current-fed energy injection converters, but not exactly from the perspective of the principles summarized at the beginning of this section.

Fig. 2-4 in chapter 2 shows the main circuit topology of the voltage-fed energy injection converter [180, 181, 183, 185]. The major characteristics of the voltage-fed energy injection converter in comparison with those of the current-fed energy injection converter as shown in Fig. 3-1 of this chapter are summarized below:

**Advantages of the voltage-fed energy injection converter:**

- The topology of the main circuit of the voltage-fed energy injection converter is simpler than that of the current-fed energy injection converter because the later uses one more inductor $L_D$ as shown in Fig. 3-1. Moreover, the control circuit of the voltage-fed converter is also simpler than that of the current-fed converter because the later has to include some control logic to charge the inductor $L_D$ first at start up.

- The waveforms of the current of the inductor in the resonant tank of the voltage-fed converter are symmetrical between their positive and negative half cycles while they are asymmetrical for the current-fed converter as shown in Fig. 3-1.

**Disadvantages of the voltage-fed energy injection converter:**

- The voltage-fed converter has a high-side driving switch $S_1$ while both of the two switches of the current-fed converter as shown in Fig. 3-1 are low-side driving switches.
The switch S2 is included in the serial resonant tank of the voltage-fed energy injection converter to constitute a closed loop for oscillation after the energy is injected while there is no such a need for current-fed energy injection converters. As the current of the resonant tank of the voltage-fed energy injection converter is generally much larger than those parts of the circuit outside the resonant tank, switches included in resonant tank usually consume more energy.

- If the two switches of the voltage-fed energy injection converter close at the same time, the voltage source will be shorted, so there is a deadline problem for the voltage-fed energy injection converter.

- The voltage-fed energy injection converter has to detect the current in the resonant tank as a feedback to control the on and off of the switches while the current-fed energy injection converter detects the voltage of the resonant tank which is more convenient in most cases.

### 3.4.3 Obstacles in Realizing High-frequency Converters and Possible Solutions

Theoretically, according to Faraday's law of electromagnetic induction, increasing the operating frequency of IPT systems is a fundamental way to increase their power transfer abilities. Practically, however, it is not easy to build high-frequency DC-AC converters for generating the high-frequency currents or voltages used for WPT. According to the study of this research, generally there are two main obstacles to building high-frequency converters as below:

- The dead time problem
- The switching loss problem caused by hard switching

Voltage-fed converters generally have both of the above two problems. Current-fed converters usually have only the switching loss problem because there is no concern about dead time in the practical design of current-fed (especially push-push) converters as practical switches turn on faster than they turn off, and there is a short period both switches turn on, which is not a problem for a current source input. Class E converters are an exception. They have neither of the above two problems because they use only one switch and can realize ZVS automatically when the resonant frequency of the system is stable. As a result, Class E converters are traditionally the first choice for high-frequency converters. They do not detect...
the frequency of the resonant tank but drive the only switch with a fixed frequency and can achieve soft switching within a certain scope instead of at only one point like other converters. This is because of the existence of the body diode in their switches or an externally added one which clamps the negative half cycle of the voltage across the resonant tank (refer to Fig. 2-5 in Chapter 2) to roughly zero \[123-125\] so that ZVS can be achieved during a long period of roughly half a cycle as shown in Fig. 3-27.

Fig. 3-27. ZVS can be achieved for Class E converters during a long period of roughly half a cycle.

Moreover, Class E converters are driven with a fixed frequency which is an advantage over the autonomous push pull converters, the frequencies of which vary. Fixed frequency is usually preferable for IPT systems. However, to guarantee soft switching, Class E converters require that the natural oscillating frequency of the resonant tank should be very stable because the scope at which Class E converters can achieve soft switching is only about half a cycle of the natural frequency of their resonant tanks, which gets smaller and smaller with the increase of the frequency. If the natural oscillating frequency of the resonant tank is different from the fixed switch driving frequency, soft-switching may not be achieved as shown in Fig. 3-28.

Fig. 3-28. The non-ZVS of Class E converters.

In short, class E converters can run at high frequencies at a limited scope under the condition of having a very stable resonant tank. However, if the natural oscillating frequency of the
resonant tank is not stable, ZVS is not guaranteed, especially at high frequencies, which limits the application of Class E converters for high-frequency operations.

As current-fed energy injection converters do not have the dead time problem, they are very promising for high-frequency operations if the switching loss problem can be solved. The switching loss problem is caused by hard switching due to the inconsistency between the gate driving frequency and the natural ZVS frequency of the resonant tank. To reduce the switching loss, soft switching, i.e. driving the switches at exactly the zero voltage or current crossing points is needed, which requires that the gate driving frequency follow the natural ZVS frequency of the resonant tank. To achieve this, the natural ZVS frequency of the resonant tank needs to be detected first. However, detection has delays, or in other words, there are propagation delays for the detection and feedback circuitry. Furthermore, gate drivers also have delays between their inputs and outputs. At high frequencies, these delays become very significant so that cannot be ignored anymore. In fact, they are the major obstacles to limit the frequencies to be increased further because the detection or propagation delay makes the gate driving signals lag behind the actual ZVS points of the resonant tank.

![Fig. 3-29. Delays caused by the detection and feedback circuitry.](image)

Fig. 3-29 shows how long the detection and feedback delay can add up to even if almost the fastest detection, control and driving components are used.

Fig. 3-30 shows how serious the detection delay problem can be at high-frequency operations. The 10MHz sine wave in Fig. 3-30 represents the voltage of the resonant tank. The period of a 10MHz sine wave is 100ns. The time from the zero crossing point to the peak value is only 25ns. It can be seen from Fig. 3-30 that the actual gate driving signal goes almost to the peak amplitude after an 18.9ns delay for 10MHz operations, which is no longer soft switching at all. The switching loss caused by such big detection delays is simply too high to be acceptable. As a result, it is not realistic to detect the frequency of the resonant tank.
Chapter 3: Investigation of High-frequency Power Converters

tank first and then use the detected signal to drive the switches directly at high-frequency operations.

![Fig. 3-30. The detection delay problem when the frequency goes up to 10MHz.](image)

In summary, detection delay constitutes the biggest obstacle to realizing high-frequency converters. According to the study of this research, three possible means to bypass or overcome the detection delay problem are summarized below:

- Open loop control without detections such as the class E converter
- Autonomous push pull converter, the detection delay of which is nearly zero
- Detecting the Zero Crossing Points (ZCP) of the voltage or current in advance or delaying the detected ZCP signal

Fig. 3-31 shows the strategy to detect ZCP in advance so that after the feedback delay it can drive the switches at exactly the ZCP.

![Fig. 3-31. The strategy of detecting ZCP in advance.](image)
Fig. 3-32 shows the strategy to delay the detected ZCP signal and using it as the switch driving signal in the next oscillation cycle.

![Fig. 3-32. The strategy of delaying the detected ZCP.](image)

Fig. 3-32 and Fig. 3-34 illustrate the circuit block diagrams to realize these two strategies. Both of them use a phase detector to compare the phase difference between the ZCP signal and the real switch driving signal. The difference between these two strategies is that one uses the phase difference to adjust how much the ZCP should be detected in advance while the other uses it to adjust how much the ZCP signal should be delayed. In general, the ZCP delay strategy is simpler and easier to realize than the strategy to detect the ZCP in advance because the later needs to detect not only the ZCP but also the ZCP in advance. What is worse, detecting the ZCP in advance is very difficult or even impossible sometimes like in
the case of push pull converters because the signal being detected only has the positive half cycles of a sine wave.

The next section will introduce the method to realize high-frequency operation with the autonomous push pull converter, which does not have the dead time and detection delay problems but suffer from the problem of low switch driving ability.

### 3.5 A High-frequency (Tens of MHz) Autonomous Push Pull Converter

Fig. 3-35 shows the circuit structure of the high-frequency autonomous push pull converter, which can run at tens of MHz (maximum 70MHz in the experiment) with the amplitude of the voltage of the resonant tank being about 30 volts.

![Basic circuit structure of the MHz level autonomous push pull converter.](image)

As can be seen, instead of using resistors as the autonomous push pull converter introduced in Chapter 7 of [185], the one shown in Fig. 3-35 uses capacitors in parallel with diodes connected between the resonant tank and the gates of the two switches as gate drivers. The capacitors used (C1 and C2) makes the rising edges of the gate driving signals sharper than when only resistors are used, and the diodes (D1 and D2) makes the falling edges of the gate driving signals sharper because the input capacitances of the two switches can be discharged more quickly than when only resistors are used. These features improve the gate driving condition of the converter making it more suitable for high-frequency operations.

Another feature which can be seen from Fig. 3-35 is that different from the autonomous push pull converter introduced in Chapter 7 of [185], the one shown in Fig. 3-35 does not include a resonant capacitor in its resonant tank. Instead, the capacitance and parasitic capacitances of the circuit itself, mainly C1, C2 and the parasitic capacitances of the two switches S1 and S2...
are used as resonant capacitances. As explained in more details with equivalent circuit analysis in the next chapter, these capacitances are in parallel with the resonant inductor $L$ of the resonant tank, so they can act as resonant capacitors. As only $C_1$, $C_2$ and small parasitic capacitances of the circuit are used as resonant capacitances, the frequency of the converter can go to very high levels because the frequency of the converter is determined by the values of the resonant capacitances and inductances, and the smaller the resonant capacitances and inductances are, the higher the frequency of the converter. In the experiments, the power MOSFET FDS86106 is used as the two switches $S_1$ and $S_2$ of the converter, which has very small parasitic capacitances, so the frequency of the converter can go to tens of MHz depending on the value of the resonant inductor $L$ of the resonant tank used. Fig. 3-36 shows the experimental waveform of the resonant tank (top) and gate (bottom) voltages at more than 50MHz when the value of the resonant inductor $L$ is about 0.14uH.

![Fig. 3-36. Experimental waveforms of the resonant tank (top) and gate (bottom) voltages of the high-frequency autonomous push pull converter shown in Fig. 3-35.](image)

### 3.6 Summary

This chapter studied the general characteristics of some conventional resonant power converters such as the Class E converter, the autonomous push pull converter, the voltage-fed energy injection converter, etc. and proposed and explored a few new circuit topologies, specifically, one single-side current-fed energy injection converter and two double-side current-fed energy injection converters. Based on these investigations and explorations, some basic principles for designing current-fed energy injection converters are summarized, the
advantages and disadvantages of current-fed and voltage-fed energy injection converters compared, the obstacles in realizing high-frequency converters analysed and possible solutions suggested. A high-frequency autonomous push pull converter was realized which can operate at tens of MHz by making use of the parasitic capacitances of the circuit and small resonant inductors.

To realize high-frequency operation with low switching losses, soft switched resonant converters are a common choice. As current-fed resonant converters usually do not have the dead time problem, and the push-pull topology has no common ground gate drive issues, current-fed push-pull resonant converters are chosen to be the base converter in the next step of this research.
Chapter 4:
Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Gate Side DC Voltage Control

4.1 Introduction

Parasitic parameters can be used advantageously to achieve high-frequency operation of autonomous push pull converter at tens of MHz or even higher. However, as no external capacitors are used for tuning the circuit for high frequency operation, traditional ways to adjusting the frequency of the converter with switching mode capacitors can no longer be used. This chapter proposes a method to achieve ZVS frequency adjustment of the autonomous push pull converter (see Fig. 3-35 in Chapter 3) by DC voltage control at its gate side. The method proposed in this chapter will lead to the proposal of DC-voltage Controlled Variable Capacitors (DCVC) to be presented in details in Chapters 5 and 6.

4.2 The Proposed Method and Basic Operating Principle

Fig. 4-1 shows the basic circuit structure of the method to adjust the ZVS frequency of the high-frequency autonomous push pull converter by taking advantage of the parasitic capacitances Cds1, Cgd1, Cgs1 (for switch S1), Cds2, Cgd2, Cgs2 (for switch S2), and the two feedback capacitors C1 and C2, respectively. The two transistors Q1 and Q2 in Fig. 4-1 function as variable resistors. Their equivalent resistances are controlled by the voltage Vc through the two base resistors Rb1 and Rb2. When the resistances of Q1 and Q2 change, the gate voltages of the two switches S1 and S2 change also, which have an influence on the conduction periods of the two diodes D1 and D2. When the diodes conducts, the two capacitors C1 and C2 are short-circuited so that the total capacitance of the circuit changes. In short, the equivalent capacitance of the circuit changes with the variation of the conduction periods of the two diodes. As the conduction periods of the two diodes can be controlled by
the equivalent resistances of the two transistors Q1, Q2 and the equivalent resistance of Q1 and Q2 can be controlled by the controlling voltage \( V_c \), the equivalent capacitance of the circuit and therefore the frequency of the converter can finally be controlled by the voltage \( V_c \).

![Fig. 4-1. The basic circuit structure to adjust the frequency of the autonomous push pull converter through parasitic capacitance modulation.](image)

### 4.3 Equivalent Circuit Analysis

Fig. 4-2 shows the equivalent circuit of Fig. 4-1 when the switch S1 is closed and S2 open.

![Fig. 4-2. The equivalent circuit when S1 is closed and S2 open.](image)

The output parasitic capacitance \( C_{ds1} \) of the switch S1 is removed from the circuit because it is short-circuited by the conducting switch S1. For simplicity, the two transistors Q1 and Q2 in Fig. 4-1 are replaced by the two variable resistors \( R_{Q1} \) and \( R_{Q2} \) in Fig. 4-2, and the two base resistors \( R_{b1}, R_{b2} \) and the controlling voltage \( V_c \) are removed from the circuit because their function is only to control the resistances of \( R_{Q1} \) and \( R_{Q2} \).
Chapter 4: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Gate Side DC Voltage Control

Fig. 4-3. The equivalent circuit when D1 is open and D2 is short-circuited.

Fig. 4-3 shows the equivalent circuit of the one as shown in Fig. 4-2 further simplified when the diode D1 is off and the diode D2 is on, from which it can be seen that the parasitic capacitors are in parallel with the inductor L of the resonant tank. As a result, the parasitic capacitors and the inductor constitute a resonant tank, which is why the common fixed value capacitor of the resonant tank can be replaced by the parasitic capacitors. Assume that the capacitance of $C_{gd1}$ and $C_{ds1}$ in parallel is $C_1'$ and replace $C_{gd1}$ and $C_{ds1}$ with $C_1'$, the part of the circuit consisting of $C_1$, D1, $C_{gd1}$ and $C_{ds1}$ in Fig. 4-2 can be transformed into the one as shown in Fig. 4-4. The three components $C_1$, $C_1'$ and D1 constitute a Voltage Controlled Variable Capacitor Structure (VCVCS). Its equivalent capacitance can be controlled by adjusting the voltage on the anode of the diode D1 through an external circuit. It will be proved by simulation in the next section that there is a fixed relationship between the peak voltage at the anode of the diode D1 and the equivalent capacitances of the VCVCS.

Fig. 4-4. The equivalent circuit when $C_{gd1}$ and $C_{ds1}$ are replaced by $C_2$.

The circuit shown in Fig. 4-4 is the essence of the whole complex circuit shown in Fig. 4-2 in the sense that the circuit shown in Fig. 4-4 reveals the fundamental reason why the capacitance of the circuit shown in Fig. 4-2 changes with the controlling voltage. The situation when the switch S1 is open and S2 closed is similar to that when the switch S1 is closed and S2 open.
4.4 Simulation Study

Simulation study using the software LTSpice is carried out with the circuit as shown in Fig. 4-1. The components and parameters of the circuit used in the simulation are shown in Table 4-1.

<table>
<thead>
<tr>
<th>( V_{\text{DC}} ) (V)</th>
<th>L1, L2 (mH)</th>
<th>L (uH)</th>
<th>D1, D2</th>
<th>S1, S2</th>
<th>Q1, Q2</th>
<th>( R_{b1}, R_{b2} ) (kΩ)</th>
<th>( V_c ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1</td>
<td>10</td>
<td>MBRS360</td>
<td>IRFP240</td>
<td>BC547B</td>
<td>10</td>
<td>4–40</td>
</tr>
</tbody>
</table>

Table 4-1. The parameters of the components used in the simulation.

Fig. 4-5 shows the simulation relationship between the frequency of the converter “\( f \)” and the control voltage “\( V_c \)”, from which it can be seen that they are inversely related to each other, i.e. the higher the control voltage is, the lower the frequency. This is because the equivalent capacitance of the circuit “\( C_e \)” is directly proportional to the control voltage, which is shown in Fig. 4-5 too.

![f & C_e vs. Vc](image)

The proportional relationship between the equivalent capacitance of the circuit and the control voltage \( V_c \) is because the higher \( V_c \) is, the smaller the equivalent resistance of the two transistors Q1 and Q2, and the smaller the equivalent resistance of Q1 and Q2 is, the higher the gate voltage of the two switches S1 and S2. The higher the gate voltages is, the longer the two diodes D1 and D2 conduct, and the longer the two diodes conduct, the larger the equivalent capacitance is. This is because when the diode conducts, the capacitors which are in parallel with the diode are short-circuited and only those in serial with the diodes are left in
the circuit. As the capacitance of two capacitors in series is smaller than either of them, the capacitance of the circuit when the diode conducts is larger than when the diode is off.

Fig. 4-6 shows the simulation relationship between the peak gate voltage and the control voltage \( V_c \), from which it can be seen that as expected the higher the control voltage \( V_c \) is, the higher the peak gate voltage because the higher the control voltage is, the smaller the equivalent resistance of the two transistors Q1 and Q2 is, and the smaller the equivalent resistance of the two transistors, the bigger the voltage of the resonant tank influences the voltage of the gates of the two switches.

![Fig. 4-6. Simulation result of the relationship between the peak gate voltage and the control voltage \( V_c \).](image)

Fig. 4-7 shows the relationship between the peak gate voltage \( V_{gate} \) and the equivalent capacitance \( C_e \), from which it can be seen that as expected the higher the peak gate voltage, the larger the equivalent capacitance because the higher the peak gate voltage is, the longer...
the diodes conduct, and as explained above the equivalent capacitance of the circuit is larger when the diodes conduct longer. The relationship between the peak gate voltage and the conduction period of the diodes $T_{con}$ is shown in Fig. 4-7 too, from which it can be seen that as expected the higher the peak gate voltage is, the longer the diodes conduct.

![Graph showing the relationship between frequency vs. peak gate voltage](attachment:image1.png)

**Fig. 4-8.** The coincidence of the relationship between the frequency of the converter and the peak gate voltage when $R_{b1}=R_{b2}=10k\Omega$ and $R_{b1}=R_{b2}=100k\Omega$, respectively.

![Graph showing the relationship between equivalent capacitance vs. peak gate voltage](attachment:image2.png)

**Fig. 4-9.** The coincidence of the relationship between the equivalent capacitance of the converter and the peak gate voltage when $R_{b1}=R_{b2}=10k\Omega$ and $R_{b1}=R_{b2}=100k\Omega$, respectively.

A comparison simulation is carried out to prove that there is indeed a fixed relationship between the equivalent capacitance of the circuit and the gate voltage. For the comparison, two simulations with different circuit parameters are conducted. One is with the values of the two resistors $R_{b1}$ and $R_{b2}$ (refer to Fig. 4-1) to be $10k\Omega$. The other is with the values of the two resistors to be $100k\Omega$. The frequency of the converter and the peak gate voltages are measured when the controlling voltage $V_c$ changes. As can be expected, the relationship between the controlling voltage $V_c$ and the frequency of the circuit, and the relationship...
between the controlling voltage $V_c$ and the peak gate voltage of the switches, are very different in these two situations. However, the relationship between the frequency of the converter and the peak gate voltage and the relationship between the equivalent capacitance of the circuit and the peak gate voltage got from these two simulations almost completely coincide with each other as shown in Fig. 4-8 and Fig. 4-9, respectively.

The coincidence of the two curves indicates that although noncritical parameters of the circuit such as the two resistors $R_{b1}$ and $R_{b2}$ are quite different, as long as the diodes and switches used are the same, the relationship between the peak gate voltage and the equivalent capacitance, and the relationship between the peak gate voltage and the frequency of the converter remain unchanged. This is because the parasitic capacitors of the diodes and switches which constitute the equivalent capacitance of the VCVCS are the same, and as long as the equivalent capacitance of the VCVCS remains the same, the frequency of the circuit should remain the same also. In conclusion, there is indeed a fixed relationship between the peak gate voltage and the equivalent capacitance of the circuit, and therefore a fixed relationship between the peak gate voltage and the frequency of the converter. The frequency of the converter can be controlled by the controlling voltage $V_c$ through controlling the peak gate voltages of the two switches.

### 4.5 Theoretical Modelling

According to different combinations of the on and off states of the two switches S1 and S2 and the two diodes D1 and D2, the instant and equivalent capacitances of the circuit as shown in Fig. 4-1 are different. The situation is very complex. Section 4.5.1 makes an analysis of these different combinations of the on-off states of S1, S2, D1, D2, and gives the instant capacitance of each state. Section 4.5.2 provides a simplified approximate mathematical model for the relationship between the equivalent capacitance of the circuit and the on-resistances of Q1 and Q2.

#### 4.5.1 The Instant Capacitances When S1 is Closed and S2 Open

Fig. 4-2 shows the equivalent circuit when the switch S1 is closed and S2 open. According to the combinations of the conduction states of the two diodes D1 and D2, the states of the circuit can be divided further into the following four cases:

- Case 1: D1 conducts and D2 open.
Case 2: D2 conducts and D1 open.
Case 3: both of D1 and D2 open.
Case 4: both of D1 and D2 conduct.

The equivalent circuits of the four cases and the relevant instant capacitances when the two resistance branches of $R_{Q1}$ and $R_{Q2}$ are neglected assuming that the values of the resistances are far bigger than the values of the capacitances so that the currents in these two resistance branches are far smaller than those in the branches of the capacitors, and therefore the influence of the resistors to the capacitances of the circuit can be ignored.

According to Fig. 4-10, the instant capacitance of the circuit of Case 1, i.e. when the diode D1 conducts and D2 open, can be calculated as:

$$C_{case1} = C_{gd1} + C_{gs1} + C_{ds2} + \frac{C_{gd2}(C_{gs2} + C_2)}{C_{gd2} + C_{gs2} + C_2}$$

According to Fig. 4-11, the instant capacitance of the circuit of Case 2, i.e. when the diode D2 conducts and D1 open, can be calculated as:
Chapter 4: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Gate Side DC Voltage Control

\[ C_{\text{case2}} = C_{ds2} + C_{gd2} + \frac{C_1(C_{gd1} + C_{gs1})}{C_{gd1} + C_{gs1} + C_1} \quad (4-2) \]

Fig. 4-12. The equivalent circuit of Case 3- both D1 and D2 open.

According to Fig. 4-12, the instant capacitance of the circuit of Case 3, i.e. when both D1 and D2 open, can be calculated as:

\[ C_{\text{case3}} = C_{ds2} + \frac{C_1(C_{gd1} + C_{gs1})}{C_{gd1} + C_{gs1} + C_1} + \frac{C_{gd2}(C_{gs2} + C_2)}{C_{gd2} + C_{gs2} + C_2} \quad (4-3) \]

Fig. 4-13. The equivalent circuit of Case 4- both D1 and D2 conduct.

According to Fig. 4-13, the instant capacitance of the circuit of Case 4, i.e. when both D1 and D2 conduct, can be calculated as:

\[ C_{\text{case4}} = C_{gd1} + C_{gs1} + C_{ds2} + C_{gd2} \quad (4-4) \]

In fact, the condition of Case 4 does not happen in the real circuit, i.e. the two diodes D1 and D2 never conduct at the same time.

According to the value of the equivalent capacitance of the two transistors Q1 and Q2, the different conduction situation and combinations of D1 and D2 during the period S1 is closed and S2 open are shown in Fig. 4-14, Fig. 4-15 and Fig. 4-16, respectively.
Chapter 4: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Gate Side DC Voltage Control

Fig. 4-14. D1 and D2 conduct during both the period S1 is closed and open.

Fig. 4-14 shows the situation that the diode D2 closes before the switch S1 close and opens before S1 opens, and the diode D1 closes before S1 opens and opens after S1 opens, where (a) shows the voltage at the point B (refer to Fig. 4-1 and Fig. 4-2), (b) shows the conduction period of the diode D2 and (c) the conduction period of the diode D1. The switch S1 closes (S2 opens accordingly) during the period $V_B$ is at its positive half cycle.

Fig. 4-15. D1 and D2 close at exactly the moments S1 opens and closes respectively.

Fig. 4-15 shows the situation that the two diodes D1 and D2 close at exactly the moments the switch S1 opens and closes, respectively, and open before the moments the switch S1 closes and opens again.

Fig. 4-16 shows the situation that the two diodes D1 and D2 close during the periods of the switch S1 open and close respectively. The situation when S1 is open and S2 closed is completely symmetrical and similar to that when S1 is closed and S2 open.
One general principle is that the instant capacitance of the circuit changes when the state of any one of the four components S1, S2, D1 and D2 changes.

### 4.5.2 A Simplified Mathematical Model

It can be seen from the above analysis that the situation of the parasitic capacitances is very complex. The instant capacitance of the circuit changes whenever any of the states of the four components S1, S2, D1 and D2 change. To find the exact relationship between the overall equivalent capacitance of the circuit and the control voltage $V_c$, the relationship between the control voltage and the exact moments the two diodes D1 and D2 begin and stop to conduct need to be found first. After that, the overall equivalent capacitance of the circuit needs to be calculated based on the instant capacitances of the circuit in different combinations of the conduction states of the four components S1, S2, D1 and D2. To make matters worse, the combinations of the conduction states of the four components S1, S2, D1 and D2 are not fixed but change with the controlling voltage $V_c$ or the equivalent resistance of the two transistors Q1 and Q2, which makes the situation much more complex. In view of the difficulty in getting an accurate mathematical model for the relationship between the equivalent capacitance of the circuit and the controlling voltage, this section presents a simplified mathematical model based on mainly two assumptions.

Firstly, it is assumed that during the positive half cycle of the voltage at the point A (refer to Fig. 4-1), the diode D1 is always on and the diode D2 is always off, and during the negative half cycle of the voltage at the point A (the positive half cycle of the voltage at the point B accordingly), the diode D1 is always off and the diode D2 is always on as shown in Fig. 4-17,
which is similar to the real circuit situation (refer to Fig. 4-5) and makes the theoretical analysis much simplified.

Secondly, the mature steady state analysis method is used to approximate the transient frequency of the circuit, which also makes the analysis of the circuit much simplified. Although it is not one hundred percent accurate, it can be proved by simulation that the error is small. The simulation is carried out with the circuit as shown in Fig. 4-18.

The purpose is to find out the difference between the transient and steady state responses when the capacitor of the resonant tank of the push pull converter changes between two distinctly different values $C_L$, and $C_L$ and $C_R$ in parallel abruptly. The parameters of the components used in the simulation are shown in Table 4-2, where $R_L$ means the equivalent resistance of the inductor $L$. 

![Fig. 4-17. The waveforms of $V_A$, $V_B$, $T_{D1}$ and $T_{D2}$.](image1)

![Fig. 4-18. The circuit used in the simulation to prove that there is not much difference between the frequencies of the transient and steady state responses.](image2)
Table 4-2. The parameters of the components used in the simulation.

<table>
<thead>
<tr>
<th>V_{DC} (V)</th>
<th>L1, L2 (mH)</th>
<th>C1, C2 (nF)</th>
<th>D1, D2</th>
<th>S1, S2</th>
<th>L (μH)</th>
<th>R_L (Ω)</th>
<th>C_L (nF)</th>
<th>C_R (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>34</td>
<td>1</td>
<td>2.5</td>
<td>1N4148</td>
<td>IRFP240</td>
<td>100</td>
<td>10</td>
<td>300</td>
<td>150</td>
</tr>
</tbody>
</table>

The results are shown in Fig. 4-19 to Fig. 4-23, where the green waveforms on the top are the voltages of the resonant tank while the red ones at the bottom are the driving signal for the switch S_R, which changes the capacitance of the resonant tank between C_L and C_L and C_R in parallel.

It can be seen from Fig. 4-19 that the difference of the amplitude of the resonant tank voltage between the steady and transient periods are relatively larger.

From Fig. 4-20 and Fig. 4-21, it can be seen that the frequency changes instantly instead of gradually at the moments the capacitor of the resonant tank changes abruptly, which means
that there is not much difference between the frequency of the transient state and the frequency of the steady state so that the frequency calculated in steady state can be used to approximate the frequency of the transient state.

Fig. 4-22. The zoomed-in view of the high-frequency period.

![Resonant Voltage and Switching Signal](image1)

Fig. 4-23. The zoomed-in view of the low frequency period.

![Resonant Voltage and Switching Signal](image2)

It can be seen further from the zoomed-in views in Fig. 4-22 and Fig. 4-23 that the frequency does not change much between the transient and steady states. In conclusion, the steady state frequency can be used to approximate the transient state frequency without much error.

Generally, it is no correct to use steady state response replace transient state response, for example there is a big difference between the steady state and the transient state responses of the amplitude. There is no way to substitute the transient amplitude response with the steady state amplitude response. However, in some special cases such as the frequency response, there is not much difference between the transient and the steady responses so that the steady frequency response can be used to approximate the transient frequency response. Moreover, the major task here is not to find out the exact frequency but how other parameters of the circuit influence the frequency. If the parameter of the circuit such as the control voltage $V_c$ as shown in Fig. 4-1 influences the steady state frequency in one way, it will influence the transient frequency in the same way. For example, if the steady state frequency increases with the increase of the control voltage $V_c$, the transient state frequency should also increase with the increase of the control voltage $V_c$. As a result, for simplicity, the steady state response of the frequency calculated through the concept of the input admittance of the circuit will be
used to approximate the transient state response of the frequency to find out the relationship between the frequency of the converter and the equivalent resistance of the two control transistors Q1 and Q2.

![Diagram](image)

**Fig. 4-24. The strategy to derive the approximate equivalent capacitance through the concept of input admittance.**

Based on the above two assumptions, the equivalent circuit when the switch S1 is closed and S2 open is shown in Fig. 4-24 (a). The waveforms of the voltages of the resonant tank and the conduction states of the two diodes D1 and D2 during this period, i.e. when the voltage at the point B (refer to Fig. 4-1) is on its positive half cycle, can be seen from Fig. 4-17.

The final purpose of the theoretical analysis is to find out the relationship between the frequency of the converter and the control voltage $V_c$. However, as shown in Fig. 4-8 and Fig. 4-9, the most basic and essential relationship which remain unchanged in spite of the change of noncritical circuit parameters such as the two resistors $R_{b1}$ and $R_{b2}$, or the type of the transistors used, is the relationship between the frequency or equivalent capacitance of the converter and the peak gate voltage. Nevertheless, the parameter which has a direct influence on the peak gate voltage is the equivalent on-resistance of the two transistors Q1 and Q2 instead of the control voltage $V_c$. Because as can be expected, the relationship between the peak gate voltage and the control voltage $V_c$ varies with the variation of the two base resistors $R_{b1}$ and $R_{b2}$. In fact, the relationship between the control voltage $V_c$ and the on-resistance of the two transistors Q1 and Q2 also depends upon the type of transistors used. This relationship is complex and nonessential. As a result, the emphasis of the theoretical analysis is placed on finding out the relationship between the equivalent capacitance of the circuit and the on-resistance of the two transistors Q1 and Q2 instead of the frequency of the circuit and the control voltage $V_c$. Once the relationship between the equivalent capacitance of the circuit and the on-resistance of the two transistors Q1 and Q2 is derived out, it is easy to find
Chapter 4: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Gate Side DC Voltage Control

the relationship between the frequency of the converter and the on-resistance of the two transistors Q1 and Q2.

In fact, there are many different kinds of frequencies for the push pull converter such as the Zero Phase Angle Resonant Frequency \((f_r)\), the Maximum Inductor Current Frequency \((f_{ilm})\), the Maximum Capacitor Voltage Frequency \((f_{vc})\) and ZVS Frequency \((f_{ZVS})\) [2], etc. They are very complex but all converge to the undamped Natural Oscillation Frequency \((f_f)\) when \(Q\) is large. The real operating frequency of the autonomous push pull converter is the last one, i.e. the ZVS Frequency \((f_{ZVS})\). Strictly speaking, the frequency adjusted by any parameter of the circuit can only be the real ZVS frequency, but in the theoretical analysis, the Natural Oscillation Frequency \((f_f)\) is used for simplicity because the real ZVS frequency of the converter is too complex to be expressed with an analytical formula. Moreover, the point of the theoretical analysis here is not to make an accurate differentiation of different kinds of frequencies, but to concentrate on how generally these frequencies are influenced by another circuit parameter. If the circuit parameter such as the control voltage \(V_c\) influences one frequency in one way, it will influence other frequencies in a similar way. In short, the natural oscillation frequency \((f_f)\) expressed by (4-5) will be used in the theoretical analysis.

\[
\omega = \frac{1}{\sqrt{LC}}
\]  

(4-5)

where \(L\) represents the inductance and \(C\) the equivalent capacitance of the resonant tank, respectively.

Assume that the capacitance of the part of the circuit as shown in the dashed box of Fig. 4-24 (a) is equivalent to the capacitance of the capacitor \(C_e\) as shown in Fig. 4-24 (b), then the natural oscillation frequency of the circuit as shown in Fig. 4-24 (a) should be equal to the natural oscillation frequency of the circuit as shown in Fig. 4-24 (b). The natural oscillation frequency of the circuit as shown in Fig. 4-24 (b) can be found through formula (3-5), while the natural oscillation frequency of the circuit as shown in Fig. 4-24 (a) can be found by calculating the input admittance of the circuit. The imaginary part of the input admittance of the circuit should be zero when the circuit resonates at its natural oscillation frequency because the circuit should be purely resistive in this state.

The input admittance \(Y_{in}\) of the circuit as shown in Fig. 4-24 (a) is expressed by (4-6).
\[ Y_{in} = \frac{-\omega L k_4 + j \left[ -Lk_2(k_2k_3 + C_1k_1)\omega^4 + \left( k_2^2 - \frac{L(k_3 + k_1)}{R_1^2} \right)\omega^2 + \frac{1}{R_1^2} \right]}{-\omega L \left( \frac{1}{R_1^2} + \omega^2 k_2^2 \right)} \]  

(4-6)

where:

\[ k_1 = C_{gd1} + C_{gs1} \]

\[ k_2 = C_{gd1} + C_{gs1} + C_1 \]

\[ k_3 = C_{ds2} + C_{gd2} \]

\[ k_4 = \frac{\omega^2 (C_{gd1} + C_{gs1})(C_{gd1} + C_{gs1} + C_1) - \omega^2 c_1 (C_{gd1} + C_{gs1})}{R_1} \]

When the circuit resonates at the natural oscillation frequency \( f_0 \), the imaginary part of \( Y_{in} \) should be zero, i.e.:

\[ -Lk_2(k_2k_3 + C_1k_1)\omega^4 + \left( k_2^2 - \frac{L(k_3 + k_1)}{R_1^2} \right)\omega^2 + \frac{1}{R_1^2} = 0 \]  

(4-7)

Resolving (4-7), gives the resonant frequency \( \omega_0 \) of the circuit shown in Fig. 4-24 (a):

\[ \omega_0^2 = \frac{-k_2^2 + \frac{L(k_3 + k_1)}{R_1^2} - \sqrt{\left[ k_2^2 - \frac{L(k_3 + k_1)}{R_1^2} \right]^2 + 4 \frac{Lk_2(k_2k_3 + C_1k_1)}{R_1^2}}}{-2Lk_2(k_2k_3 + C_1k_1)} \]  

(4-8)

As having been assumed, if the capacitance of the part of the circuit as shown in the dashed box of Fig. 4-24 (a) is equivalent to the capacitance of the capacitor \( C_e \) as shown in Fig. 4-24 (b), the natural oscillation frequency of the circuit as shown in Fig. 4-24 (b) should also be \( \omega_0 \). Substituting \( \omega_0 \) into (4-5), the equivalent capacitance \( C_e \) can be derived as:

\[ C_e = \frac{1}{L \cdot \omega_0^2} \]  

(4-9)

Substituting (4-8) into (4-9) gives:
Chapter 4: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Gate Side DC Voltage Control

\[ C_e = \frac{2Lk_2(k_2k_3 + C_1k_1)}{L \cdot \left[ k_2^2 - \frac{L(k_3+k_1)}{R_1^2} + \sqrt{\left[ k_2^2 - \frac{L(k_3+k_1)}{R_1^2} \right]^2 + 4 \frac{Lk_2(k_2k_3+C_1k_1)}{R_1^2}} \right]} \]  

(4-10)

Formula (4-10) gives the relationship between the equivalent capacitance \( C_e \) of the circuit shown in Fig. 4-24 (a) and the resistance of the variable resistor \( R_1 \).

Substituting (4-10) into formula:

\[ f_e = \frac{1}{2\pi \sqrt{L C_e}} \]

(4-11)

The above analysis is about the situation when \( S_1 \) is closed and \( S_2 \) open. The situation when \( S_2 \) is closed and \( S_1 \) open is similar due to symmetry. Formula (4-12) and (4-13) express the relationship between \( C_e \) and \( R_2 \), and \( f_e \) and \( R_2 \) respectively when \( S_2 \) is closed and \( S_1 \) open, where \( R_2 \) is the equivalent on-resistance of the transistor \( Q_2 \).

\[ C_e = \frac{2Lk_2'(k_2'k_3' + C_{2}k_1')}{L \cdot \left[ k_2'^2 - \frac{L(k_3'+k_1')}{R_2^2} + \sqrt{\left[ k_2'^2 - \frac{L(k_3'+k_1')}{R_2^2} \right]^2 + 4 \frac{Lk_2'(k_2'k_3'+C_{2}k_{1}'k_1')}{R_2^2}} \right]} \]  

(4-12)

\[ f_e = \frac{\sqrt{k_2'^2 - \frac{L(k_3'+k_1')}{R_2^2} + \sqrt{\left[ k_2'^2 - \frac{L(k_3'+k_1')}{R_2^2} \right]^2 + 4 \frac{Lk_2'(k_2'k_3'+C_{2}k_{1}'k_1')}{R_2^2}}}{2\pi \sqrt{Lk_2'(k_2'k_3'+C_{2}k_{1}'k_1')}} \]  

(4-13)

where: \( k_1' = C_{gd2} + C_{gs2}, k_2' = C_{gd2} + C_{gs2} + C_2, k_3' = C_{ds1} + C_{gd1} \)

Fig. 4-25 and Fig. 4-26 show the theoretical relationship between \( C_e \) and \( R_1 \), and that between \( f_e \) and \( R_1 \) when substituting the real circuit parameters and parasitic capacitance values as shown in Table 4-3 into (4-10) and (4-11), respectively.

**Table 4-3. Parameters used in theoretical calculation.**

<table>
<thead>
<tr>
<th>L (uH)</th>
<th>C1 (nF)</th>
<th>Cgd1 (nF)</th>
<th>Cgs1 (nF)</th>
<th>Cds2 (nF)</th>
<th>Cgd2 (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3.3</td>
<td>1.33</td>
<td>1.25</td>
<td>0.3</td>
<td>0.1</td>
</tr>
</tbody>
</table>
For comparison, simulation is carried out with the two transistors Q1 and Q2 in the circuit as shown in Fig. 4-1 replaced by two resistors R1 and R2, respectively, and the two base resistors Rb1, Rb2 and the control voltage $V_c$ deleted. The main circuit parameters and components used in the simulation is shown in Table 4-4.

<table>
<thead>
<tr>
<th>C1, C2 (nF)</th>
<th>L (uH)</th>
<th>L1, L2 (mH)</th>
<th>D1, D2</th>
<th>S1, S2</th>
<th>VDC (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>1</td>
<td>1</td>
<td>1N4148</td>
<td>IRFP240</td>
<td>10</td>
</tr>
</tbody>
</table>

The simulation results and those got from (4-10) and (4-11) for the relationship between the equivalent capacitance $C_e$ of the circuit and the equivalent resistance $R_c$ of the transistors, and the relationship between the equivalent frequency $f_e$ and $R_c$ are shown in Fig. 4-25 and Fig. 4-26, respectively, from which it can be see that they agree with each other roughly well.

![Fig. 4-25. The relationship curve between $C_e$ and $R_c$ got from formula (4-10) and simulation.](image1)

![Fig. 4-26. The relationship curve between $f_e$ and $R_c$ got from formula (4-11) and simulation.](image2)
The main reason for the inconsistency between the results of the simulation and theoretical analysis is that the on and off of the two diodes D1 and D2 is not exactly in consistent with the on and off the two switches S1 and S2 as shown in Fig. 4-17, but as shown in Fig. 4-14 to Fig. 4-16, etc. In other words, $T_{D1}$ and $T_{D2}$ (the conduction periods of the two diodes D1 and D2) are influenced by the value of the resistance of the two variable resistors R1 and R2. It is only an approximation and simplification to assume that when S1 is on and S2 is off, D1 will be off and D2 on, and vice versa as shown in Fig. 4-17. Besides, there are also other factors such as the diodes and the switches are assumed to be ideal in the theoretical analysis but they are not in simulation, and the values of the parasitic capacitances especially $C_{gd1}$ and $C_{gd2}$ are fixed in the theoretical calculation, however, they vary greatly in simulation and real circuit operation.

### 4.6 Experimental Study

Practical circuit experiments are carried out with the circuit as shown in Fig. 4-1. The components and parameters used in the experiments are shown in Table 4-5.

**Table 4-5. The devices and parameters used in the experiment.**

<table>
<thead>
<tr>
<th>V$_{DC}$ (V)</th>
<th>L1, L2 (mH)</th>
<th>L (μH)</th>
<th>C1, C2 (nF)</th>
<th>D1, D2</th>
<th>S1, S2</th>
<th>Q1, Q2</th>
<th>R1, R2 (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1</td>
<td>2.47</td>
<td>2.2</td>
<td>BYV26</td>
<td>FDS86106</td>
<td>BC547B</td>
<td>180kΩ</td>
</tr>
</tbody>
</table>

![Fig. 4-27. Experimental relationship between the controlling voltage $V_c$ and the frequency of the converter.](image)

Fig. 4-27 shows the experimental relationship between the controlling voltage $V_c$ and the frequency of the converter, which agrees with the simulation result as shown in Fig. 4-5 in that the frequency is inversely related to the controlling voltage. The difference in the
frequency range is because that the power MOSFET switches used in simulation and real circuit experiments are different. IRFP240 is used in simulation while FDS86106 is used in real circuit experiment. As the parasitic capacitances of FDS86106 are much smaller than those of IRFP240, the frequency of practical circuit experiment is much higher than that of simulation.

**Fig. 4-28. Experimental relationship between the control voltage Vc and the peak gate voltage.**

Fig. 4-28 shows the practical experimental relationship between the controlling voltage Vc and the peak gate voltage, from which it can be seen that they are directly proportional to each other because the higher the control voltage Vc is, the lower the resistance of the two transistors Q1 and Q2, and the lower the resistance of Q1 and Q2 is, the higher the gate voltage.

**Fig. 4-29. Experimental relationship between the peak gate voltage and the calculated parasitic capacitor of the circuit.**
Fig. 4-29 shows the experimental relationship between the peak gate voltage and the equivalent parasitic capacitance of the circuit, from which it can be seen that as expected the higher the peak gate voltage, the larger the equivalent parasitic capacitance because the higher the peak gate voltage, the longer the diodes conduct. The equivalent capacitance of the circuit is calculated from the measured frequency of the converter.

Fig. 4-30 is some experimental waveforms which show how the frequency changes with the control voltage $V_c$. 
Fig. 4-30. Practical circuit experimental waveforms of the controlling voltage $V_c$ (green at the bottom) and the voltage of the resonant tank (yellow on the top) showing the frequency of the converter.

As can be seen, the higher the control voltage $V_c$ is, the lower the frequency, specifically, when the controlling voltage $V_c$ increases roughly from 2V to 25V, the frequency declines from about 9 MHz to 6.14 MHz. The green curve at the bottom is the control voltage $V_c$ and the yellow one on the top is the voltage on one side of the resonant tank showing the frequency of the converter. The frequency of the converter is shown in the bottom-left corner of each plot. They are 9.009MHz, 7.04MHz, 6.62MHz and 6.14MHz, respectively from the first to the fourth plot. The average control voltage is shown in the bottom-right corner of
each plot. They are 2.03V, 10.02V, 15.03V and 25.09V, respectively from the first to the fourth plot.

Fig. 4-31 are some experimental waveforms showing how the peak gate voltage changes with the control voltage $V_c$, from which it can also be seen the proportional relationship between the two as shown in Fig. 4-28, i.e. the higher the control voltage $V_c$ is, the higher the peak gate voltage. Besides, the inverse relationship between the control voltage $V_c$ and the frequency of the gate voltage which is the same as the frequency of the converter can also be seen from Fig. 4-28, specifically when the control voltage $V_c$ increases roughly from 0V to 19V, the frequency declines from about 10MHz to 6.5MHz. The green curve at the bottom is the control voltage $V_c$ and the yellow one on the top is the gate voltage.
Chapter 4: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Gate Side DC Voltage Control

Fig. 4-31. Experimental waveforms of the controlling voltage $V_c$ (green, bottom) and the gate voltage (yellow, top).

The frequency of the gate voltage is shown in the bottom-left corner of each plot. They are 10.309MHz, 7.46MHz, 7.04MHz and 6.49MHz, respectively, from the first to the fourth plot. The peak gate voltage is shown in the second place at the same line as the frequency. They are 2.8V, 9.4V, 12.7V and 18.9V, respectively, from the first to the fourth plot. The average control voltage is shown in the third place at the same line as the frequency. They are 490mV, 5.02V, 10.04V and 18.97V respectively from the first to the fourth plot.

4.7 Other Methods to Adjust the Gate Voltage

In fact, the essence of the method proposed in this chapter is to adjust the average equivalent parasitic capacitance and therefore the frequency of the autonomous push pull converter.
through regulating the gate voltages of the two switches. Therefore, whatever the method is, as long as it can vary the voltage on the gates of the two switches, it can adjust the equivalent capacitance and therefore the frequency of the converter. Fig. 4-1 shows just one method to realize this goal. There are still other approaches. This section introduces two of them.

Fig. 4-32. The first alternative way to control the voltage on the gates of the two switches S1 and S2.  

Fig. 4-32 shows one alternative to adjust the voltage on the gates of the two switches of the autonomous push pull converter. Compared to the one shown in Fig. 4-1, the circuit structure of this method is simpler because the two transistors Q1 and Q2 as shown in Fig. 4-1 are deleted. However, one disadvantage of this method is that when the values of the two resistors R1 and R2 are small, power losses on them will be high because a big current will flow through them when the corresponding diodes conduct. The red-coloured dashed arrow lines in Fig. 4-32 shows the current flowing through the resistor R1 directly to the ground when the switch S2 is closed and S1 open and the diode D1 is conducting. The situation can be improved by using bigger value resistances. However, the bigger the resistances of R1 and R2, the smaller the influence of the control voltage Vc to the gate voltages.

Fig. 4-33 shows another example to adjust the voltage on the gates of the two switches of the autonomous push pull converter. It uses two programmable precision voltage references TL431 (T1 and T2) so that the peak gate voltage can be made very stable when the control voltage Vc remains unchanged. By adjusting the equivalent resistance of the two transistors Q1 and Q2 through the control voltage Vc, the output voltage of the two programmable precision voltage references TL431 at the gates of the two switches S1 and S2 can be adjusted between 2.5V~36V.
Fig. 4-33. The second alternative way to control the voltage on the gates of the two switches S1 and S2.

4.8 Summary

This chapter proposed a method to control the average equivalent parasitic capacitances of a high-frequency autonomous push pull converter simply with a DC voltage so that the frequency of this high-frequency autonomous push pull converter can be adjusted and controlled with this DC voltage. The reason for this was analysed in details with equivalent circuit analysis. It was found that the structure as shown in Fig. 4-4 is in fact the essence why the parasitic capacitances and frequency of the autonomous push pull converter can be controlled by a DC voltage. It was based on this observation that the two most important findings of this research – the Resistor-controlled DCVC and the Transistor-controlled DCVC, were made which will be presented in details in the following chapters 5 and 6.
Chapter 5: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Resistor-controlled DCVC

5.1 Introduction

As mentioned in Section 2.2 of Chapter 2, there are three methods to improve the loosely coupled nature of an IPT system to increase the power transfer ability and efficiency, i.e.:

- Increasing the frequency of the magnetic field
- Improving the coupling degree between the primary and secondary coil
- Making use of the principle of resonance.

High-frequency operations of different types of resonant power converters were investigated in Chapter 3, which showed high-frequency autonomous push pull converter operation can be realized by utilizing the parasitic capacitances of the circuit. Chapter 4 proposed a method to vary the equivalent capacitances by taking the parasitic capacitances into consideration, thereby to adjust the frequency of this high-frequency autonomous push pull converter with a DC voltage. However, this method is limited to the gate side control of the push pull resonant converter. Based on the work presented in Chapter 4, Chapter 5 and 6 will introduce DC-voltage Controlled Variable Capacitors (DCVC) which can be used in normal resonant circuits of IPT systems for ZVS frequency variation or stabilization.

One method for adjusting the operating frequency but still maintaining the resonant operation of an IPT system is to adjust the switching frequency of the converter to match the resonant or ZVS frequency of the system as in the autonomous push pull converter which follows the resonant or ZVS frequency of the system automatically. The other is to adjust the resonant or ZVS frequency of the system dynamically to match the fixed switching or gate driving
Chapter 5: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Resistor-controlled DCVC

Traditionally, this is realized through switching mode capacitors [103-106, 186-202] or inductors [203-218]. PWM signals instead of a DC voltage are used for their control, and the active switches in them may need gate drivers and a separate voltage source. This makes the circuit complex and sometimes inconvenient, for example when used in the secondary side of an IPT system where an auxiliary power supply is not readily available. Furthermore, at high frequencies it is difficult for switch mode circuits to be accurately soft-switched due to practical detection delays, component accuracies, etc. In addition the circuit structure of switch mode capacitors and inductors may become very complex when soft-switching is considered, otherwise the switching loss and EMI will be high, or more importantly, the normal operation of the main circuit may be seriously influenced.

This chapter proposes a new method to adjust the resonant or ZVS frequency of autonomous push pull converters through a Resistor-controlled DCVC (R-DCVC). The equivalent capacitance of this R-DCVC can be controlled simply with a DC voltage, which influences the conduction period of a diode. The conduction of the diode short-circuits a capacitor in parallel with the diode, so that the overall equivalent capacitance of the R-DCVC changes. Compared to traditional switch mode capacitors, the circuit structure and control strategy of the R-DCVC is much simpler because no active switches are needed in the circuit, and therefore the EMI is low. Additionally the R-DCVC has the potential to be used in much higher frequency applications because of the smooth control of the equivalent capacitance with a DC voltage instead of PWM signal. This chapter is structured as follows. The basic operating principle of the proposed method is explained in Section 5.2. Section 5.3 presents the theoretical modelling of the R-DCVC. Sections 5.4 and 5.5 provide the simulation and practical experimental results, respectively. Finally a summary is made in Section 5.6.

5.2 The Proposed Method and Basic Operating Principle

Fig. 5-1 (a) shows the proposed method to control the frequency of the autonomous push pull converter through a DC voltage, from which it can be seen that the normal fixed value capacitor in the resonant tank of the autonomous push pull converter is replaced by the part of the circuit in the dashed box consisting of $C_{up}$, $C_{dw}$, $D_c$ and $R_c$, which form the R-DCVC. The equivalent capacitance $C_e$ of the R-DCVC can be varied by the control voltage $V_c$. The higher $V_c$ is, the larger the equivalent capacitance of the R-DCVC will be and therefore the lower frequency.
the equivalent frequency $f_e$ of the converter. As a result, the equivalent frequency $f_e$ can be controlled by $V_c$.

Fig. 5-1 (a). The proposed R-DCVC applied to the autonomous push pull converter.

The reason why $C_e$ can be varied by $V_c$ is that $V_c$ influences the conduction period $T_{\text{con}}$ of the diode $D_c$. The higher $V_c$ is, the longer the diode conduction period $T_{\text{con}}$ will be, because the higher $V_c$ is, the higher the voltage at the anode of the diode $D_c$ $V_{\text{anod}}$ is, and the higher $V_{\text{anod}}$ is, the longer the diode conducts. When the diode $D_c$ conducts, $C_{\text{up}}$ is short-circuited so that only $C_{\text{dw}}$ functions in the circuit. When $D_c$ does not conduct, $C_{\text{up}}$ is connected back to the circuit again. As the capacitance of $C_{\text{dw}}$ is larger than that of $C_{\text{up}}$ and $C_{\text{dw}}$ in series, the longer the diode conducts, the larger the average equivalent capacitance $C_e$ of the R-DCVC is. In summary, $V_c$ controls the equivalent capacitance $C_e$ of the R-DCVC by varying the conduction period $T_{\text{con}}$ of the diode $D_c$, and it can be deducted that the maximum adjustable range of the equivalent capacitance of the R-DCVC is between the capacitance of $C_{\text{dw}}$ and the capacitance of $C_{\text{up}}$ and $C_{\text{dw}}$ in series as will be proved by (5-21) and (5-22) in Section 5.3.4.

Fig. 5-3 (a) and (b) in Section 5.3 (Theoretical modelling) show the typical waveforms of the voltage at the cathode ($V_{\text{cath}}$) and anode ($V_{\text{anod}}$) of the diode, respectively. Fig. 5-3 (c) shows the conduction period $T_{\text{con}}$ of the diode $D_c$, during which $V_{\text{anod}}$ is bigger than $V_{\text{cath}}$. The position or height of $V_{\text{anod}}$ in the Y-axis ($H_{\text{Vanod}}$) is influenced by the controlling voltage $V_c$. The larger $V_c$ is, the higher $H_{\text{Vanod}}$, and as can be seen from Fig. 5-3, the higher $H_{\text{Vanod}}$ is, the longer the diode conducts. In short, $T_{\text{con}}$ is roughly proportional to $V_c$, which will be verified by the theoretical analysis in Section 5.3.

When the diode $D_c$ in the R-DCVC as shown in Fig. 5-1 (a) conducts only at the positive or negative half cycle of the voltage across the resonant tank, the waveform of the voltage of the
resonant tank will not be balanced. To solve this problem, a balanced version of the R-DCVC as shown in Fig. 5-1 (b) can be adopted, where the two diodes $D_{c1}$ and $D_{c2}$ conduct at the positive and negative half cycle of the voltage of the resonant tank, respectively, so that the waveform of the voltage of the resonant tank will be balanced. For simplicity, analysis of the R-DCVC in this research will focus on the single-side version as shown in Fig. 5-1 (a).

![Fig. 5-1 (b). The double-sided balanced version of R-DCVC applied to the autonomous push pull converter.](image)

### 5.3 Theoretical Modelling

The task of the theoretical analysis of the R-DCVC is to find the relationship between the equivalent capacitance $C_e$ of the R-DCVC and the control voltage $V_c$. For this purpose, the circuit in Fig. 5-1 (a) is simplified as shown in Fig. 5-2.

![Fig. 5-2. The simplified circuit for theoretical analysis of the R-DCVC.](image)

As can be seen, the simplified circuit in Fig. 5-2 includes only $C_{up}$, $C_{dw}$, $D_c$, $R_c$ and $V_c$ of the original circuit as shown in Fig. 5-1 (a) and is driven periodically by positive and negative...
Chapter 5: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Resistor-controlled DCVC

half cycle sinusoidal waves in turn as shown in Fig. 5-2, which being the same case as in the original circuit.

Fig. 5-3 shows the typical waveforms of $v_a$, $v_b$ and the conduction period $T_{con}$ of the diode Dc. The circuit is turned on at $t=0$ and is in the transient process until $t=t_1$. After $t_1$, the circuit goes into steady state. It can be seen from Fig. 5-3 that generally $V_{anod}$ oscillates at a much lower voltage level in steady state than in transient state. This is because that half a cycle later after the power is turned on, i.e. at the point $t_0$ when the circuit is going to change from being driven by the positive half cycle sine wave as shown in Fig. 5-2 (a) to being driven by the negative half cycle sine wave as shown in Fig. 5-2 (b), the diode is on, during which $V_{anod}$ is clamped to roughly being equal to $V_{cath}$, i.e. zero. In short, the conduction of the diode during the transient period clamps $V_{anod}$ to a much lower level which continues in the steady state making $V_{anod}$ become negative mostly. Otherwise, if the diode does not conduct, $V_{anod}$ will be always positive and may be always much higher than $V_{cath}$ because of the influence of the control voltage $V_c$.

![Fig. 5-3. Typical waveforms of the circuit: $V_{cath}$ (a), $V_{anod}$ (b) and the period the diode conducts (c).](image)

The origin of coordinates for the analysis of the steady state of the circuit is chosen at the point of “o” as shown in Fig. 5-3. The relationship between $C_e$ and $V_c$ is determined in three steps. Firstly, the relationship between $T_{con}$ and $V_c$ is found out. Secondly, the relationship between $C_e$ and $T_{con}$ is derived. Finally, the relationship between $C_e$ and $V_c$ is calculated with
the above two relationships. To find out the relationship between $T_{\text{con}}$ and $V_c$, two exact moments, i.e. the moment the diode starts to conduct ($t_{\text{on}}$) and the moment the diode stops to conduct ($t_{\text{off}}$) needs to be determined first. After that, $T_{\text{con}}$ can be calculated with (5-1):

$$T_{\text{con}} = t_{\text{off}} - t_{\text{on}}$$  \hspace{1cm} (5-1)

### 5.3.1 Determination of the Moment When the Diode Stops to Conduct

Fig. 5-4 shows the equivalent circuit when the diode is conducting. $C_{up}$ and $D_c$ are removed because an ideal conducting diode amounts to a short-circuit.

The diode is regarded as stopping to conduct when the current in it $i_s$ drops to zero. $i_s$ is governed by (5-2):

$$i_s = C_{dw} \frac{dV_S}{dt} + \frac{V_C}{R_c}$$  \hspace{1cm} (5-2)

Substituting $V_S = A_s \sin \omega t$ and $i_s = 0$ into (5-2), the moment the diode stops to conduct $t_{\text{off}}$ can be derived as:

$$t_{\text{off}} = \arccos\left(-\frac{V_c}{\omega A_s R_c C_{dw}}\right)$$  \hspace{1cm} (5-3)

### 5.3.2 Determination of the Moment When the Diode Starts to Conduct

Fig. 5-5 shows the equivalent circuit when the diode is not conducting, regarded as an open circuit so that removed from the circuit. The voltage at the anode of the diode $V_{\text{anod}}$ is $V_{\text{Cup}}$ during this period, which is governed by (5-4):
Chapter 5: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Resistor-controlled DCVC

\[
\frac{dV_{C_{\text{up}}}}{dt} + \frac{1}{R_c(C_{\text{up}} + C_{\text{dw}})} \cdot V_{C_{\text{up}}} = \frac{\omega A_s R_c C_{\text{dw}} \cos \omega t + V_C}{R_c(C_{\text{up}} + C_{\text{dw}})}
\]  

(5-4)

![Fig. 5-5. The equivalent circuit when the diode is not conducting.](image)

The solution of (5-4) is:

\[
V_{C_{\text{up}}} = \omega k_1 \cdot \sin \omega t + kk_1 \cdot \cos \omega t + V_C + Ke^{-kt}
\]  

(5-5)

where \( k = \frac{1}{R_c(C_{\text{up}} + C_{\text{dw}})} \), \( k_1 = \frac{\omega A_s C_{\text{dw}}}{(C_{\text{up}} + C_{\text{dw}})(\omega^2 + k^2)} \)

The constant \( K \) in (5-5) can be determined by the initial condition, i.e. the value of \( V_{C_{\text{up}}} \) at the moment of \( t_2 \) as shown in Fig. 5-3. It can be seen from Fig. 5-3 that the moment \( t_2 \) can be expressed by (5-6):

\[
t_2 = t_{\text{off}} - \frac{2\pi}{\omega}
\]  

(5-6)

Substituting (5-3), (5-6) and \( V_{C_{\text{up}}} = 0 \) into (5-5), the constant \( K \) can finally be derived as:

\[
K = \frac{-\omega k_1 \sqrt{1 - k_2^2} + kk_1 k_2 - V_C}{e^{-k \cdot \arccos(-k_2) - 2\pi} / \omega}
\]  

(5-7)

where \( k_2 = \frac{V_C}{\omega A_s R_c C_{\text{dw}}} \)
Chapter 5: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Resistor-controlled DCVC

It can be seen from Fig. 5-3 that the diode starts to conduct when $V_{anod}$, which is the same as $V_{Cup}$ in Fig. 5-5, becomes zero during the period from 0 to $\pi$, which can be expressed by substituting $V_{Cup} = 0$ into (5-5) as:

$$\omega k_1 \cdot \sin\omega t + kk_1 \cdot \cos \omega t + V_C + Ke^{-kt} = 0$$

(5-8)

The exponential component $Ke^{-kt}$ in (5-8) relates to the transient response of the circuit which does not change much during a short time period of one or half a cycle of $V_{Cup}$, which is usually much smaller than the time constant of the circuit $\tau$ determined by the product of the capacitor and resistor of the circuit $R_c(C_{up} + C_{down})$. As a result, $Ke^{-kt}$ can be set roughly at a constant value $Ke^{-kt_c}$ where $t_c$ can be simply zero. However, the closer $t_c$ is to the moment the diode starts to conduct $t_{on}$, the smaller the error it will cause. From (5-8), the moment the diode starts to conduct can finally be derived as:

$$t_{on} \approx \frac{\arcsin \left( -\frac{V_c+Ke^{-kt_c}}{k_1\sqrt{\omega^2+k^2}} \right) - \arctan \frac{k}{\omega}}{\omega}$$

(5-9)

5.3.3 The Relationship between $T_{con}$ and $V_c$

Substituting (5-3) and (5-9) into (5-1), the diode conduction period $T_{con}$ can be derived as:

$$T_{con} \approx \frac{\arccos \left( -\frac{V_c}{\omega \sqrt{R_c C_{down}}} \right) + \arcsin \left( \frac{V_c+Ke^{-kt_c}}{k_1\sqrt{\omega^2+k^2}} \right) + \arctan \frac{k}{\omega}}{\omega}$$

(5-10)

Fig. 5-6 of Section 5.4 shows the relationship curve between $T_{con}$ and $V_c$ when substituting the real circuit parameters in Table 5-1 of Section 5.4 into (5-10), from which it can be seen that $T_{con}$ is roughly proportional to $V_c$.

It can be seen from (5-10) that the angular frequency $\omega$ is included in it, which means that the frequency of the circuit has an influence on the relationship between $T_{con}$ and $V_c$. Actually in a LC parallel resonant circuit such as the one in the resonant tank of a push pull converter, when the influence of the load is ignored, the natural oscillation frequency of the circuit can be simplified as (5-11):
\[ \omega = 2\pi f = \frac{1}{\sqrt{LC}} \]  

(5-11)

Replacing the angular frequency \( \omega \) in (5-10) with relevant inductance and equivalent capacitances of the circuit expressed by (5-11), (5-10) becomes:

\[ T_{\text{con}} = \sqrt{LC_{\text{on}}} \cdot \left( \arccos\left( -\frac{V_C \cdot \sqrt{LC_{\text{on}}}}{A_sR_cC_{\text{dw}}} \right) - \arcsin\left( -\frac{V_C + Ke^{-\frac{1}{k_1}L_{\text{off}}}}{k_1\sqrt{L_{\text{off}}} + k^2} \right) + \arctan(k\sqrt{L_{\text{off}}}) \right) \]  

(5-12)

Where \( C_{\text{on}} \) and \( C_{\text{off}} \) represent the capacitance of the circuit when the diode is on and off, respectively, as expressed by (5-13) and (5-14).

\[ C_{\text{on}} = C_{\text{dw}} \]  

(5-13)

\[ C_{\text{off}} = \frac{C_{\text{up}}C_{\text{dw}}}{C_{\text{up}} + C_{\text{dw}}} \]  

(5-14)

### 5.3.4 The Relationship between \( C_e \) and \( V_c \)

The relationship between \( C_e \) and \( T_{\text{con}} \) needs to be found first before combining it with (5-12) to get the relationship between \( C_e \) and \( V_c \). The derivation of the relationship between \( C_e \) and \( T_{\text{con}} \) is based on a LC parallel resonance circuit. From (5-11), the equivalent capacitance of the circuit can be derived as:

\[ C = \frac{1}{L \cdot (2\pi f)^2} = \frac{T^2}{4\pi^2L} \]  

(5-15)

where \( T \) represents the duty cycle, i.e. the reciprocal of the frequency \( f \). Assume that the inductance of the circuit is fixed while the capacitance switches between two distinct values \( C_{\text{on}} \) and \( C_{\text{off}} \), if the period the capacitance being \( C_{\text{on}} \) is \( t_{\text{on}} \) and that the capacitance being \( C_{\text{off}} \) is \( t_{\text{off}} \) respectively in one duty cycle, according to (5-15), the equivalent capacitance \( C_e \) of the circuit is:

\[ C_e = \frac{(t_{\text{on}} + t_{\text{off}})^2}{4\pi^2L} \]  

(5-16)
Actually, $t_{on}$ equals $T_{con}$, and $t_{off}$ can be derived based on the principle that the waveforms when the capacitance is $C_{on}$ and $C_{off}$ need to go continuously into each other. Finally the relationship between $C_e$ and $T_{con}$ is derived as:

$$
C_e = \frac{(2\pi\sqrt{LC_{off}} + (1 - \frac{C_{off}}{C_{on}}) \cdot T_{con})^2}{4\pi^2 L} \tag{5-17}
$$

Substituting (5-12) into (5-17), gives the relationship between $C_e$ and $V_c$:

$$
C_e = \left[ \sqrt{C_{off}} + \frac{\sqrt{C_{on}} - \sqrt{C_{off}}}{2\pi} (\arccos \left( -\frac{V_c \sqrt{LC_{on}}}{A_s R_c \cdot C_{dw}} \right) - \arcsin \left( -\frac{V_c + Ke^{-kt_c}}{k_1 \sqrt{\frac{1}{LC_{off}} + k^2}} \right) + a \arctan(k\sqrt{LC_{off}}) \right]^2 \tag{5-18}
$$

which can be simplified as:

$$
C_e = \left[ \sqrt{C_{off}} + \frac{\sqrt{C_{on}} - \sqrt{C_{off}}}{2\pi} \cdot T_{rad} \right]^2 \tag{5-19}
$$

where:

$$
T_{rad} = \arccos \left( -\frac{V_c \sqrt{LC_{on}}}{A_s R_c \cdot C_{dw}} \right) - \arcsin \left( -\frac{V_c + Ke^{-kt_c}}{k_1 \sqrt{\frac{1}{LC_{off}} + k^2}} \right) + a \arctan(k\sqrt{LC_{off}}) \tag{5-20}
$$

Actually, $T_{rad}$ is the diode conduction period $T_{con}$ in radians. Theoretically, $T_{rad}$ changes from 0 to $2\pi$.

When $T_{rad}$ is 0, (5-19) becomes:

$$
C_e = C_{off} \tag{5-21}
$$

It means that when the diode conduction period is 0, or in other words the diode never conducts, the equivalent capacitance is $C_{off}$ which coincides exactly with the real circuit situation. While when $T_{rad}$ is $2\pi$ which means that the diode always conducts so as to be equivalent to a short-circuit, (5-19) becomes:
Again, this is in agreement with the basic concept and practical circuit situation.

Fig. 5-7 of Section 5.4 shows the relationship curve between \( C_e \) and \( V_c \) when substituting the real circuit parameters in Table 5-1 of Section 5.4 into (5-18), from which it can be seen that \( C_e \) is roughly proportional to \( V_c \).

### 5.3.5 The Relationship between \( f_e \) and \( V_c \)

Substituting (5-18) into (5-11), gives the relationship between \( f_e \) and \( V_c \):

\[
f_e = \frac{1}{2\pi \sqrt{L} \cdot \left( \sqrt{C_{\text{off}}} + \frac{\sqrt{C_{\text{on}} - C_{\text{off}}}}{2\pi} \right) \left( \arccos \left( -\frac{V_c/LC_{\text{on}}}{A_vRCL} \right) - \arcsin \left( -\frac{V_c + Ke^{-k_1}}{k_1 \sqrt{C_{\text{off}}}} \right) + a \arctan \left( \frac{k_1 \sqrt{C_{\text{off}}}}{k_2 + k_1} \right) \right)} \quad (5-23)
\]

Fig. 5-8 of Section 5.4 shows the relationship curve between \( f_e \) and \( V_c \) when substituting the real circuit parameters in Table 5-1 of Section 5.4 into (5-23), from which it can be seen that \( f_e \) is roughly inversely proportional to \( V_c \).

### 5.4 Simulation Study

Simulation study is conducted with the push pull converter as shown in Fig. 5-1 (a). Table 5-1 shows the circuit parameters used in the simulation and theoretical calculation.

<table>
<thead>
<tr>
<th>Vdc (V)</th>
<th>As (V)</th>
<th>( R_c ) (Ω)</th>
<th>( L ) (µH)</th>
<th>( C_{up} ) (nF)</th>
<th>( C_{dw} ) (nF)</th>
<th>( f ) (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>30</td>
<td>100</td>
<td>3.3</td>
<td>300</td>
<td>300</td>
<td>200</td>
</tr>
</tbody>
</table>

Fig. 5-6 shows the simulation and theoretical analysis results for the relationship between \( T_{\text{on}} \) and \( V_c \) together, from which it can be see that they coincide with each other almost exactly especially when \( V_c \) is smaller than 150V. Fig. 5-7 and 5-8 are the simulation and theoretical analysis results for the relationships between \( C_e \) and \( V_c \), and \( f_e \) and \( V_c \) together, respectively, from which it can be seen that the simulation and theoretical analysis results agree with each other quite well.
Chapter 5: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Resistor-controlled DCVC

Fig. 5-6. Simulation and theoretical analysis results of the relationship between $T_{con}$ and $V_c$.

Fig. 5-7. Simulation and theoretical analysis results of the relationship between $C_e$ and $V_c$.

Fig. 5-8. Simulation and theoretical analysis results for the relationship between $f_e$ and $V_c$.

Factors which cause the errors between the simulation and theoretical analysis results include the simplification of the real push pull converter to the circuit as shown in Fig. 5-2, the idealization of the diode, the assumption that the transient response of the circuit $Ke^{-kt}$ in (5-8) is fixed, and the assumption that the driving voltage source $V_{DC}$ is a fixed frequency.
and amplitude pure sinusoidal wave in the theoretical analysis, however, both the frequency and amplitude of the resonant tank in real push pull converter is not fixed absolutely, and the real soft switching frequency of the push pull converter is not the natural oscillating frequency expressed by (5-11) literally. Further the frequency of the real push pull converter is not solely determined by the inductor and capacitor in its resonant tank, but also influenced by other factors such as the capacitance of C1 and C2 as shown in Fig. 5-1 (a) especially at high frequencies.

5.5 Experimental Results

Fig. 5-9 shows the real circuit experimental result of the relationship between $f_e$ and $V_c$ with the circuit shown in Fig. 5-1 (a). The main circuit parameters used in the experiments are: $V_{dc}$ (10V), L (12.49uh), $C_{up}$ (60nF), $C_{dw}$ (60nF) and $R_c$ (100Ω). It can be seen from Fig. 5-9 that when the control voltage increases from 0 to 30 volts, the frequency decreases from 242 kHz to 224 kHz changing 18 kHz in total, which agrees with the simulation and theoretical analysis result in that $f_e$ is inversely proportional to $V_c$.

Fig. 5-9. Experimental result of the relationship between $f_e$ and $V_c$.

Fig. 5-10 shows some experimental waveforms which display the inverse relationship between $f_e$ and $V_c$. The green DC line at the bottom is the control voltage $V_c$ and the yellow waveform on the top is the voltage at one terminal of the resonant tank. It can be seen from Fig. 5-10 that frequency declines from 242 kHz to 230 kHz while the control voltage $V_c$ increases roughly from 0V to 20V.
Fig. 5-10. Practical experimental results showing the higher the control voltage is, the lower the frequency.
Fig. 5-11 shows some experimental waveforms which display the voltage of the resonant tank (the yellow one on the top) and the controlling voltage (the green one on the bottom) at around 10 MHz. As can be seen from Fig. 5-11 that as the equivalent capacitance of the R-DCVC can be varied continuously with a DC voltage, potentially this method is able to be used at very high-frequency applications.
5.6 Summary

A new method to adjust the frequency of switching mode resonant converters using the autonomous push pull converter as an example is presented in this chapter. It varies the frequency of the converter by including an R-DCVC in its resonant tank. The R-DCVC is constituted with two capacitors in series and a diode in parallel with one of them. The equivalent capacitance of the R-DCVC is controlled by the voltage on the positive terminal of the diode. This voltage varies the equivalent capacitance by changing the conduction period of the diode. The higher the voltage on the positive terminal of the diode is, the longer the diode conducts and the longer the diode conducts, the larger the equivalent capacitance of the R-DCVC. The adjustable range of the R-DCVC is between the capacitance of the capacitor not in parallel with the diode and the capacitance of the two capacitors in series. Finally, the frequency of the converter is inversely related to the controlling voltage of the R-DCVC. The circuit structure and control strategy of the proposed method is much simpler than traditional switch mode capacitors and inductors, and as there is no switch used in the R-DCVC, the EMI problem is much reduced. As the equivalent capacitance of the R-DCVC is varied smoothly with a DC voltage, it has the potential to be applied to much higher frequency levels than traditional switch mode capacitors and inductors. Mathematical models for the relationship between the equivalent capacitance of the R-DCVC and the control voltage $V_c$, and the relationship between the ZVS frequency of the autonomous push pull converter and the control voltage $V_c$ were developed and verified by simulation and experimental results.
Chapter 6:

Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Transistor-controlled DCVC

6.1 Introduction

Dynamic frequency adjustment is often needed for both low power radio systems and power electronic circuits. For example, it is of great importance to be able to adjust the operating frequency of wireless power transfer (WPT) systems dynamically, so that soft-switching and resonant operation can be achieved for maximum power transfer and efficiency [70, 219-222]. Traditionally, this is realized through switching mode capacitors [21, 75, 101, 102, 223-225] or inductors [107, 109-114, 226]. PWM signals instead of a DC voltage are used in their control. The active switches in them may need gate drivers and a separate voltage source, which makes the circuit complex and sometimes inconvenient, for example when used at the secondary side of an IPT system where an auxiliary power supply is not readily available. Furthermore, at high frequencies it is difficult for switch mode circuits to be accurately soft-switched due to practical detection delays, component accuracies, etc.

On the other hand, varactors are widely used for frequency control in radio engineering [180, 227-229]. However, the voltage and current ratings of varactors are too low to be applied in power electronics circuits. A $R-DCVC$ was introduced in the previous chapter. The equivalent capacitance of this $R-DCVC$ can be controlled with a DC voltage. This chapter proposes a Transistor-controlled $DCVC$ ($T-DCVC$) for dynamic frequency control of IPT systems. Similar to varactors the equivalent capacitance of the $T-DCVC$ can also be controlled simply with a DC voltage, therefore, when the $T-DCVC$ is used as a variable resonant capacitor in a WPT system, the ZVS frequency of the system can be adjusted smoothly and as a result can reach very high (MHz) levels with low EMI. As no active switching is involved in the $T$-

DCVC, no switch mode gate drivers are needed which makes the overall structure of the $T$-DCVC simpler. In addition, the $T$-DCVC can be used flexibly in different locations in resonant circuits for parallel and series tuning, which is often required in wireless power transfer systems. With the $T$-DCVC, mature PLL technology can be employed directly to lock the operating frequency of DC-AC converters such as the autonomous push pull converter, which becomes a voltage controlled oscillator (VCO) when the $T$-DCVC is applied to its resonant tank.

There are variations in the method proposed in this chapter by realizing the transistor with BJTs, or MOSFETs, or connecting the ground of the control voltage to the ground of the autonomous push pull converter, or to one end of the resonant tank, or to the base or gate of the transistor, respectively. As the basic operating principle of these variations are the same, only one of them is described in full in this chapter with detailed theoretical analysis and practical circuit experimental results.

The chapter is organized as follows. Section 6.1 is the Introduction. The basic operating principle of the $T$-DCVC is explained in Section 6.2. Section 6.3 presents the theoretical modelling of the $T$-DCVC by establishing the relationships of the equivalent capacitance of the $T$-DCVC and the ZVS frequency of the converter against the DC control voltage. Practical experimental results for the open-loop relationship between the ZVS frequency of the converter and the control voltage, and the closed-loop (with the PLL controller added which will be introduced in detail in Chapter 7) waveforms of the circuit, are provided in Section 6.4. Section 6.5 introduces some variations of the proposed method, and finally a summary is made in Section 6.6.

### 6.2 The $T$-DCVC and Basic Operating Principle

To take advantage of the ZVS frequency changing with the variation of its resonant capacitor, an autonomous push pull converter as shown in Fig. 6-1 (a) is used as an example to show how the T-DCVC works and explain its basic operating principle. It can be seen from Fig. 6-1 (a) that the normal fixed value resonant capacitor of the autonomous push pull converter is replaced by the $T$-DCVC consisting of $C_{up}$, $C_{dw}$, $D_c$, $Q_c$ and $R_b$ as shown in the dashed box titled “$T$-DCVC”. The equivalent capacitance of the $T$-DCVC can be controlled by the voltage $V_c$ because $V_c$ influences the conduction period of the diode $D_c$ by controlling the base and collector currents $i_b$ and $i_c$ of the transistor $Q_c$. The higher $V_c$ is, the larger $i_b$ and $i_c$, and the
larger $i_c$ is, the higher the voltage on the anode of the diode $D_c$ and the longer $D_c$ conducts. When the diode $D_c$ conducts, the equivalent capacitance of the T-DCVC is the capacitance of $C_{dw}$. When the diode is off, the equivalent capacitance of the T-DCVC is approximately the capacitance of $C_{up}$ and $C_{dw}$ in series. As $C_{dw}$ is bigger than $C_{up}$ and $C_{dw}$ in series, the longer the diode conducts, the larger the average equivalent capacitance of the T-DCVC is. By controlling the conduction period of the diode $D_c$, the voltage $V_c$ controls the average equivalent capacitance of the T-DCVC and finally the ZVS frequency of the autonomous push pull converter.

When the diode $D_c$ in the T-DCVC as shown in Fig. 6-1 (a) conducts only at the positive or negative half cycle of the voltage across the resonant tank, the waveform of the voltage of the resonant tank will not be balanced. To solve this problem, a balanced version of the T-DCVC as shown in Fig. 6-1 (b) can be adopted, where the two diodes $D_{c1}$ and $D_{c2}$ conduct at the positive and negative half cycle of the voltage of the resonant tank, respectively, so that the waveform of the voltage of the resonant tank will be balanced. For simplicity, analysis of the T-DCVC in this research will focus on the single-side version as shown in Fig. 6-1 (a).
6.3 Theoretical Modelling

Fig. 6-2 shows the equivalent circuit for theoretical modelling.

Fig. 6-2. The simplified circuit for theoretical analysis and derivation of approximate equivalent capacitance of the T-DCVC.

Based on the fact that the voltage of the resonant tank ($v_{ab}$) of the autonomous push pull converter is approximately a sine wave, the autonomous push pull converter shown in Fig. 6-1 (a) is simplified as the one shown in Fig. 6-2 (a), which includes only the sinusoidal source $v_s$ and the T-DCVC, where $i_c$ represents the collector current of $Q_c$. Fig. 6-2 (b) shows the situation when the T-DCVC is replaced by its equivalent capacitance $C_e$.

Fig. 6-3 shows the typical wave forms of the circuit in steady state including the voltage source-$v_s$, the voltage across the capacitor $C_{up}$ and the diode $D_c$-$v_{Cup}$, the current flowing through the diode $D_c$-$i_D$ and the current of the capacitor $C_{up}$-$i_{Cup}$. It can be seen from Fig. 6-3 that the voltage across the diode ($v_{Cup}$) is zero at both of the moments when the diode is
turned on and off, which means that the diode is zero voltage switched. The current of the diode \( i_D \) reduces to zero gradually before the diode turns off, so the diode reverse recovering is less an issue. This helps the passive diode to operate at a fully soft switched condition, making the T-DCVC suitable for high-frequency operation.

As the equivalent capacitance \( C_e \) of the T-DCVC plays a central role for the proposed method, the major task of the theoretical analysis is to find the relationship between \( C_e \) and the control voltage \( V_c \), which is achieved in three steps. Firstly the relationship between the diode conduction period \( T_{con} \) and \( V_c \) is to be found. Secondly it is to find the relationship between \( C_e \) and \( T_{con} \). Finally the relationship between \( C_e \) and \( V_c \) can be derived based on the above two relationships.

### 6.3.1 The Relationship between \( T_{con} \) and \( V_c \)

Before the relationship between \( T_{con} \) and \( V_c \) is derived, two exact moments, i.e. the moment the diode starts to conduct “\( t_{on} \)” and the moment the diode stops to conduct ‘\( t_{off} \)” need to be determined first. Then \( T_{con} \) can be calculated with (6-1):

\[
T_{con} = t_{off} - t_{on}
\]  

Fig. 6-4 shows the equivalent circuit of Fig. 6-2 (a) when the diode is conducting, got by removing \( C_{up}, D_c \) and \( i_c \), as an ideal conducting diode amounts to a short-circuit. “\( i_s \)” in Fig. 6-4 represents the current flowing through the conducting diode \( D_c \). \( D_c \) is regarded as stopping to conduct when \( i_s \) drops to zero. As \( i_s \) drops to zero when the voltage \( v_s \) reaches its maximum at \( \pi/2 \), the moment the diode stops to conduct \( t_{off} \) can be express by (6-2).

![Fig. 6-4. The equivalent circuit when the diode is conducting.](image)
\[ t_{\text{off}} = \frac{\pi}{2\omega} \]  

(6-2)

Fig. 6-5 shows the equivalent circuit of Fig. 6-2 (a) when the diode is not conducting, regarded as open and removed from the circuit. The diode is regarded as starting to conduct when the voltage \( v_{\text{Cup}} \) becomes zero.

Fig. 6-5. The equivalent circuit when the diode is not conducting and the transistor is modelled as a current source.

Assume \( v_s = A_s \sin \omega t \), the equation governing \( v_{\text{Cup}} \) is:

\[
\frac{dv_{\text{Cup}}}{dt} = \frac{\omega A_s C_{dw} \cos \omega t + i_c}{C_{\text{up}} + C_{\text{dw}}} 
\]

(6-3)

The solution of (6-3) is:

\[
v_{\text{Cup}} = \frac{A_s C_{\text{dw}}}{C_{\text{up}} + C_{\text{dw}}} \sin \omega t + \frac{i_c}{C_{\text{up}} + C_{\text{dw}}} t + K
\]

(6-4)

To determine the integral constant \( K \) in (6-4), substituting the initial condition (\( t = -\frac{3\pi}{2\omega} \) and \( v_{\text{Cup}} = 0 \) as shown in Fig. 6-3) into (6-4) gives:

\[
K = \frac{3\pi}{2\omega} i_c - A_s C_{\text{dw}} \\
\]

(6-5)

Equation (6-4) expresses \( v_{\text{Cup}} \) during the period the diode is off. The moment the diode starts to conduct \( t_{\text{on}} \) is when \( v_{\text{Cup}} \) becomes zero as expressed by (6-6):
There is no accurate analytical solution for (6-6). However, using Taylor’s series and ignoring the high order terms gives: $\sin \omega t_{on} = \omega t_{on}$. Substituting it into (6-6), an approximate analytical solution of $t_{on}$ can be obtained as:

$$t_{on} \approx -\frac{K(C_{up} + C_{dw})}{\omega A_s C_{dw} + i_c}$$

(6-7)

Substituting (6-2) and (6-7) into (6-1) gives the relationship between $T_{con}$ and $i_c$.

$$T_{con} \approx \frac{\pi}{2\omega} + \frac{K(C_{up} + C_{dw})}{\omega A_s C_{dw} + i_c}$$

(6-8)

Assuming the amplification of the transistor $Q_c$ is $\beta$, the relationship between $i_c$ and $V_c$ can be expressed by (6-9):

$$I_D = \beta \cdot \frac{V_c - 0.7}{R_b}$$

(6-9)

Substituting (6-5) and (6-9) into (6-8) gives the relationship between $T_{con}$ and $V_c$.

$$T_{con} \approx \frac{\pi}{2\omega} + \frac{\frac{3\pi}{2\omega} \beta \cdot \frac{R_b A_s C_{dw}}{V_c - 0.7}}{\beta + \omega A_s C_{dw} \frac{R_b A_s C_{dw}}{V_c - 0.7}}$$

(6-10)

Fig. 6-6 shows the theoretical relationship between $T_{con}$ and $V_c$ got from (6-10) using parameters of the components shown in Table 6-1 of Section 6.4, from which it can be seen that a higher $V_c$ leads to a longer diode conduction period as explained in Section 6.2. When $V_c$ goes to infinite, (6-10) becomes “$T_{con} \approx \frac{2\pi}{\omega}$”, which means that $T_{con}$ cannot go beyond the period of the oscillation of the circuit $\frac{2\pi}{\omega}$ in theory.
6.3.2 The Relationship between $C_e$ and $T_{con}$

The relationship between $C_e$ and $T_{con}$ is derived based on the circuit shown in Fig. 6-2, and the idea that the AVECD (absolute value of the electric charge and discharge) of the $T$-$DCVC$ equals that of its equivalent capacitance $C_e$ during one cycle of the sinusoidal source $v_s$. The AVECD of a capacitor $C$ during the period from $t_1$ to $t_2$ when the voltage across the capacitor is “$v$” can be calculated by (6-11):

$$|\Delta Q| = \int_{t_1}^{t_2} |i(t)| \cdot dt = \int_{t_1}^{t_2} C \cdot |v'| \cdot dt \quad (6-11)$$

where $i(t)$ is the current flowing through the capacitor during the period. As the value of $v'$ is positive when “$v$” increases and negative when “$v$” decreases, $|\Delta Q|$ is derived by calculating its values during the periods that “$v$” increases and decreases, respectively, and adding the results together by taking the negative value of “$\Delta Q$ ” into consideration during the period when “$v$” decreases. Equation (6-11) is used to calculate the various AVECD below. The reason to use the AVECD instead of the real value of electric charge and discharge is that the total real value of electric charge and discharge during one cycle of the sinusoidal source $v_s$ is zero.

The equivalent capacitance $C_e$ is calculated in three steps. Firstly, the AVECD of the $T$-$DCVC$- $|\Delta Q_{T-DCVC}|$ is calculated. Secondly, the AVECD of the equivalent capacitance $C_e$-$|\Delta Q_{Ce}|$ is calculated. Finally, $C_e$ is derived by equating $|\Delta Q_{T-DCVC}|$ and $|\Delta Q_{Ce}|$. 
\[ |\Delta Q_{\text{Don}}| = \int_{\omega t_{\text{on}}}^{\frac{\pi}{2}} C_{\text{on}}(A_s\sin \omega t) \, d(\omega t) = C_{\text{on}} A_s (1 - \sin \omega t_{\text{on}}) \] (6-12)

As can be seen from Fig. 6-3, the “on” period of the diode is from \( \omega t_{\text{on}} \) to \( \frac{\pi}{2} \) when \( v_s \) increases.

\[
|\Delta Q_{\text{vs}}| = -\int_{-\frac{3\pi}{2}}^{-\frac{\pi}{2}} C_{\text{off}} \cdot (A_s\sin \omega t) \, d(\omega t) + \int_{-\frac{\pi}{2}}^{\omega t_{\text{on}}} C_{\text{off}} \cdot (A_s\sin \omega t) \, d(\omega t) = C_{\text{off}} A_s (3 + \sin \omega t_{\text{on}}) \] (6-13)

As can be seen from Fig. 6-3, the “off” period of the diode is from \(-\frac{3\pi}{2}\) to \(\omega t_{\text{on}}\), which is divided into two periods “from \(-\frac{3\pi}{2}\) to \(-\frac{\pi}{2}\), and \(-\frac{\pi}{2}\) to \(\omega t_{\text{on}}\)”, when \(v_s\) decreases and increases, respectively.

\[
|\Delta Q_{\text{ic}}| = i_c \cdot \Delta t = i_c \frac{\omega t_{\text{on}} + \frac{3\pi}{2}}{\omega} \] (6-14)

where \(\Delta t\) is the period during which the diode is off, i.e. from \(-\frac{3\pi}{2}\) to \(\omega t_{\text{on}}\), which should be in the form of the absolute time instead of radians.

\[ |\Delta Q_{\text{DCVC}}| = |\Delta Q_{\text{Don}}| + |\Delta Q_{\text{vs}}| + |\Delta Q_{\text{ic}}| \]

\[ = A_s [3C_{\text{off}} + C_{\text{on}} + (C_{\text{off}} - C_{\text{on}})\sin \omega t_{\text{on}}] + i_c \left( t_{\text{on}} + \frac{3\pi}{2\omega} \right) \] (6-15)
The $C_{on}$ and $C_{off}$ in (6-12), (6-13), (6-14) and (6-15) means the instant capacitance of the T-DCVC during the period the diode is on and off, respectively as expressed by (6-16) and (6-17).

$$C_{on} = C_{dw}$$

$$C_{off} = \frac{C_{up}C_{dw}}{C_{up} + C_{dw}}$$

The AVECD of the equivalent capacitance $C_e$ during one cycle of the sinusoidal voltage source $v_s$ can be calculated by (6-18):

$$|\Delta Q_{Ce}| = -\int_{\frac{-\pi}{2}}^{\frac{-3\pi}{2}} C_e(A_s\sin\omega t')d(\omega t) + \int_{\frac{-\pi}{2}}^{\frac{\pi}{2}} C_e(A_s\sin\omega t')d(\omega t) = 4C_eA_s$$

The calculation of $|\Delta Q_{Ce}|$ is divided into two periods “from $-\frac{3\pi}{2}$ to $-\frac{\pi}{2}$, and $-\frac{\pi}{2}$ to $\frac{\pi}{2}$” because it can be seen from Fig. 6-3 that $v_s$ decrease and increase during these two periods, respectively so that $v_s'$ is negative and positive accordingly which provides convenience for the calculation of the absolute value.

By equating (6-15) and (6-18), the equivalent capacitance $C_e$ of the T-DCVC can finally be derived as:

$$C_e = \frac{3C_{off} + C_{on} + (C_{off} - C_{on})\sin\omega t_{on}}{4} + \frac{t_{on} + \frac{3\pi}{2\omega}}{4A_s}i_c$$

As “$t_{off}$” is a fixed value $\frac{\pi}{2\omega}$, only “$t_{on}$” appears in (6-19). By calculating $T_{con}$ with (6-10) and $C_e$ with (6-19), the relationship between $C_e$ and $T_{con}$ can be obtained as shown in Fig. 6-7 using parameters of the components shown in Table 6-1 of Section 6.4, from which it can be seen that the longer the diode conducts, the larger the equivalent capacitance of the T-DCVC is as explained in Section 6.2.
6.3.3 The Relationship between \( C_e \) and \( V_c \)

Substituting (6-9) into (6-19) gives the relationship between \( C_e \) and \( V_c \):

\[
C_e = \frac{3C_{off} + C_{on} + (C_{off} - C_{on})\sin\omega t_{on}}{4} + \frac{\beta(t_{on} + \frac{3\pi}{2\omega})}{4A_S R_b} \cdot (V_c - 0.7) \tag{6-20}
\]

where: \( t_{on} \) is expressed by (6-7). As the relationships of \( T_{con} \) and \( V_c \), and \( C_e \) and \( T_{con} \) as shown in Fig. 6-6 and Fig. 6-7 are proportionate, it can be deduced that \( C_e \) is proportional to \( V_c \) as well, which is in consistent with the theoretical and experimental results shown in Fig. 6-9 of Section 6.4 that the operating frequency \( f \) decreases with the control voltage \( V_c \).

6.3.4 The Relationship between \( f \) and \( V_c \)

Strictly speaking, what the voltage \( V_c \) controls is the ZVS frequency of the autonomous push pull converter. However, when the circuit quality factor \( Q \) is high, the ZVS frequency is close to the undamped natural oscillation frequency as expressed by (6-21) [180].

\[
f = \frac{1}{2\pi\sqrt{LC}} \tag{6-21}
\]

Substituting (6-20) into (6-21) gives the relationship between the approximate ZVS frequency of the converter and the control voltage \( V_c \).
\[
f = \frac{1}{2\pi L} \sqrt{\frac{3C_{\text{off}} + C_{\text{on}} + (C_{\text{off}} - C_{\text{on}}) \sin \omega t_{\text{on}}}{4} + \frac{\beta (t_{\text{on}} + \frac{3\pi}{2\omega})}{4A_{\beta}R_{b}} \cdot (V_c - 0.7)}
\] (6-22)

### 6.4 Experimental Results

Fig. 6-8 shows the experimental setup, including the push pull converter, the \(T-DCVC\), the primary and secondary side coil \(L_p\) and \(L_s\), the parallel tuning full-bridge regulation pick-up circuit and the PLL controller (will be introduced in detail in chapter 7). Such a configuration may be suitable for low power contactless battery charging applications with very small physical separation between the primary and secondary coils.

![Experimental Setup](image)

**Fig. 6-8. The experimental setup.**

Table 6-1 and 6-2 show the components and parameters of the primary and secondary side circuits, and the parameters of the coils, respectively.

| \(V_{DC}\) (V) | \(L_1, L_2\) (mH) | \(C_1, C_2\) (nF) | \(D_1, D_2\) | \(S_1, S_2\)| \(C_{\text{up}}\) (nF) | \(C_{\text{dw}}\) (nF) | \(D_{\text{c}}\) | \(Q_{\text{c}}\) | \(R_{\text{b}}\) (k\(\Omega\)) | \(k\) | \(C_S\) (nF) | \(D_{\text{S1}}-D_{\text{S4}}\) | \(C_f\) (\(\mu\)F) | \(R_{\text{load}}\) (\(\Omega\)) |
|----------------|-----------------|-----------------|-------------|-------------|---------------|-----------------|-------------|-------------|----------------|------|-------------|----------------|-------------|--------------|----------------|
| 12             | 1               | 5.5             |BYV26C      | IRF3205     |               |                 |             |             |                 |      |             |                 |             |              |                |
| 1              | 50              | C3D02060F       | KSE13003   | 12          |               |                 |             |             |                 |      |             |                 |             |              |                |
|                |                 |                 |             |             |               |                 |             |             |                 |      |             |                 |             |              |                |
Table 6-2. Parameters of the primary and secondary side coils $L_P$ and $L_S$ (No iron cores).

<table>
<thead>
<tr>
<th>No iron cores</th>
<th>Value (uH)</th>
<th>Number of turns</th>
<th>Diameter of the coil (mm)</th>
<th>Diameter of the litz wire (mm)</th>
<th>Distance between $L_P$ and $L_S$ (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_P$</td>
<td>1.06</td>
<td>7</td>
<td>36.5</td>
<td>2.2</td>
<td>2.8</td>
</tr>
<tr>
<td>$L_S$</td>
<td>1.35</td>
<td>8</td>
<td>40</td>
<td>2.2</td>
<td>2.8</td>
</tr>
</tbody>
</table>

Fig. 6-9 shows the open-loop (without the PLL controller) experimental and theoretical relationships between the operating frequency of the converter and the control voltage $V_c$ together under two different situations when there is ($R_{load}=100\Omega$) and there is no load, from which it can be seen that the theoretical and experimental results agree with each quite well, and the operating frequency is negatively related to the control voltage $V_c$ as explained in Sections 6.2 and 6.3.

![Fig. 6-9. Experimental and theoretical relationship between the operating frequency of the converter and the control voltage.](image)

Fig. 6-10 shows the open-loop experimental relationships of the output power $P_{out}$ and efficiency $\eta$ (%) against the control voltage $V_c$, from which it can be seen that the output power and efficiency reach maximum of 10.8W and 74.7%, respectively with the control voltage $V_c$ is around 10V, when the operating frequency of the converter is about 1.65MHz (refer to Fig. 6-9). The efficiency $\eta$ (%) is calculated as the ratio of the output power ($V_{out}^2/R_{load}$) to the input power ($V_{DC}*i_{DC}$), where $V_{DC}$ and $i_{DC}$ are the voltage and current of the DC voltage source, respectively.
Chapter 6: Adjusting the ZVS Frequency of Autonomous Push Pull Converter by Transistor-controlled DCVC

Fig. 6-10. Experimental relationships of the output power $P_{out}$ (W) and efficiency $\eta$ (%) vs. the control voltage $V_c$.

Fig. 6-11. Experimental waveforms of $v_a$, COMP_IN, SIG_IN and $V_c$ when the reference frequency is set at 1.65MHz.

Fig. 6-11 shows the closed-loop waveforms (with the PLL controller added) of the voltage $v_a$ at the point “a” of the resonant tank (channel 1), the signal COMP_IN after the comparator $U_a$ (channel 2), the reference frequency SIG_IN (channel 3) and the output voltage of the PLL controller $V_c$ (channel 4) when the reference frequency is set at 1.65MHz. The details of the PLL controller is presented in Chapter 7.

It can be seen from Fig. 6-11 that the frequencies of all the first three channels $v_a$, COMP_IN and SIG_IN are 1.65MHz, which means that the operating frequency of the converter is locked in at 1.65MHz by the PLL controller through adjusting the equivalent capacitance of the $T$-DCVC with the control voltage $V_c$, when the output power and voltage reach their
maximum of 10.8 W and 32.87 V, respectively with the load resistance $R_{\text{load}}$ is 100Ω and the coupling coefficient $k$ is 0.62. In the experiment, the operating frequency can remain to be locked at 1.65MHz with the load resistance and the coupling coefficient $k$ changing between 50Ω to 250Ω, and 0.62 to 0.53, respectively.

### 6.5 Alternative Ways to Control the Voltage on the Anode of the Diode

Three major variations for the circuit as shown in Fig. 6-1 (a) will be introduced in this section as shown in Fig. 6-12, Fig. 6-17 and Fig. 6-18 respectively by changing the ground of the control voltage $V_c$ or by replacing the BJT transistor $Q_c$ with a MOSFET. The advantages and disadvantages of different options will be analysed and compared.

#### 6.5.1 Alternative Ways using BJT

Actually the ground of the control voltage $V_c$ in the circuit as shown in Fig. 6-1 (a) may not necessarily be connected to the ground of the autonomous push pull converter. Instead, it can also be connected to the emitter of the control BJT transistor $Q_c$ directly as shown in Fig. 6-12 to fulfill the task of controlling the collector current $i_c$ of the transistor $Q_c$.

![Fig. 6-12. The situation when the ground of the control voltage $V_c$ is connected to the emitter of $Q_c$.](image)

The major difference between the performances of the circuit as shown in Fig. 6-1 (a) and that of the one as shown in Fig. 6-12 is that for the one as shown in Fig. 6-1 (a), the frequency of the converter or the equivalent capacitance of the T-DCVC can be adjusted by the control voltage $V_c$ more finely, which means that a smaller change of the frequency or the equivalent capacitance needs a relatively larger change of the control voltage $V_c$ so that the frequency and the equivalent capacitance do not fluctuate or change abruptly with the noises on the control voltage $V_c$. However, the disadvantage of the circuit topology as shown in Fig. 6-1 (a) is that a higher control voltage $V_c$ is needed to control the frequency to change within the
same range as that of the circuit topology as shown in Fig. 6-12. For example, the control voltage \( V_c \) needs to change between 0 ~ 20V for the frequency to change 40 kHz for the circuit as shown in Fig. 6-1 (a) while the control voltage \( V_c \) may only need to change between 0 ~ 5V to control the frequency to have a 40 kHz change for the circuit topology as shown in Fig. 6-12. This is because the fluctuation of the voltage of the resonant tank needs to be offset by the controlling voltage \( V_c \) for the circuit topology as shown in Fig. 6-1 (a) where the ground of the control voltage \( V_c \) connects to the ground of the autonomous push pull converter.

Below are the simulation and experimental results of the two circuit topologies as shown in Fig. 6-1 (a) and Fig. 6-12, respectively. Fig. 6-13 shows the simulation results of the two circuits for comparison. Fig. 6-14 shows the practical experimental results of the two circuits together. Fig. 6-15 shows the simulation and practical experiment results for the circuit as shown in Fig. 6-1 (a) together and Fig. 6-16 shows the simulation and practical experiment results for the circuit as shown in Fig. 6-12 together for comparison.

Table 6-3 and Table 6-4 show the components and parameters used in the simulation and the practical experiments, respectively.

**Table 6-3. Components and parameters used in the simulation.**

<table>
<thead>
<tr>
<th>( V_{dc} ) (V)</th>
<th>( L_1, L_2 ) (mH)</th>
<th>( C_1, C_2 ) (nF)</th>
<th>( D_1, D_2 )</th>
<th>( S_1, S_2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1</td>
<td>4.5</td>
<td>1N4148</td>
<td>IRFP240</td>
</tr>
<tr>
<td>( L ) (( \mu )H)</td>
<td>( C_{up}, C_{dw} ) (nF)</td>
<td>( D_c )</td>
<td>( Q_{Re} )</td>
<td>( R_b ) (( \Omega ))</td>
</tr>
<tr>
<td>7.85</td>
<td>20</td>
<td>MUR460</td>
<td>2N5550</td>
<td>1.8k</td>
</tr>
</tbody>
</table>

**Table 6-4. Components and parameters used in the practical experiments.**

| \( V_{dc} \) (V) | \( L_1, L_2 \) (mH) | \( C_1, C_2 \) (nF) | \( D_1, D_2 \), \( S_1, S_2 \) |
|------------------|------------------|------------------|-----------------|-----------------|
| 10               | 1                | 4.5              | BYV26           | IRFP240         |
| \( L \) (\( \mu \)H) | \( C_{up}, C_{dw} \) (nF) | \( D_c \) | \( Q_{Re} \) | \( R_b \) (\( \Omega \)) |
| 7.85             | 20               | BYV26           | KSE13003        | 1.8k           |

Fig. 6-13 and Fig. 6-14 show the simulation and practical experimental results for the two circuits as shown in Fig. 6-1 (a) and Fig. 6-12, respectively, from which it can be seen that both simulation and practical experiment results prove that the adjustable range of the frequency when the ground of the control voltage \( V_c \) is connected to the emitter of the control transistor \( Q_c \) is larger than that when the ground of the control voltage \( V_c \) is connected to that
of the autonomous push pull converter because of the reason mentioned above. The adjustable range of the frequency can be seen from the Y-axes of the plots.

Fig. 6-13. Simulation results of the two circuits as shown in Fig. 6-1 (a) and Fig. 6-12, respectively.

It can be seen from Fig. 6-13 that the adjustable range of the frequency when the ground of the control voltage is connected to the ground of the push pull converter is about 63 kHz changing roughly from 500 kHz to 437 kHz, while the adjustable range of the frequency when the ground of the control voltage is connected to the emitter of the control transistor $Q_c$ is about 90 kHz changing roughly from 519 kHz to 429 kHz.

Fig. 6-14. Experimental results of the two circuits as shown in Fig. 6-1 (a) and Fig. 6-12 respectively.

It can be seen from Fig. 6-14 that the adjustable range of the frequency when the ground of the control voltage is connected to the ground of the push pull converter is about 51 kHz changing roughly from 519 kHz to 468 kHz, while the adjustable range of the frequency when the ground of the control voltage is connected to the emitter of the control transistor $Q_c$
is about 100 kHz changing roughly from 536 kHz to 436 kHz. These results are summarized in Table 6-5 for comparison.

**Table 6-5.** Comparison between the results of simulation and practical experiments for the adjustable range of the frequency when the ground of the control voltage is connected to that of the push pull converter and the emitter of the control transistor, respectively.

<table>
<thead>
<tr>
<th>Results</th>
<th>Adjustable range of the frequency (kHz)</th>
<th>Ground to push pull</th>
<th>Ground to emitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation</td>
<td></td>
<td>63</td>
<td>90</td>
</tr>
<tr>
<td>Experiment</td>
<td></td>
<td>51</td>
<td>100</td>
</tr>
</tbody>
</table>

It can be seen from Table 6-5 that both simulation and practical experiment proves the adjustable range of the frequency when the ground is connected to the emitter is much larger than that when the ground is connected to the push pull converter.

Fig. 6-15 and Fig. 6-16 show the simulation and practical circuit experimental results together for comparison for the two circuit topologies as shown in Fig. 6-1 (a) and Fig. 6-12, respectively, from which it can be seen that the development trend of the curves are roughly the same, however there is indeed some difference between the results of the simulation and that of practical circuit experiments, especially the one when the ground of the control voltage is connected to the emitter of the controlling transistor $Q_c$ as shown in Fig. 6-16, when the result is more heavily influenced by the characteristic of the concrete transistor $Q_c$ used. As shown in Table 6-3 and 6-4, D1, D2, Dc and $Q_c$ used in the simulation and practical circuit experiments are different, all of which tend to pose a difference between the results of
the simulation and practical circuit experiments especially $Q_c$ as reflected by the result shown in Fig. 6-16.

![Fig. 6-16. Simulation and experiment result when the ground of the control voltage is connected to the emitter of the control transistor $Q_{rc}$.](image)

6.5.2 Alternative Ways using MOSFET

Instead of using BJTs, MOSFETs can also be used to realize the function of a voltage controlled variable resistor. Fig. 6-17 and Fig. 6-18 show the circuit topologies when the BJT $Q_c$ in the circuits as shown in Fig. 6-1 (a) and Fig. 6-12 are replaced by MOSFETs.

![Fig. 6-17. The circuit structure when a MOSFET instead of a BJT is used and the ground of the control voltage is connected to that of the push pull converter.](image)

Similar to the situation when BJTs are used, the major difference between the performances of the circuit topology when the ground of the control voltage is connected to the ground of push pull converter as shown in Fig. 6-17 and that when the ground of the control voltage is connected to the source of the MOSFET as shown in Fig. 6-18 is that the frequency of the converter of the former can be adjusted more finely by the control voltage than the latter,

![Graph](image)
which can be seen from both of the simulation and practical circuit experimental results as shown in Fig. 6-19 and Fig. 6-20, respectively.

Fig. 6-18. The circuit structure when a MOSFET instead of a BJT is used and the ground of the control voltage is connected to the source of the MOSFET.

Fig. 6-19 shows the simulation results of the two circuits as shown in Fig. 6-17 and Fig. 6-18, respectively, for the relationship between the frequency of the converter and the control voltage $V_c$, from which it can be seen that the frequency of the one with the ground of the control voltage connected to that of the push pull converter can be adjusted by the control voltage much more finely than that with the ground of the control voltage connected to the source of the MOSFET. Actually, it can be seen from Fig. 6-19 that the frequency of the one with the ground of the control voltage connected to the source of the MOSFET change so abruptly that it seems unrealistic to use the control voltage to adjust the frequency.
Fig. 6-20. Practical circuit experimental results of the two circuits as shown in Fig. 6-17 and Fig. 6-18 respectively.

Fig. 6-20 is the results of the practical circuit experiments, which shows similar feature as that of the simulation. Table 6-6 shows the components and parameters used in the simulation and practical circuit experiments for the two circuits as shown in Fig. 6-17 and Fig. 6-18.

Table 6-6. Components and parameters used in the simulation and practical circuit experiments for the two circuits as shown in Fig. 6-17 and Fig. 6-18.

<table>
<thead>
<tr>
<th>Vdc (V)</th>
<th>L1, L2 (mH)</th>
<th>C1, C2 (nF)</th>
<th>D1, D2</th>
<th>S1, S2</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1</td>
<td>4.5</td>
<td>BYV26</td>
<td>IRFP240</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L (μH)</td>
<td>C_{up}, C_{dw} (nF)</td>
<td>Dc</td>
<td>Sc</td>
<td>Rg(Ω)</td>
</tr>
<tr>
<td>7.85</td>
<td>20</td>
<td>BYV26</td>
<td>IRFP240</td>
<td>10k</td>
</tr>
</tbody>
</table>

Fig. 6-21 and Fig. 6-22 show the simulation and practical circuit experimental results together for comparison for the two circuits as shown in Fig. 6-17 and Fig. 6-18, respectively, from which it can be seen that the simulation and practical circuit experimental results comply with each other quite well for the circuit as shown in Fig. 6-17 while there is a relatively big difference between the simulation and practical circuit experimental results for the circuit as shown in Fig. 6-18, the ground of the control voltage of which is connected directly to the source of the MOSFET because, in this way, the characteristic of the MOSFET used has a big direct influence on the results of the simulation and practical circuit experiments. The big difference between the simulation and practical circuit experimental results may be because that there is a big difference between the characteristic of the MOSFET used in the software of the simulation and that used in the practical circuit experiment.
Fig. 6-21. Simulation and experiment result for the circuit as shown in Fig. 6-17.

Fig. 6-22. Simulation and experiment result for the circuit as shown in Fig. 6-18.

Fig. 6-22 shows the simulation and practical circuit experimental results together for the circuit as shown in Fig. 6-18, from which it can be seen that not only the simulation and practical circuit experimental results do not comply with each other very well, but the frequency of the converter change quite abruptly also instead of smoothly with the change of the control voltage. As a result, the circuit topology shown in Fig. 6-18 seems not quite practical as a way to adjust the frequency of the converter with the control voltage $V_c$, where the ground of the control voltage $V_c$ is connected directly to the source of the MOSFET.

### 6.5.3 The Situation When the Ground of the Control Voltage is Connected to One End of the Resonant Tank

The two circuit topologies as shown in Fig. 6-23 and Fig. 6-24 are also investigated, where the ground of the control voltage are connected to one end of the resonant tank.
Both of these two circuits can work in both simulation and practical circuit experiments. However, it is found in the practical circuit experiments that the waveforms of the voltages of the resonant tank of these two circuit topologies are quite seriously deformed, so they seem not practical circuit topologies. In summary, the most promising and practical choices are the three circuit topologies as shown in Fig. 6-1 (a), Fig. 6-12 and Fig. 6-17.

6.6 Summary

This chapter proposed a Transistor-controlled DCVC (T-DCVC), which functions similar to varactors in that its equivalent capacitance can be controlled by a DC voltage. However, the T-DCVC can handle high voltages and currents so that it can be used in DC-AC power converters of WPT systems, such as an autonomous push pull resonant converter, to adjust ZVS frequency. When combined with a PLL controller, the operating frequency of the system can be stabilized to simplify the circuit and EMI filter design, particularly for WPT systems with multiple power pickups, while maintaining soft-switching operation of the converter against magnetic coupling and load variations. The relationship between the
equivalent capacitance of the $T\text{-}DCVC$ and the DC control voltage was developed by theoretical analysis and verified by experimental results. A prototype circuit was built with a PLL controller to demonstrate that the soft-switching condition of the converter is maintained when the operating frequency is locked in at 1.65MHz under load and magnetic coupling variations.

In comparison to the method introduced in the last chapter to control the voltage level on the anode of the diode directly with a DC voltage through a resistor, the methods introduced in this chapter controlled the voltage level on the anode of the diode with BJTs or MOSFETs. One obvious advantage of the methods presented in this chapter is that the controlling current can be much smaller because the voltage level on the anode of the diode is mainly modulated by the voltage of the resonant tank itself, through the variation of the collector or drain current of the BJTs or MOSFETs. The function of the controlling voltage is only to control the base current of the BJTs, or gate voltage of the MOSFETs. In the case of MOSFETs, the currents of the gates are almost zero while when BJTs are employed the base currents are also much smaller than with the method introduced in the last chapter.

In total, six different circuit topologies using transistors to control the voltage level on the anode of the diode were investigated in this chapter. The topology using a BJT and with the ground of the controlling voltage connected to that of the autonomous push pull converter is described in detail, including the basic operating principle, detailed theoretical modelling and practical experimental results. The others are only briefly explained because their basic operating principles are the same. In conclusion, of the six different circuit topologies, three are promising and practical: the two using BJTs but with the ground of the controlling voltage connected to the ground of the autonomous push pull converter and to the emitter of the BJT, respectively; and the one using a MOSFET with the ground of the controlling voltage connected to the ground of the autonomous push pull converter.
Chapter 7:
Stabilizing the ZVS Frequency of Autonomous Push Pull Converter by PLL Control

7.1 Introduction

This chapter introduces one of the applications of the DCVCs presented in the previous chapter by combining it with a Phase Looked Loop (PLL) controller for stabilizing the frequency of the autonomous push pull converter. One of the most important advantages of the methods presented in Chapters 4, 5 and 6 is that they can be combined directly with the PLL technology to stabilize or adjust the frequency of high power DC-AC converters because their equivalent capacitance can be controlled with a DC voltage similar to the Voltage Controlled Oscillator (VCO) in a PLL control loop.

![Diagram of PLL controller](image)

PLL is a mature, effective and standard technology for frequency stabilization and adjustment in low power radio systems. Fig. 7-1 shows a typical PLL control loop which comprises three main parts: the Phase Detector (PD), the Low-pass Filter (LF) and the Voltage Controlled Oscillators (VCO).

Most oscillating circuits include inductors and capacitors, which determine the natural oscillating frequency of the circuit. The frequency of the circuit can be adjusted either through changing the value of the inductance or the value of the capacitance of the circuit.
Usually, capacitance adjustment is used because it is relatively more convenient than inductance adjustment. For VCOs in PLL control loops, the adjustment of the frequency is through varactors [227-238], one of the key components in a PLL control loop [239-252]. Varactors are special types of diodes. The capacitance of such types of diode varies with its reverse bias voltage so that it can be used for electronic tuning of frequency, especially in VCOs of a PLL control loop. The invention of varactors is of great significance because the inductance or capacitances of the circuits do not have to be adjusted mechanically anymore for frequency control. Instead, frequency adjustment can be realized automatically and accurately through electronic tuning of the capacitance of the varactors.

However, as the voltage and current ratings of varactors are too low they cannot be used in most power electronic circuits. Consequently, although PLL is a very mature and effective technology for accurately controlling the frequency of VCOs in low power signal processing circuits, it cannot be applied directly to controlling the frequency of high power DC-AC converters because there is no effective ways to adjust the frequency of high power DC-AC converters simply with a DC voltage. It is not difficult to imagine that this problem could be solved if some kind of voltage controlled variable capacitor like varactors were available and their voltage and current ratings were high enough to be used in high power circuits at the same time. In this way, the frequency of switching mode resonant converters including such a voltage controlled variable capacitor in its resonant tank could be adjusted conveniently with a DC voltage so that the converter functions like a voltage controlled oscillator (VCO). As a result, the frequency of the converter could be controlled with the mature PLL technology similar to the VCOs.

In summary, the main reason the frequency of a VCO can be controlled by a DC voltage is because of the availability of varactors. However, the voltage and current ratings of varactors are too low for them to be used in high power energy conversion circuits. Nevertheless, with the DCVCs presented in the previous, it becomes possible to control the frequency of resonant DC-AC power converters such as the autonomous push pull converter directly with the PLL technology in the same way as PLL technology is used to control the frequency of low power signal processing circuits. Because now with the availability of the DCVCs the frequency of DC-AC resonant converters can also be controlled by a DC voltage, which makes the DC-AC power converters for example, the autonomous push pull converter functions similar to a VCO.
A few PLL controllers will be presented in this chapter in combination with the \( T-DCVC \) to stabilize the frequency of the autonomous push pull converter. Similar approaches can also be applied to the methods introduced in Chapters 4 and 5. The content of this chapter is organized as follows. Section 7.1 is the Introduction. Section 7.2 presents the overall strategy and operating principle of the PLL controller. Section 7.3 provides the design details of the PLL control circuits. Section 7.4 describes the experimental results and Section 7.5 makes a summary.

### 7.2 The Overall Strategy and Operating Principle

Fig. 7-2 shows the overall circuit structure to stabilize the frequency of the autonomous push pull converter in comparison with a PLL control loop.

![Fig. 7-2. Comparison between the proposed method and a PLL control loop.](image)

The part of the circuit numbered ⑤ is an autonomous push pull converter with the common fixed value capacitor in its resonant tank replaced by a \( T-DCVC \) consisting of \( C_{up} \), \( C_{dw} \), \( D_c \) and \( Q_c \) in the dashed block, which has been presented in chapter 6. As explained in Chapter 6, the equivalent capacitance of the \( T-DCVC \) and therefore the frequency of the autonomous push pull converter changes with the control voltage \( V_c \). As a result, the autonomous push pull converter functions similar to a VCO because its frequency can be controlled by a DC voltage. However, one difference between the VCO formed by the autonomous push pull
Chapter 7: Stabilizing the ZVS Frequency of Autonomous Push Pull Converter by PLL Control

Converter as shown in the block numbered ⑤ in Fig. 7-2 and a normal VCO in a PLL loop is that the voltage and current ratings of the VCO formed by the autonomous push pull converter is much larger than those of normal VCOs in PLL control loops. Therefore, to insert the VCO formed by the autonomous push pull converter into a PLL loop, voltage and current matching circuits are needed before and after this special VCO as shown by the two red-coloured boxes numbered ① and ④, respectively, in Fig. 7-2.

With the autonomous push pull converter modified into a VCO, the five circuit blocks numbered ①, ②, ③, ④ and ⑤, respectively as shown in Fig. 7-2, constitute a PLL loop. The frequency of the VCO numbered ⑤ in Fig. 7-2 (actually the autonomous push pull converter) can be adjusted dynamically to stabilize at the “reference frequency” input into the phase detector numbered ② as shown in Fig. 7-2. The block diagram under the thick black line in Fig. 7-2 shows a typical PLL control loop for comparison, from which it can be seen that the only difference between the typical PLL loop and the PLL loop to stabilize the frequency of the autonomous push pull converter is that two voltage and current matching circuits as shown by the two red-coloured boxes numbered ① and ④, respectively, are needed by the later to solve the problem of voltage and current matching so that the high voltage and current VCO formed by the autonomous push pull converter can be fitted into a normal, low power PLL control loop.

The voltage and current matching circuits as shown by the two red-coloured boxes numbered ① and ④ in Fig. 7-2 can be realized in a variety of ways as detailed in the next section.

7.3 Circuit Design

The part of the circuit numbered ⑤ in Fig. 7-2 (the VCO) can be realized by any of the circuits introduced in chapters 4, 5 and 6 (not necessarily only the one shown in Fig. 7-2), as long as the frequency of the circuit can be controlled by a DC voltage so that it functions like a VCO. The one shown in Fig. 7-2 is only one example of them. As they have been discussed in details in the previous chapters, their design will not be repeated here. Similarly, the parts of the circuits numbered ② and ③ respectively in Fig. 7-2 are only common components of a PLL control loop, so their design will not be discussed in detail in this thesis neither because there is nothing special with the PD and LF here compared to the PD and LF used extensively in PLL control loops in low power signal processing circuits. In the practical circuit experiments in this chapter, phase comparator 2 of the PLL chip CD4046BE is used for the
Chapter 7: Stabilizing the ZVS Frequency of Autonomous Push Pull Converter by PLL Control

PD, and there are technical details in the datasheet of CD4046BE for the design of the corresponding LF. The focus of this section will be placed on the design of the two voltage and current matching circuits represented by the two red-coloured blocks numbered ① and ④ respectively in Fig. 7-2, because they are unusual in the whole circuit structure compared to a common PLL control loop widely used in low power signal processing circuits.

7.3.1 The Voltage Matching Circuit before the PD

The function of the part of the circuit numbered ① in Fig. 7-2 is to monitor the real operating frequency of the autonomous push pull converter continuously and output a voltage signal with the same frequency as that of the converter but the amplitude is low enough to be input into the PD after it. Fig. 7-3 shows one realization of the voltage matching circuit numbered ① in Fig. 7-2. \( v_a \) and \( v_b \) are the voltages at the two points “a” and “b” of the resonant tank of the autonomous push pull converter as shown in Fig. 7-2. The function of the four resistors \( R_1, R_2, R_3 \) and \( R_4 \) in Fig. 7-3 is to reduce the level of the two voltages \( v_a \) and \( v_b \) within the input voltage range of the comparator \( U_c \) so that they can be input into the comparator. The comparator \( U_c \) compares the difference between the two voltages \( v_a \) and \( v_b \), and outputs a square wave with the same frequency as that of the resonant tank of the converter.

![Fig. 7-3. The voltage matching circuit numbered ① in Fig. 7-2.](image)

The square wave from \( U_c \) is fed into the PD (the circuit block numbered ② in Fig. 7-2). The PD compares this square waveform with a reference frequency, and combined with the Low-pass Filter (LF), outputs a voltage finally from the LF which changes according to the difference between the frequencies of the two input signals into the PD. The output voltage from the LF changes between 0 and 5 V which is not high enough to be used as the
controlling voltage for the T-DCVC in the resonant tank of the autonomous push pull converter, which needs to be at the same level of the peak value of the voltage of the resonant tank to control the diode in the T-DCVC to be always conducting or never conducting. When the controlling voltage is at this level, the adjustable range of the equivalent capacitance of the T-DCVC and the frequency of the converter reach their maximum values. Depending on the fluctuation range of the frequency, the maximum value of the controlling voltage can be designed lower than the peak value of the voltage of the resonant tank as long as the fluctuating frequency can be adjusted back to the reference frequency. The general principle for determining the maximum value of the controlling voltage is that the higher the controlling voltage is, the larger the adjustable range of the frequency. Another factor which has an influence on the design of the maximum value of the controlling voltage is the resistance of the base resistor $R_b$ as shown in the circuit block numbered ⑤ in Fig. 7-2. The larger the resistance of $R_b$ is, the less the influence of the controlling voltage is on the equivalent capacitance of the T-DCVC and the frequency of the converter.

7.3.2 The Voltage and Current Matching Circuits after the LF

The task to amplify the voltage signal from the LF (which changes only between 0 to 5 V) in both voltage and current levels so that it becomes high enough to be used as the controlling voltage for the T-DCVC of the resonant tank of the autonomous push pull converter is fulfilled by the part of the circuit numbered ④ in Fig. 7-2. In addition to amplifying the voltage and current levels of the output signal from the LF, another function of the voltage and current matching circuit numbered ④ in Fig. 7-2 is to invert the phase of the voltage signal from the LF, which means that the output voltage of the voltage and circuit matching circuit numbered ④ in Fig. 7-2 should be inversely related to its input voltage. This is because the controlling voltage is reversely related to the frequency of the autonomous push pull converter; however, the PLL chip used in the experiment (CD4046BE) requires a positive relationship between its output voltage and the frequency of its VCO. This is guaranteed after the voltage is inverted twice, i.e. the inversion by the circuit block ④ and the inversion of the relationship between the frequencies of the autonomous push pull converter and the control voltage $V_c$. The functions of the voltage and current matching circuit numbered ④ in Fig. 7-2 can be realized in a variety of ways as shown in Fig. 7-4, 7-5 and 7-7, respectively.
Chapter 7: Stabilizing the ZVS Frequency of Autonomous Push Pull Converter by PLL Control

The circuit shown in Fig. 7-4 is the simplest realization of the voltage and current matching circuit block numbered ④ in Fig. 7-2. Both of the two tasks of voltage amplification and phase inversion are fulfilled by the transistor Q1 while the function of the transistor Q2 is to fulfil the task of current amplification.

Fig. 7-4. The first realization of the voltage and current matching circuit numbered ④ in Fig. 7-2.

Fig. 7-5 shows another realization of the voltage and current matching circuit block numbered ④ in Fig. 7-2. It centres on the programmable precision voltage reference chip TL431 (T1 as shown in Fig. 7-5) so that the output voltage $V_c$ is more stable than the method as shown in Fig. 7-4. The transistor Q1 in Fig. 7-5 works in linear mode and functions as a variable resistor controlled by the input voltage $V_{LP}$. The function of the transistor Q2 in Fig. 7-5 is to increase the output range of the current of TL431. When the part of the circuit consisted of R7, R8, R9 and Q1 is replaced by the variable resistor R2 (the two resistors R10 and R11 are replaced by R3 and R1 respectively at the same time) and the transistor Q2 is deleted, the circuit shown in Fig. 7-5 is transformed to the one shown in Fig. 7-6, which is
one of the typical application circuits of the programmable precision voltage reference chip TL431.

![Fig. 7-6. One application example of TL431.](image)

The output voltage $V_{KA}$ of the circuit shown in Fig. 7-6 is given by (7-1):

$$V_{KA} = V_{ref} \cdot \left(1 + \frac{R_1}{R_2}\right) + I_{ref} \cdot R_1$$  \hspace{1cm} (7-1)

Choosing different values of $R_1$ and $R_2$, the output voltage $V_{KA}$ can be adjusted between $2.5V \sim 36V$. The value of the current limiting resistor $R_3$ should guarantee that the cathode current $I_k$ is between 1 to 100mA as required by the operating condition of the chip TL431. Two modifications have been made to the circuit shown in Fig. 7-6 for it to become the one shown in Fig. 7-5 so that its output voltage $V_{KA}$ changes with the output voltage of the LF $V_{LP}$ and can output a current big enough to drive the T-DCVC in the resonant tank of the autonomous push pull converter. Firstly, as the output current of TL431 is limited, the transistor $Q_2$ is added (refer to Fig. 7-5) to increase the output current. Secondly, to make the output voltage $V_{KA}$ change with the output voltage of the LF $V_{LP}$ and fulfil the task that there should be a reverse relationship between the input and output voltages, the resistor $R_2$ in Fig. 7-6 is replaced by the PNP transistor $Q_1$ in Fig. 7-5, which acts as a variable resistor controlled by its base voltage. The higher its base voltage is, the larger its resistance. As can be seen from formula (7-1), the larger the resistance of $R_2$ is, the smaller the output voltage $V_{KA}$ of TL431 will be, so finally there will be a reverse relationship between the base voltage of $Q_1$ and the output voltage $V_{KA}$ because the higher the base voltage of $Q_1$ is, the larger its resistance, and the larger its resistance, the smaller the output voltage $V_{KA}$ of TL43. The
function of the two resistors of R7 and R8 is to transform the output voltage of the LF from changing between 0 and 5V to changing roughly between 0 and 2.5V so that the base voltage of Q1 will not go higher than 2.5V. The reason for this is that the reference pin of TL431 which connects to the emitter of Q1 is normally at 2.5V, so there is no use for the base voltage of Q1 to go beyond that value. Considering the voltage drop between the emitter and the base of Q1, it is found in the experiment that actually there is no use for the base voltage of Q1 to go higher than 2.2V. The base current limiting resistor R9 should have a large value so that the voltage between R7 and R8 is influenced as less as possible by a big base current of the transistor Q1.

Fig. 7-7 shows the third method to realize the voltage and current matching circuit numbered ④ in Fig. 7-2. It is based on the inverting amplifier circuit to fulfil the task of voltage amplification and phase inversion. The function of the transistor Q1 is to increase the output current of the circuit. To guarantee the output voltage is positive, the non-inverting input of the op-amp Ua is connected to a positive reference voltage instead of ground. The output voltage of the inverting amplifier is expressed by (7-2):

$$V_o = V_{ref} \cdot \frac{(R_1 + R_f)}{R_1} - V_{LP} \cdot \frac{R_f}{R_1}$$

(7-2)

For the output voltage of the inverting amplifier $V_o$ to stay always positive, the reference voltage input into the non-inverting terminal of Ua should meet the requirement expressed by (7-3):

$$V_{ref} \geq V_{LP} \cdot \frac{R_f}{R_1 + R_f}$$

(7-3)
Fig. 7-8 shows the waveforms of $V_{LP}$ (green) and $V_O$ (blue) when the input signal $V_{LP}$ is a sine wave, from which it can be seen that $V_O$ is an amplified version of $V_{LP}$ with the phase inverted, and most importantly $V_O$ is always positive instead of negative as in a common inverting amplifier because the non-inverting input of the amplifier is connected to a positive reference voltage instead of ground. The input and output waveforms of the circuits shown in Fig. 7-4 and Fig. 7-5 are similar to the one shown in Fig. 7-8.

As mentioned at the beginning of Section 7.3, phase comparator 2 of the PLL chip CD4046BE is used in the experiments for the PD, which has two inputs: SIG_IN and COMP_IN. When the frequency of SIG_IN is higher than that of COMP_IN, the output voltage from the LF increases, and vice versa. The frequency of the VCO in CD4046BE is positively related to the control voltage, i.e. the higher the control voltage, the higher the frequency. As a result, SIG_IN is usually used as the fixed reference frequency and COMP_IN is connected to the output of the VCO. In this way, the higher the frequency of the VCO, the lower the voltage from the LF becomes so that the frequency of the VCO becomes lower when the voltage from the LF is used to control the frequency of the VCO. This is the case for the three methods as shown in Fig. 7-4, 7-5 and 7-7, i.e. the frequency from the VCO (the autonomous push pull converter here) is connected to the COMP_IN terminal of the PD of CD4046BE while the SIG_IN terminal is connected to the reference frequency. As the frequency of the autonomous push pull converter is inversely related to the control voltage $V_c$ instead of positively related to the control voltage as in the case of the VCO within CD4046BE, the phases of the input and output voltages of the three methods as shown in Fig. 7-4, 7-5 and 7-7 need to be inversed. However, when the frequency from the VCO is input into the terminal SIG_IN while the reference frequency is connected to the terminal COMP_IN, the higher the frequency of the VCO, the higher the voltage from the LF will become. When the higher voltage from the LF is used to control the frequency of the VCO (the autonomous push pull converter here), the frequency of the VCO will become lower so
as to form a negative feedback control loop to keep the frequency of the VCO constant or follow the reference frequency. In this way, the phase of the input and output of the voltage and current matching circuit as shown by the block numbered ④ in Fig. 7-2 do not need to be inversed. This case is shown in Fig. 7-9.

![Fig. 7-9. The fourth realization of the voltage and current matching circuit numbered ④ in Fig. 7-2.](image)

As can be seen, the voltage and current matching circuit as shown by the block numbered ④ in Fig. 7-9 is a noninverting amplifier instead of an inverting amplifier as shown in Fig. 7-7. A transistor can be added at the output of the circuit block numbered ④ in Fig. 7-9 to increase the output current when needed similar to the case as shown in Fig. 7-7.

### 7.4 Experimental Results

Two different experiments are carried out. One is for low frequency and the other is for high-frequency as detailed below.

#### 7.4.1 Low frequency experiments

The low frequency experiments are based on the circuit as shown in Fig. 7-2. The two voltage and current matching circuit blocks numbered ① and ④, respectively, in Fig. 7-2 are based on the circuit as shown in Fig. 7-3 and Fig. 7-4, respectively. The two circuit blocks numbered ② and ③ in Fig. 7-2 are common PLL circuits as explained in the last section.

Fig. 7-10 shows the result of the low frequency experiment for the waveforms of the voltage at the point “a” of the resonant tank $v_a$, the controlling voltage $V_c$ and the reference frequency $f_{\text{ref}}$ of the PD of the circuit as shown in Fig. 7-2. The time scale of the plots in Fig. 7-10 is 2.00us as shown by the fifth term in the first line of the plots. The yellow waveform on the top is the voltage $v_a$, the green one in the middle is the control voltage $V_c$ and the purple square waveform at the bottom is the reference frequency input into the phase detector.
Chapter 7: Stabilizing the ZVS Frequency of Autonomous Push Pull Converter by PLL Control

Fig. 7-10. The waveforms of $v_a$ (yellow on the top), $V_C$ (green in the middle) and $f_{ref}$ (purple at the bottom) when $f_{ref}$ is set at 230kHz, 235kHz and 242kHz, respectively.

The experiment is carried out by changing the frequency of the reference signal. The three plots in Fig. 7-10 show the situations when the reference frequency is set at 230 kHz, 235
kHz and 242 kHz, respectively. The frequency of the voltage $v_a$ and the reference frequency are shown in the first and third position of the second line at the bottom of each plot, from which it can be seen that they are always the same, which means that the real operating frequency of the autonomous push pull converter (represented by the frequency of $v_a$) follows the frequency of the reference signal, or the frequency of the reference signal has a control over the real operating frequency of the converter. The second term in the same line as the frequencies in each plot shows the control voltage $V_c$, from which it can be seen that $V_c$ changes with the change of the frequency, specifically the higher $V_c$ is, the lower the operating frequency of the converter, which is in agreement with the conclusions drawn in chapters 4, 5 and 6. Actually, the fact is that the real operating frequency of the converter changes with the change of the control voltage $V_c$. The reference frequency controls the real operating frequency of the converter by adjusting the control voltage $V_c$ through the PLL control loop.

Fig. 7-11 shows the experimental results when the reference frequency is set at 240 kHz and a secondary coil is coupled to the primary coil (the inductor $L$ as shown in Fig. 7-2) at different distances. As is well known, the frequency of the converter will change greatly at such situations if there is no controller to control the frequency. However, it can be seen from Fig. 7-11 that the frequency of converter does not change but firmly follows the 240 kHz reference frequency. Nevertheless, although the frequency does not change, the controlling voltage $V_c$ does change meaning that the controller is making the frequency constant by adjusting the controlling voltage $V_c$. 
Fig. 7-11. The waveforms of $v_a$ (yellow on the top), $V_c$ (green in the middle) and $f_{\text{ref}}$ (purple at the bottom) when $f_{\text{ref}}$ is set at a fixed value of 240kHz but the coupling coefficient between the primary and secondary coil changes.
Similar experiments have also been carried out with the reference frequency $f_{\text{ref}}$ set at other values such 235 kHz, 230 kHz, etc. The results are the same, meaning that the frequency of the converter does not change, but the controlling voltage $V_c$ changes to make the frequency of the converter constant. In conclusion, it can be seen from the experiments that when the frequency of the converter fluctuates due to some disturbance, the PLL control loop can draw it back to the reference frequency by changing the controlling voltage $V_c$.

### 7.4.2 High-frequency Experiments

As shown in Fig. 7-12, the high-frequency experiments are based on circuit Fig. 4-1 of chapter 4 and the PLL controller introduced in this chapter. As explained in Chapter 4, the frequency of this circuit can go to very high levels because it does not include an external capacitor in the resonant tank, instead only parasitic capacitances of the circuit are employed as resonant capacitors.

The capacitors $C_{\text{ds1}}$, $C_{\text{gd1}}$, $C_{\text{gs1}}$, $C_{\text{gd2}}$, $C_{\text{gs2}}$ and $C_{\text{ds2}}$ in Fig. 7-12 are parasitic capacitances of the two power MOSFET switches $S_1$ and $S_2$, respectively. The main parameters and components used in the experiments are shown in Table 7-1.
Table 7-1. Parameters and components used in the experiments.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DC} (V)</td>
<td>10</td>
</tr>
<tr>
<td>L1, L2 (mH)</td>
<td>1</td>
</tr>
<tr>
<td>L (uH)</td>
<td>2.34</td>
</tr>
<tr>
<td>S1, S2</td>
<td>Q3</td>
</tr>
<tr>
<td>D1, D2</td>
<td>Rb3</td>
</tr>
<tr>
<td>Q1, Q2</td>
<td>Rb1, Rb2 (Ω)</td>
</tr>
<tr>
<td>BC547</td>
<td>BC547</td>
</tr>
<tr>
<td>Rb3</td>
<td>330k</td>
</tr>
<tr>
<td>Rc3</td>
<td>7.2k</td>
</tr>
</tbody>
</table>

Fig. 7-13 shows the high-frequency experimental results for the waveforms of the voltage at the point “A” of the resonant tank $v_A$, the controlling voltage at the output of the circuit block numbered ④ $v_c$ and the reference frequency input into the phase detector as shown by the circuit block 2 in Fig. 7-12-$f_{ref}$. 
Chapter 7: Stabilizing the ZVS Frequency of Autonomous Push Pull Converter by PLL Control

Fig. 7-13. The waveforms of $v_A$ (yellow, on the top), $V_C$ (green, in the middle) and $f_{ref}$ (purple, at the bottom) when $f_{ref}$ is set at 10MHz, 9MHz, 8MHz, 7.4MHz and 7MHz, respectively.
Chapter 7: Stabilizing the ZVS Frequency of Autonomous Push Pull Converter by PLL Control

The voltage $v_A$ represents the frequency of the converter. It can be seen from Fig. 7-13 that the frequency of the converter and the reference frequency $f_{ref}$ are always the same, which means the frequency of the converter follows the reference frequency, or the reference frequency has a control over the frequency of the converter.

The time scale of the plots in Fig. 7-13 is 100.0ns as shown by the fifth term in the first line of the plots. The yellow waveform on the top is the voltage $v_A$, the green one in the middle is the control voltage $V_c$ and the purple square waveform at the bottom is the reference frequency $f_{ref}$ input into the phase detector. The experiment is carried out by changing the frequency of the reference signal. The five plots in Fig. 7-13 show the situations when the reference frequency is set at 10MHz, 9MHz, 8MHz, 7.4MHz and 7MHz, respectively. The frequency of the voltage $v_A$ and the reference frequency are shown at the bottom-right corners of the plots represented by Freq [1] and Freq [3], respectively, from which it can be seen that they are always the same, which means that the real operating frequency $v_A$ of the autonomous push pull converter (represented by Freq [1]) follows the frequency of the reference signal (Freq[3]), or the frequency of the reference frequency has a control over the real operating frequency of the converter. The third term in the “Measurements” region at the bottom-right corner of each plot shows the average of the control voltage $V_c$ represented by “Avg - FS [2]”. As the value of the control voltage is not only decided by the output voltage of the low pass filter- the circuit block numbered ③ in Fig. 7-12, but also influenced by the voltages on the gates of the two power MOSFET switches which are half sinusoidal waves, it can be seen from Fig. 7-13 that $V_c$ is not an absolute DC voltage.

Besides that the frequency of the converter follows the frequency of the reference frequency, another important feature which can be seen from Fig. 7-13 is that the control voltage $V_c$ changes with the change of the frequency, specifically the higher $V_c$ is, the lower the operating frequency of the converter, which is in agreement with the practical experimental results as shown by Fig. 4-27 in Chapter 4. Actually, the fact is that the real operating frequency of the converter changes with the change of the control voltage $V_c$. The reference frequency controls the real operating frequency of the converter by adjusting the control voltage $V_c$ through the PLL control loop.
Chapter 7: Stabilizing the ZVS Frequency of Autonomous Push Pull Converter by PLL Control
Chapter 7: Stabilizing the ZVS Frequency of Autonomous Push Pull Converter by PLL Control

Fig. 7-14 shows the experimental results when the reference frequency is set at 6.8 MHz and a secondary coil is coupled to the primary coil (the inductor L as shown in Fig. 7-12) at different distances.

As is well known, the frequency of the converter will change greatly at such situations if there is no control over the frequency of the converter. However, it can be seen from Fig. 7-14 that the frequency of the converter does not change at all but firmly follows the 6.8 MHz reference frequency. Nevertheless, although the frequency remains constant at 6.8 MHz, it can be seen from Fig. 7-14 that the control voltage $V_c$ in different plots of Fig. 7-14 are different, specifically they are 17.009V, 12.524V, 8.467V and 4.497V from the first to the last plot of Fig. 7-14, which means that the controller is making the frequency constant by adjusting the control voltage $V_c$.

7.5 Summary

One of the most important applications of the methods for controlling the frequency of the autonomous push pull converter with a DC voltage presented in previous chapters is to combine them with the PLL technology to stabilize the frequency of high power DC-AC converters by dynamically adjusting the equivalent capacitance of the resonant tank of the converter. The main topic of this chapter is the design of concrete PLL controllers to realize this goal. The overall strategy and major difference between a PLL controller used for this purpose and a common PLL controller used in low power signal processing circuits are
Chapter 7: Stabilizing the ZVS Frequency of Autonomous Push Pull Converter by PLL Control

presented in Section 7.2. The design of different circuit blocks of the PLL controller, especially those which are different from a common PLL control loop, i.e. the voltage and current matching circuits, are discussed in detail in Section 7.3. One method to realize the voltage matching circuit before the phase detector and four methods to realize the voltage and current matching circuit after the low pass filter of the PLL control loop are presented. The principles and reasons for designing the voltage and current matching circuits after the low pass filter are discussed in detail. The validity of the method and concrete circuit blocks were proved with practical circuit experiments in Section 7.4. The experiments were carried out for both low frequency (a few hundred kHz) and high-frequency (MHz level) applications, proving that the frequency of the converter can be stabilized or adjusted flexibly by the PLL controller.
Chapter 8: Output Voltage Regulation of Wireless Power Pick-ups by T-DCVC

8.1 Introduction

Chapter 7 was about the application of the DCVCs at the primary side of an IPT system for stabilizing the operating frequency when combined with the PLL technology. This chapter is to propose an output voltage regulation method based on T-DCVC. R-DCVC may also be used for the purpose, but because it needs a larger control current which may be difficult to supply from a power pickup, so only T-DCVC is studied in this chapter. The secondary side of an IPT system is tuned/detuned by a variable capacitor of DCVC to control the power flow and stabilize the output voltage. Both parallel and serial tuning options are studied at the secondary side of an IPT system for this purpose. This chapter is organized as follows. Section 8.1 is the Introduction. Section 8.2 presents the method where the T-DCVC is used as a parallel tuning capacitor. Section 8.3 describes the method for using the T-DCVC as a serial tuning capacitor. Finally a summary is made in Section 8.4.

8.2 The Parallel Tuning Method

There are generally two approaches to adjusting the output voltage of the secondary side of an IPT system. One is to control the output voltage from the primary side [75, 253, 254], and the other from the secondary side [21, 24, 118, 255]. The latter is relatively more straightforward than the former because a separate communication channel is normally needed to control the output voltage of the secondary side from the primary side. A simple way to adjust the output voltage directly from the secondary side is to use an active switch [21, 24, 118], which generates switching noises and causes ripples at the output because of switching. An alternative method is proposed by Kumar and Hu [255] which does not use
Chapter 8: Output Voltage Regulation of Wireless Power Pick-ups by T-DCVC

switches but simply employs a variable resistor formed by operating a power transistor in the linear region. It has the advantage of smooth power regulation and lower EMI, but the adjustable range is limited.

This section proposes a new method for adjusting the output voltage directly from the secondary side through the \( T-DCVC \) presented in Chapter 6, based on the principle of tuning and detuning. As the equivalent capacitance of the \( T-DCVC \) can be controlled by a DC voltage, when it is used as a parallel tuning capacitor at the secondary side of an IPT system, the output voltage can be controlled by this DC voltage through the effect of tuning and detuning. Additionally, a simple PI controller can be employed to conveniently generate the controlling DC voltage to make the output voltage constant. As there is no active switch used in the \( T-DCVC \) it has no switch driving problems, such as the need of a high up-to-20V voltage source, which is particularly advantageous for its application at the secondary side of an IPT system. The \( T-DCVC \) also has the potential to be used at much higher frequencies than traditional switch mode capacitors because of the smoothness of the adjustment of its equivalent capacitance through a DC voltage. The basic operating principle of the method is explained in Section 8.2.1. Section 8.2.2 provides deeper theoretical analysis by simulation study. Section 8.2.3 provides the practical experimental results and conclusions are presented in Section 8.2.4.

8.2.1 Basic Operating Principle of the Parallel Tuning Method

Fig. 8-1 shows the IPT system where the \( T-DCVC \) is used as a parallel tuning capacitor at the secondary side of the system.

![Fig. 8-1. The parallel tuning method to regulate the output voltage.](image)

To concentrate on studying the performance and characteristics of the secondary side circuit, the primary side uses simply power amplifier \( v_s \) to generate a sinusoidal current at a fixed
frequency to drive the primary coil $L_p$. The secondary side is a parallel-tuned half-bridge regulation circuit, in which the $T-DCVC$, comprised of $C_{up}$, $C_{dw}$, $D_c$, $Q_c$ and $R_b$, is added in parallel with the normal fixed value parallel tuning capacitor $C_s$. The average equivalent capacitance of the $T-DCVC$ can be controlled by the voltage $V_c$ because $V_c$ controls the conduction period of the diode $D_c$. When $D_c$ conducts, the equivalent capacitance of the $T-DCVC$ is $C_{up}$ and when $D_c$ is off, the equivalent capacitance of the $T-DCVC$ is $C_{up}$ and $C_{dw}$ in series. The output voltage $V_{out}$ changes with the variation of the equivalent capacitance of the $T-DCVC$ because of the effect of tuning and detuning.

As explained in Chapter 6, the voltage $V_c$ controls the conduction period of the diode $D_c$ through its influence on the base and collector currents $i_b$ and $i_c$ of the transistor $Q_c$. The higher $V_c$ is, the larger $i_b$ and $i_c$ will be, and the larger $i_c$ is, the lower the voltage across the diode $D_c$. The conduction period $T_{con}$ of the diode $D_c$ increases with the decrease of the voltage across it. In brief, $V_c$ controls the equivalent capacitance of the $T-DCVC$ and the output voltage $V_{out}$ by adjusting the conduction period $T_{con}$ of the diode $D_c$ through its influence on $i_b$, $i_c$ and the voltage across the diode $D_c$.

### 8.2.2 Theoretical Analysis and Simulation Study

Fig. 8-2 shows the simulated waveforms of the voltage across the diode $D_c$-$v_{DC}$, the collector current of the transistor $Q_c$-$i_c$ and the current of the diode $D_c$-$i_{DC}$ when the control voltage $V_c$ is set at 1V (Fig. 8-2 (a), (b), (c)) and 10V (Fig. 8-2 (d), (e), (f)), respectively. It can be seen from Fig. 8-2 that the higher the control voltage $V_c$ is, the higher $i_c$, the lower $v_{DC}$ and the longer the diode $D_c$ conducts, which can be seen from the conduction period $T_{con}$ during which $i_{DC}$ is not zero. Another important feature that can be seen from Fig. 8-2 is that the transition condition of the state of the diode $D_c$ is very favorable because both of the current $i_{DC}$ and the voltage $v_{DC}$ are zero when the diode $D_c$ turns on and off, which makes the switching noise of the proposed method much lower than that of traditional methods using active switches. Moreover, as the switching of the diode can be controlled smoothly with a DC voltage, the proposed method has the potential to be applied to much higher frequencies than traditional switch mode capacitors which use active switches controlled by PWM signals.
8.2.3 Experimental Results

Fig. 8-3 shows the experimental setup.

Table 8-1 show the components and parameters of the circuit used in the experiments.

<table>
<thead>
<tr>
<th>Frequency (kHz)</th>
<th>Lp (uH)</th>
<th>Ls (uH)</th>
<th>Cs (nF)</th>
<th>Cup (nF)</th>
<th>Cdw(nF)</th>
<th>Dc</th>
</tr>
</thead>
<tbody>
<tr>
<td>290</td>
<td>24.6</td>
<td>10.1</td>
<td>100</td>
<td>100</td>
<td>10</td>
<td>BYV26C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>k</th>
<th>Qc</th>
<th>Rs (Ω)</th>
<th>D1</th>
<th>C_f (μF)</th>
<th>R_load(Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.77</td>
<td>KSE13003</td>
<td>360</td>
<td>BYV28</td>
<td>10</td>
<td>3.3</td>
</tr>
</tbody>
</table>
Fig. 8-4 shows the open-loop experimental relationship between the output voltage $V_{\text{out}}$ and the control voltage $V_{c}$ under different values of the base resistor $R_{b}$, from which it can be seen that $V_{\text{out}}$ and $V_{c}$ are negatively related to each other, and at the same value of $V_{c}$, the smaller $R_{b}$ is, the lower the output voltage meaning the stronger the influence of $V_{c}$ to $V_{\text{out}}$.

![Fig. 8-4. Experimental relationships between $V_{\text{out}}$ and $V_{c}$ with $R_{b}$ at different values.](image)

Fig. 8-5 shows the transient experimental waveforms of the output voltage $V_{\text{out}}$ (yellow on the top) and the control voltage $V_{c}$ (green at the bottom) at the moment when the load is changed suddenly from about 3.3Ω to 5.3Ω with the PI controller is working. It shows that the control voltage can respond immediately to keep the output voltage constant when load changes occur. In the experiments, the output voltage can be stabilized between 5V and 5.5V with the load resistance and the coupling coefficient $k$ changes between 3.3Ω and 5.3Ω (output power between 7.6W and 5.7W), and 0.77 and 0.67 respectively. The experiments are carried out
with Qi standard coils at low frequencies to show its practical application. However, the method itself has the potential to be used at much higher frequencies than traditional methods using active switches because of its smooth control of the switching of the diode and the output voltage with a DC voltage instead of a PWM signal.

8.3 The Serial Tuning Method

Last section is about the situation when the T-DCVC is used as a parallel tuning capacitor. As the experiments prove, the parallel tuning method is more suitable for small load resistance of a few ohms (3.3Ω~5.3Ω in the experiments) and low output voltage (5V in the experiments) when maximum output power is achieved. This section presents the situation when the T-DCVC is used as a serial tuning capacitor, which is more suitable for larger load resistance (100Ω in the experiments) and higher output voltage (24V in the experiments) when maximum output power is achieved as proved in the experiments.

8.3.1 Basic Operating Principle of the Serial Tuning Method

Fig. 8-6 shows the situation the T-DCVC is used as a serial tuning capacitor to stabilize the output voltage of the secondary side of an IPT system when combined with a PI controller. Similar to the parallel tuning situation in the last section, to concentrate on studying the performance and characteristics of the T-DCVC at the secondary side, the primary side circuit uses simply a power amplifier $v_s$ to generate a sinusoidal current at a fixed frequency to drive the primary side coil $L_p$.

![Fig. 8-6. The serial tuning method to regulate the output voltage.](image)
Chapter 8: Output Voltage Regulation of Wireless Power Pick-ups by T-DCVC

The secondary side of the system is a series-tuned half-bridge rectification pick-up with the common fixed-value tuning capacitor replaced by the T-DCVC comprised of $C_{up}$, $C_{dw}$, $D_c$, $Q_c$ and $R_b$ as shown in the dashed block of Fig. 8-6. The capacitance of this T-DCVC is $C_{up}$ when the diode $D_c$ is on, and $C_{up}$ and $C_{dw}$ in series when the diode $D_c$ is off, because when $D_c$ is on, the capacitor $C_{dw}$ and transistor $Q_c$ are short-circuited by the conducting diode, and when $D_c$ is off, it can be regarded as open so that $C_{up}$ and $C_{dw}$ becomes in series. As the capacitance of $C_{up}$ is larger than the capacitance of $C_{up}$ and $C_{dw}$ in series, the longer the diode conducts, the larger the average equivalent capacitance of the T-DCVC will be, which changes between $C_{up}$ and the value of $C_{up}$ and $C_{dw}$ in series according to the conduction period $T_{con}$ of the diode $D_c$.

The conduction period $T_{con}$ of the diode $D_c$ can be controlled by the voltage $V_c$ through its influence on the base and collector currents $i_b$ and $i_c$ of the transistor $Q_c$. The collector current $i_c$ of the transistor $Q_c$ in turn affects the voltage across the diode $D_c$. The higher $V_c$ is, the larger $i_b$ and $i_c$, and the larger $i_c$ is, the lower the voltage across the diode $D_c$ because $i_c$ plays the role to pull the voltage on the cathode of the diode down to the ground. Lower the voltage across the diode $D_c$ leads to longer conduction period $T_{con}$ of the diode and larger equivalent capacitance of the T-DCVC.

In brief, the voltage $V_c$ influences the equivalent capacitance of the T-DCVC by controlling the conduction period $T_{con}$ of the diode $D_c$ through its influence on $i_b$, $i_c$ and the voltage across the diode $D_c$. The higher $V_c$ is, the longer the diode conducts and the larger the average equivalent capacitance of the T-DCVC.

As is well-known, the output voltage changes with the variation of the tuning capacitance and there is a value for the tuning capacitance ($C_{max}$) at which the output voltage reaches its maximum. The relationship between the tuning capacitance and the output voltage is monotonic if the tuning capacitance changes between 0 and $C_{max}$, or $C_{max}$ and $\infty$. As the application of a PI controller to stabilize the output voltage by adjusting the equivalent capacitance of the T-DCVC requires that there is a monotonic relationship between the equivalent capacitance of the T-DCVC and the output voltage, the equivalent capacitance of the T-DCVC should be designed to vary within the range either higher or lower than $C_{max}$. Here, the tuning capacitance is designed to change between $C_{max}$ and $\infty$ by making the smallest value of the equivalent capacitance of the T-DCVC, i.e. $C_{up}$ and $C_{dw}$ in series, larger than $C_{max}$ so that the pickup circuit is always over tuned when the control voltage $V_c$ is not
zero. As the higher $V_c$ is, the larger the equivalent capacitance of the T-DCVC, higher $V_c$ leads to a lower output voltage.

### 8.3.2 Theoretical Modelling and Analysis

Fig. 8-7 shows the simplified equivalent circuit for the theoretical analysis.

![simplified equivalent circuit](image)

Fig. 8-7. The simplified equivalent circuit when the diode is on (a) and off (b), respectively.

As explained in the last section, the reason why the voltage $V_c$ can control the average equivalent capacitance of the T-DCVC is that $V_c$ influences the conduction period $T_{con}$ of the diode $D_c$. The relationship between $T_{con}$ and $V_c$ is therefore the basis of all the other relationships. To find the relationship between $T_{con}$ and $V_c$, the circuit is modelled as the ones shown in Fig. 8-7 (a) and (b), which represent the two situations when the diode is on and off, respectively, where $v_{ss}$ represents the voltage induced in the pick-up coil $L_s$, and the original rectification circuit, the filter capacitor $C_f$, and the DC load $R_{load}$ are simplified together as an AC load $R_{ac}$.

Fig. 8-8 shows the typical waveforms of $v_{ss}$, $i_s$, $v_{CdW}$ and $i_{Dc}$ (the current flowing through the diode $D_c$), from which it can be seen that the current $i_s$ is zero at the moments “$t_{off}$” when the diode stops conducting, and the voltage $v_{CdW}$ is zero at both of the two moments “$t_{on}$” and “$t_{off}$” when the diode $D_c$ starts and stops conducting, which means that it is ZVS when the diode turns on and both ZVS and zero current switching (ZCS) when it turns off.

To find the relationship between $T_{con}$ and $V_c$, two exact moments, i.e. the moment the diode starts to conduct “$t_{on}$” and the moment the diode stops to conduct “$t_{off}$” need to be determined first. Then, $T_{con}$ can be calculated with (8-1):
Chapter 8: Output Voltage Regulation of Wireless Power Pick-ups by T-DCVC

\[ T_{\text{con}} = t_{\text{off}} - t_{\text{on}} \]  

(8-1)

Fig. 8-8. The typical wave forms of \( v_{ss}, i_s, v_{Cdw} \) and \( i_{Dc} \).

The moment “\( t_{\text{off}} \)” can be found with the circuit when the diode is on as shown in Fig. 8-7 (a), where \( C_{dw}, D_c \) and \( Q_c \) are removed because an ideal conducting diode is equivalent to a short-circuit. The moment the diode stops to conduct “\( t_{\text{off}} \)” is regarded as when the current flowing through the diode at the moment-\( i_s \) drops to zero. Assume the voltage source \( v_{ss} \) is expressed by (8-2) (refer to Fig. 8-8 (a)).

\[ v_{ss} = V_m \cos \omega t \]  

(8-2)

The differential equation governing \( i_s \) is:

\[ L_s C_{up} \frac{d^2 i_s}{dt^2} + R_{ac} C_{up} \frac{di_s}{dt} + i_s = -C_{up} V_m \cos \omega t \]  

(8-3)

When \( R_{ac} > \frac{L_s}{2 \sqrt{C_{up}}} \), the full solution of (8-3) can be expressed by (8-4) (refer to Fig. 8-8 (b)).

\[ i_s = A_1 e^{p_1 t} + A_2 e^{p_2 t} + A \cos \omega t + B \sin \omega t \]  

(8-4)

where \( A_1 \) and \( A_2 \) are integral constants which need to be determined by the initial condition, and \( p_1, p_2, A \) and \( B \) are constants determined by the circuit parameters \( C_{up}, L_s, R_{ac} \) and \( v_{ss} \). It
can be seen from the typical waveforms as shown in Fig. 8-8 that $i_t$ is zero at the moment “$t_{off}$”, which can be expressed by:

$$0 = A_1 e^{p_1 t_{off}} + A_2 e^{p_2 t_{off}} + A \cos \omega t_{off} + B \sin \omega t_{off}$$  \hspace{1cm} (8-5)$$

Finally, $t_{off}$ can be derived approximately as expressed by (8-6) (as shown in Fig. 8-8).

$$t_{off} \approx \frac{\arcsin\left(\frac{-A_1 e^{p_1 t_{off}} - A_2 e^{p_2 t_{off}}}{\sqrt{A^2 + B^2}}\right)}{\omega} - \arctan\frac{B}{A}  \hspace{1cm} (8-6)$$

The moment “$t_{on}$” can be found with the circuit when the diode is off as shown in Fig. 8-7 (b), where the diode $D_c$ is removed because it amounts to an open-circuit when it is off, and the transistor $Q_c$ is modelled as a constant current source $i_c$ controlled by the voltage $V_c$ with the relationship:

$$i_c = \beta \cdot i_b = \beta \cdot \frac{V_c}{R_b}$$  \hspace{1cm} (8-7)$$

The moment the diode starts to conduct “$t_{on}$” is regarded as when the voltage across the diode $v_{C_{dw}}$ drops to zero. “$v_{C_{dw}}$” can be found by (8-8), where $K$ is the integral constant determined by the initial condition of the circuit.

$$v_{C_{dw}} = -\frac{1}{C_{dw}} \int i_{dw} + K$$  \hspace{1cm} (8-8)$$

The current flowing through the capacitor $C_{dw} i_{dw}$, is governed by (8-9):

$$L_s \frac{d^2 i_{dw}}{dt^2} + R_{load} \frac{di_{dw}}{dt} + \frac{C_{up} + C_{dw}}{C_{up} C_{dw}} i_{dw} = \frac{i_c}{C_{up}} - V_m \omega \sin \omega t  \hspace{1cm} (8-9)$$

When $R_{ac} > 2 \sqrt{\frac{L_s}{C_{updw}}}$, where $C_{updw} = \frac{C_{up} C_{dw}}{C_{up} + C_{dw}}$, the full solution of (8-9) is:

$$i_{dw} = A_1' e^{p_1 t} + A_2' e^{p_2 t} + \frac{C_{dw}}{C_{up} + C_{dw}} i_c + A' \cos \omega t + B' \sin \omega t  \hspace{1cm} (8-10)$$
Substituting (8-10) into (8-8) and calculate the indefinite integral of $i_{dw}$ gives:

$$v_{Cdw} = -\frac{1}{C_{dw}} \left( \frac{A'_1}{p_1} e^{p_1 t_{on}} + \frac{A'_2}{p_2} e^{p_2 t_{on}} + \frac{C_{dw}}{C_{up} + C_{dw}} i_c t + \frac{A'}{\omega} \sin \omega t - \frac{B'}{\omega} \cos \omega t \right) + K$$

(8-11)

where $A'_1$, $A'_2$ and $K$ are integral constants determined by the initial conditions of the circuit, and $p_1$, $p_2$, $A'$ and $B'$ are constants determined by the circuit parameters $C_{up}$, $L_s$, $R_{ac}$ and $v_{ss}$.

The waveform of $v_{Cdw}$ is shown in Fig. 8-8 (c), from which it can be seen that $v_{Cdw}$ is zero at the moment "$t_{on}$" when the diode starts to conduct, which can be expressed by:

$$0 = -\frac{1}{C_{dw}} \left( \frac{A'_1}{p_1} e^{p_1 t_{on}} + \frac{A'_2}{p_2} e^{p_2 t_{on}} + \frac{C_{dw}}{C_{up} + C_{dw}} i_c t_{on} + \frac{A'}{\omega} \sin \omega t_{on} - \frac{B'}{\omega} \cos \omega t_{on} \right) + K$$

(8-12)

Finally, from (8-12), $t_{on}$ can be derived as:

$$t_{on} \approx \frac{\arcsin - \frac{\omega}{\sqrt{A''^2 + B''^2}} \left( K \cdot C_{dw} - \frac{A'_1}{p_1} e^{p_1 t_{con}} - \frac{A'_2}{p_2} e^{p_2 t_{con}} - \frac{C_{dw}}{C_{up} + C_{dw}} i_c t_{con} \right) + \arctan \frac{B'}{A'}}{\omega}$$

(8-13)

With both of "$t_{off}$" and "$t_{on}$" available, $T_{con}$ can be calculated with (8-1). The moments of $t_{on}$, $t_{off}$ and the diode conduction period $T_{con}$ are shown in Fig. 8-8. The value of $i_s$ at the moment of $t_{off}$, and the values of $v_{Cdw}$ at the two moments of $t_{on}$ and $t_{off}$ can be used as part of the five initial conditions in finding the integral constants in (8-4) and (8-11).

### 8.3.3 Simulation Study

The components and parameters of the circuit used in the simulation are the same as those used in the practical experiments as shown in Table 8-2 of the next section. To reveal the principle that the higher the control voltage $V_c$ is, the higher $i_c$, and the higher $i_c$ is, the lower $v_{Cdw}$ and the longer the diode conducts, Fig. 8-9 shows the simulated waveforms of $i_c$, $v_{Cdw}$ and $i_{Dc}$ when the control voltage $V_c$ is 5V (Fig. 8-9 (a), (b) and (c)) and 20V (Fig. 8-9 (d), (e) and (f)), respectively, from which it can be seen that the amplitude of $i_c$ when $V_c$ is 20V is higher than that of the $i_c$ when $V_c$ is 5V; the amplitude of $v_{Cdw}$ when $V_c$ is 20V is lower than that of the $v_{Cdw}$ when $V_c$ is 5V, and conduction period $T_{con}$ when $V_c$ is 20V is longer than that of the $T_{con}$ when $V_c$ is 5V. Fig. 8-9 (g) shows the voltage $v_{Cdw}$ at the situation when the diode...
Chapter 8: Output Voltage Regulation of Wireless Power Pick-ups by T-DCVC

$D_c$, the transistor $Q_c$ and the base resistor $R_b$ are removed from the circuit with only the two capacitors $C_{up}$ and $C_{dw}$ left. Fig. 8-9 (h) shows the voltage $v_{Cdw}$ at the situation when the $v_{Cdw0}$ shown in Fig. 8-9 (g) is moved downwards along the Y-axis.

![Typical waveforms](image)

**Fig. 8-9. Typical waveforms $i_c$, $v_{Cdw}$ and $i_{Dc}$ when the control voltage $V_c$ is set at 5V and 20V, respectively, and when the diode and transistor are removed from the circuit.**

It can be seen from Fig. 8-9 (g) and (h) that after moved downwards, or the voltage is lowered, the length of the negative parts of the voltage (refer to Fig. 8-8 (c), the negative parts will be zero if a diode is present and the length of this part represents the conduction period $T_{con}$ of the diode) along the X-axis becomes longer ($T_{con0'} > T_{con0}$), which illustrates why when the amplitude of the voltage across the diode $D_c$ is lowered, its conduction period becomes longer. To sum up, the control voltage $V_c$ makes the conduction period of the diode $D_c$ become longer by making the voltage across the diode lower. As the conduction period $T_{con}$ of the diode $D_c$ plays a central role and is the fundamental reason why the control voltage $V_c$ can change the equivalent capacitance of the $T$-DCVC and the output voltage.
Fig. 8-10 shows the simulated relationship between $T_{con}$ and $V_c$ under different values of the base resistor $R_b$.

![Tcon vs. Vc](image.png)

**Fig. 8-10. The simulated relationships between $T_{con}$ and $V_c$ under different values of $R_b$.**

It can be seen from Fig. 8-10 that $T_{con}$ is proportionate to $V_c$, and at the same value of $V_c$, the smaller $R_b$ is, the larger the corresponding $T_{con}$, which means the stronger the influence of $V_c$ is on the conduction period of the diode. This is because that the smaller $R_b$ is, the larger the base and collector current $i_b$ and $i_c$ of the transistor $Q_c$. A higher $i_c$ pulls the level of the voltage across the diode lower so that the diode conducts longer. Actually, both $V_c$ and $R_b$ influence the diode conduction period $T_{con}$ through their impact on the base and collector currents $i_b$ and $i_c$.

![Vout vs. Vc](image.png)

**Fig. 8-11. The simulated relationship between $V_{out}$ and $V_c$ under different values of $R_b$.**

Fig. 8-11 shows the simulated relationships between the output voltage $V_{out}$ and the control voltage $V_c$ under different values of the base resistor $R_b$, from which it can be seen that higher $V_c$ leads to lower $V_{out}$, which is in consistent with the theoretical analysis in the last section and the simulation result shown in Fig. 8-9, from which it can be seen that higher $V_c$ leads to
longer $T_{\text{con}}$. As explained in Section 8.3.1, longer $T_{\text{con}}$ leads to larger equivalent capacitance of the $T$-DCVC which makes the pick-up circuit detuned more seriously and therefore the output voltage becomes lower.

Fig. 8-12 shows the simulated waveforms of the output voltage $V_{\text{out}}$, the control voltage $V_c$ when a simple PI controller is added to generate $V_c$ according to the fluctuation of the output voltage $V_{\text{out}}$ caused by the variation of the load resistance, which is controlled to change periodically between 50Ω and 100Ω with a switch. Fig. 8-12 (a), (b) and (c) show the output voltage $V_{\text{out}}$, control voltage $V_c$ and the switching signal $V_{\text{sw}}$, respectively, from which it can be seen that at the switching moments, the control voltage $V_c$ responds immediately to keep the output voltage constant at the designed value of 24V. The output voltage $V_{\text{out}}$ has only small fluctuations at the moments the load resistance is changed suddenly.

### 8.3.4 Experimental Results

Fig. 8-13 shows the experimental setup, which is the same as the one shown in Fig. 8-6, including the power amplifier $v_s$, the primary and secondary side coil $L_P$ and $L_S$, the series-tuned half-bridge rectification pick-up circuit with the $T$-DCVC as the tuning capacitor, the loads and the PI controller. Table 8-2 show the components and parameters of the circuit used in the simulation and experiments.

An open-loop experiment with the control voltage $V_c$ generated by a separate voltage source is carried out to find the relationship between the output voltage $V_{\text{out}}$ and $V_c$ under different values of the base resistor $R_b$. The result is shown in Fig. 8-14, which agrees well with the simulation results as shown in Fig. 8-11.
Table 8-2. Components and parameters of the circuit used in the simulation and experiments.

<table>
<thead>
<tr>
<th>Frequency of $v_s$ (kHz)</th>
<th>$Lp$ (uH)</th>
<th>$Ls$ (uH)</th>
<th>$C_{up}$ (nF)</th>
<th>$C_{dw}$ (nF)</th>
<th>$D_c$, $D1$, $D2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>290</td>
<td>24</td>
<td>10</td>
<td>20</td>
<td>20</td>
<td>BYV26C</td>
</tr>
<tr>
<td>Amplitude of $v_s$ (V)</td>
<td>$k$</td>
<td>$Q_c$</td>
<td>$R_b$ (kΩ)</td>
<td>$C_f$ (uF)</td>
<td>$R_{load}$ (Ω)</td>
</tr>
<tr>
<td>15</td>
<td>0.66</td>
<td>KSE13003</td>
<td>3.9</td>
<td>10</td>
<td>100</td>
</tr>
</tbody>
</table>

Fig. 8-14. Experimental relationships between $V_{out}$ and $V_c$ with $R_b$ at different values.

It can be seen from Fig. 8-14 that the output voltage changes greatly (about 12 volts, roughly from 21V to 33V) with the change of the control voltage $V_c$. Another feature that can be seen from Fig. 8-14 is that the smaller $R_b$ is, the sharper the output voltage changes with the change of the control voltage $V_c$. This is because that the smaller $R_b$ is, the more influence the control voltage $V_c$ has on the collector current $i_c$, the voltage across the diode $D_c$ and conduction period $T_{con}$ of the diode. $R_b$ should be designed to be small enough to make $V_c$ have sufficient control over the output voltage so that the adjustable range of the output.
voltage is large enough. Within the adjustable range of the output voltage, larger $R_b$ makes the system more stable.

A separate experiment with the PI controller added is carried out to test the closed-loop performance of the proposed method. The output voltage $V_{out}$ is designed to be 24V and is used as the voltage source of the PI controller directly in the experiment. Fig. 8-15 shows the transient experimental waveforms of the output voltage $V_{out}$ (yellow on the top) and the control voltage $V_c$ (green below) at the moment when the load is changed suddenly from about 50Ω to 100Ω, from which it can be seen that the control voltage can respond immediately to keep the output voltage constant when load changes occur. The power transferred varies between 11.52W ~ 5.76W with the load resistance changing between 50Ω and 100Ω and the output voltage kept consistent at 24V.

In addition to the changes of the load, the output voltage can also be kept stabilized between 23.5 V and 24.5 V with the coupling coefficient $k$ between $L_p$ and $L_s$ changing between 0.57 and 0.66 in the experiment.

### 8.4 Summary

This chapter presented the application of the $T$-$DCVC$ to the secondary side of an IPT system to stabilize the output voltage by tuning/detuning. The main characteristic of the $T$-$DCVC$ is that its equivalent capacitance can be controlled smoothly by a DC voltage, which has
already been studied in detail in Chapter 6. When the $T$-$DCVC$ is used as a resonant capacitor in the secondary side of an IPT system, the output voltage of the pick-up circuit can be controlled by adjusting the equivalent capacitance of the $T$-$DCVC$ through the controlling DC voltage. The controlling DC voltage can be generated by a PI controller, which monitors the fluctuation of the output voltage, varies the controlling DC voltage and the equivalent capacitance of the $T$-$DCVC$ accordingly to keep the output voltage constant. The $T$-$DCVC$ can be used either as a parallel or serial tuning capacitor, and it was proved in the experiments that both can work very well. The difference is that they are suitable for different situations. The experiments proved that the parallel tuning method is more suitable for small load resistance and low output power applications (3.3Ω–5.3Ω and 5V in the experiments) when maximum output power is achieved. The serial tuning method is better suited for larger load resistance and higher output voltage (100Ω and 24V in the experiments) when maximum power transfer is achieved. As there is no active switch used in the $T$-$DCVC$, compared to traditional switch mode capacitors the $T$-$DCVC$ has no switch driving problems such as a separate high up-to-20V gate driving voltage source for the switches used. This is particularly advantageous for its application at the secondary side of an IPT system. The $T$-$DCVC$ also has the potential to be used at much higher frequencies than traditional switch mode capacitors because of the smoothness of the adjustment of its equivalent capacitance through a DC voltage. Furthermore, as no active switches are used in the $T$-$DCVC$, the EMI of the circuit is much smaller.
Chapter 9:
Conclusions and Suggestions for Future Work

9.1 General Conclusions

This thesis proposed a DC-voltage Controlled Variable Capacitor (DCVC) for controlling the frequency of high frequency resonant converters. The DCVC has been applied to adjust or stabilize the resonant frequency at the primary side of IPT systems, and also to regulate the output voltage at the secondary side. The proposed methods have been verified by simulation and experimental results.

The thesis includes nine chapters in total. Chapter 1 presented the background development of WPT technology, the thesis topic, research aims and objectives as well as a precise outline of the thesis. Chapter 2 is a comprehensive literature review about the various aspects of high frequency IPT systems. Chapter 3 presented investigations on high-frequency resonant power converters for IPT systems. An autonomous push pull converter with improved gate drives has been developed to run at tens of MHz by utilizing the parasitic capacitances of the circuit. A method to adjust the frequency of this high frequency autonomous push pull converter at the gate side was presented in Chapter 4. Further on a Resistor-controlled DCVC (R-DCVC) and a Transistor-controlled DCVC (T-DCVC) was introduced at the resonant circuit side for adjusting the ZVS frequency of autonomous push pull converters in Chapter 5 and 6, respectively. Chapter 7 proposed a method to stabilize the ZVS frequency of the autonomous push pull converter by DCVC through PLL control. Chapter 8 proposed another application of T-DCVC to the secondary side of an IPT system to stabilize the output voltage. More detailed work conducted in each chapter of this thesis is presented below.
Chapter 1 was about the overall background and development of WPT technologies [4, 7-10, 12, 25, 256]. The history, origin and early work of the WPT technology [12, 175, 256] were traced and different kinds of WPT technologies [2] presented. Various applications of the technology [2] were summarized. A thorough literature review on IPT technologies [2, 15, 26] was carried out. The key features of this technology were identified and the overall strategies to improve the system performance proposed. The overall structure of an IPT system, ways to increase the power transfer ability and efficiency, different kinds of traditional converters, and the various aspects of an IPT system, such as different coupling approaches, resonance and compensation, traditional power flow control methods [2], were investigated. Different kinds of traditional converters [2], especially the merits and drawbacks of autonomous push pull converters were explored in detail. The major focus in the literature review was different kinds of traditional method for adjusting the resonant frequency of switch mode converters using switch mode capacitors [103-106, 186-188] and inductors [203-218].

Chapter 2 was a comprehensive literature survey of high frequency IPT systems regarding the basic structure and various operating principles.

Chapter 3 studied traditional high frequency resonant power converters and investigated a single-side current-fed energy injection converter and two double-side current-fed energy injection converters, based on which basic principles for designing current-fed energy injection converters were summarized. A comparison between the voltage-fed and current-fed energy injection converters was made, and possible ways for realizing high frequency operation were summarized as below:

- Open loop control without detections such as the basic class E converter
- Autonomous push pull converter without separate detection circuitry
- Detecting the Zero Crossing Points (ZCP) of the voltage or current in advance, or delaying the detected ZCP signal to take effect in the following cycle.

The open loop approach is suitable for situations when the natural oscillating frequency of system is very stable. Nevertheless, the natural oscillating frequency of an IPT system varies with many factors such as the coupling coefficient between the primary and secondary coils, the variation of the load, etc. The autonomous push pull can realize soft-switching automatically, however its gate driving signals are not sharp square waves generated by
standard gate drivers so its work is not stable. The third approach, detecting the ZCP of the voltage or current in advance or delaying the detected ZCP signal to the following cycle, is difficult to achieve for variable speed operation, particularly at high frequency. Overall, the autonomous push pull converters were regarded to be more promising for high-frequency operation as they can realize soft-switching automatically without external detection and control circuits, so they are chosen to be the main converters being studied in this research.

Chapter 4 proposed a method to adjust the ZVS frequency of an autonomous push pull converter by gate side DC voltage control utilizing the parasitic capacitances of the circuit. This laid a solid base for proposing the DCVCs presented later in Chapters 5 and 6. Simulation studies on the relationships among the key parameters of the circuit were carried out. Equivalent circuit analyses were conducted. A simplified theoretical model for the relationship between the equivalent capacitance of the circuit and the on-resistances of the two transistors was established. Experimental studies were carried out to prove the relationship between the frequency of the converter and control voltage, and the relationship between the gate voltage and the control voltage. It was proven by both simulation and experimental studies that the gate voltage plays a key role and there is a fixed relationship between the equivalent capacitance or the frequency of the converter and the gate voltage. Finally, two alternative ways to controlling the gate voltage were suggested.

Chapter 5 proposed a Resistor-controlled DCVC (R-DCVC). The basic operating principle of the R-DCVC was explained in detail. Simulation studies for the relationships among key circuit parameters such as the frequency of the converter, the equivalent capacitance of the R-DCVC, the conduction period of the diode and the control voltage were carried out. Detailed theoretical analysis was conducted and theoretical relationships between the frequency of the converter and the control voltage, the equivalent capacitance of the R-DCVC and the control voltage, and the relationship between the conduction period of the diode and control voltage were established. Practical experiments were carried out to prove the relationship between the frequency of the converter and the control voltage. As only a DC voltage and a resistor were needed, the control of the R-DCVC is very simple in comparison with traditional switch mode capacitors. As no active switching is involved in the R-DCVC, the EMI is much reduced. Finally, as the equivalent capacitance of the R-DCVC is varied smoothly with a DC voltage, it has the potential to be applied to much higher frequencies than traditional switch mode capacitors and inductors.
Chapter 9: Conclusions and Suggestions for Future Work

Chapter 6 proposed a Transistor-controlled DCVC (T-DCVC). In the T-DCVC, the voltage on the anode of the diode is controlled mainly by the collector current $i_c$ of the transistor. The DC voltage $V_c$ controls the collector current $i_c$ through the base current $i_b$, which was found to be much smaller than that of the R-DCVC. Practical experiments were carried out to prove the validity of the method with a 10W IPT system working at 1.65MHz. Other alternative ways were presented to control the voltage on the anode of the diode using BJTs and MOSFETs and with the ground of the control voltage connected to different points of the circuit, and their advantages and disadvantages were compared. It was found that only three of the control methods, i.e. the two using BJTs but with the ground of the controlling voltage connected to the ground of the autonomous push pull converter or to the emitter of the BJT, and the one using a MOSFET and with the ground of the controlling voltage connected to the ground of the autonomous push pull converter were most practical.

Chapter 7 presented the application of the DCVCs at the primary side of an IPT system for stabilizing the ZVS frequency through PLL control. The main focus of this chapter was on the design of the PLL controller. With the DCVCs used as variable resonant capacitors, the autonomous push pull converter functions like a voltage controlled oscillator (VCO) so that the PLL technology can be employed directly to stabilize its frequency. However, one difference between the VCO for the autonomous push pull converter and a common VCO in a radio system is that the voltage and current ratings of the autonomous push pull converter are normally too high to be connected directly to a low voltage PLL controller. So some voltage and current matching circuits were needed between the VCO formed by the autonomous push pull converter and a common PLL controller. After an explanation of the overall strategy and operating principle using the PLL technology to control and stabilize the frequency of the autonomous push pull converter, this chapter focused mainly on the design of the voltage and current matching circuits. In total, one voltage matching circuit before the phase detector (PD) and four different voltage and current matching circuits after the low-pass filter (LF) were proposed. The voltage matching circuit before the PD monitors the actually operating frequency of the autonomous push pull converter with a comparator while simply using a few resistors as voltage dividers to lower the high voltage of the resonant tank of the autonomous push pull converter. Relatively, there are more choices for the voltage and current matching circuit after the LF. Four of them were proposed in this research. Their main function is to generate the control voltage $V_c$ for the DCVCs used as the resonant capacitor in the autonomous push pull converter. Practical experiments were carried out to
prove the validity of this control strategy for both low frequency applications (eg at 240kHz) using the T-DCVC presented in Chapter 6, and high-frequency applications (eg upto 10MHz) using the frequency control method presented in Chapter 4.

Chapter 8 described the application of the T-DCVC at the secondary side of an IPT system for stabilizing the output voltage. The T-DCVC was used as a variable tuning capacitor for the pick-up circuit. A PI controller was designed to monitor the fluctuation of the output voltage and generate the controlling voltage accordingly for the T-DCVC. As the equivalent capacitance of the T-DCVC changes with its control voltage, the tuning and detuning condition of the pick-up circuit and therefore the power transferred from the primary to the secondary side varies with the variation of this control voltage. When this control voltage was generated by the PI controller, the output voltage of the power pickup was kept constant. Both of the two cases when the T-DCVC were used as a parallel and a serial tuned resonant capacitor were presented. It was found in the experiments that when the T-DCVC was used as a parallel resonant capacitor, the output power reached maximum when the load resistance and the output voltage were relatively small and low (3.3~5.3 Ω and 5V in the experiments). When the T-DCVC was used as a serial resonant capacitor, the output power reached maximum when the load resistance and the output voltage were relatively larger and higher (100 Ω and 24V in the experiments). The experiments were carried out at about 290 kHz to prove the practical usefulness of the method; however, as the equivalent capacitance of the T-DCVC can be controlled smoothly by a DC voltage with minimal EMI, the T-DCVC has the potential to be used at much higher frequencies than traditional switch mode capacitors.

In summary, this research proposed the DCVCs for adjusting the ZVS frequency of the autonomous push pull converter. In addition to adjusting the ZVS frequency, two further applications of the DCVCs were proposed for stabilizing the ZVS frequency of the autonomous push pull converter at the primary side through PLL control and for stabilizing the output voltage of the secondary side of an IPT system through PI controller. Autonomous push pull converters were used as a base converter to study the characteristics of the DCVCs, although the DCVCs proposed in this research can also be potentially used for other resonant DC-AC power converter applications as will be discussed later in Section 9.3.

9.2 Contributions of this Thesis

The key contributions of this thesis are summarized below:
Chapter 9: Conclusions and Suggestions for Future Work

- Proposal of the general method of DC-voltage Controlled Variable Capacitors (DCVC) for frequency control of IPT systems [27, 118, 257, 258].
- Proposal of methods to adjust the resonant frequency of MHz level autonomous push pull converter by gate side DC voltage control [258].
- Proposal of a Resistor-controlled DCVC (R-DCVC) for adjusting the resonant frequency of the autonomous push pull converter [118].
- Proposal of a Transistor-controlled DCVC (T-DCVC) for adjusting the resonant frequency of the autonomous push pull converter [257].
- Proposal of PLL controllers for stabilizing the ZVS frequency of autonomous push pull converters via the DCVCs [257].
- Proposal of methods to apply the T-DCVC to the secondary side of an IPT system for stabilizing the output voltage [259, 260].

Part of the research results have led to five journal articles [118, 257-260], three conference papers [27, 261, 262], and one patent as listed below.

Journal articles:


165
Conference papers:


Patent:


9.3 Suggestions for Future Work

Below are some suggestions for future work:

- Exploration of methods to control the voltage on the anode of the diode in the DCVC other than using a resistor (as in in the R-DCVC) or a transistor (as in the T-DCVC). The major disadvantage of the DCVC is the power consumption of the resistor in the R-DCVC and the transistor in the T-DCVC. The exploration of new methods to control the voltage on the anode of the diode in the DCVC which consumes less energy than the resistor as in the R-DCVC and the transistor as in the T-DCVC is of great significance.

- Methods to drive the autonomous push pull converters by standard gate drivers. Most of the methods proposed in this research were based on and tested with the autonomous push pull converter. The advantage of the autonomous push pull converter is that it is simple and can realize soft-switching automatically. However, one disadvantage of the autonomous push pull converter is that its gate driving signal is not a sharp square wave that could be generated by a formal gate driver. It may change with the operating
condition of the converter, which may cause large variations in the gate driving signals and lower the power efficiency of the converter. Accordingly, one direction for future work could be the realization of a push pull converter driven by standard gate drivers, while maintaining its autonomous soft-switching operation.

- New methods to dynamically monitor the resonant frequencies of IPT systems. The operating frequency of an IPT system is a key factor that influences all the important aspects of the system including soft-switching, resonant operation, power transfer capability, power efficiency, etc. The resonant frequency of the system must be considered so that soft-switching and resonant operations are achieved with maximum power transfer and efficiency. As is well known, the resonance offers advantages to IPT or WPT systems, which requires that the driving frequency follow the resonant frequency of the system. However, the resonant frequency of the system is not constant but changes with many factors such as the coupling coefficient between the primary and secondary side, and the variation of the load and other circuit parameters. Accordingly, methods are needed to dynamically monitor the resonant frequency of the system so that the system is driven with this dynamically changing frequency. Nevertheless, the current detection and feedback approaches have many drawbacks for this purpose, especially in high-frequency operations. New methods to monitor the dynamically changing resonant frequencies of the system are needed.

- Methods for achieving voltage-controlled & soft-switched capacitors. To maintain full soft switching, DCVCs have been proposed in this research. However, one disadvantage of the proposed DCVCs is that their power consumption is higher than switching mode capacitors because of the linear operation of the controlling transistor or resistor. Existing switching mode capacitors or inductors also have various disadvantages such as high EMI, and difficult to realize soft-switching. To drive an IPT or a WPT system flexibly with frequencies other than the resonant frequencies of the system while soft-switching and resonant operation are still maintained, new methods to dynamically adjust the resonant frequency of the system are required, for example by voltage controlled and soft-switched capacitors, which may be another direction for future research.

- Extending the proposed DCVCs to resonant power converters other than the autonomous push pull converters. Most of the methods proposed in this research were tested based on the autonomous push pull converter. Actually the general method can be used for other
types of converters such as the Class E converter, or the voltage-fed DC-AC resonant power converter.

- The proposed DCVCs can also be applied in power systems as variable capacitors for applications such as power factor corrections, which can be a possible new direction for future research.
Appendix A

Method to calculate the absolute value of electric charge of a capacitor

Appendix A is to explain how the absolute value of electric charge and discharge flowing into and out of a capacitor is calculated and how the equivalent capacitance is derived finally based on the concept of the physical meaning of electric charge and discharge of a capacitor. The derivation process will start from the following most basic, obvious and well-known fact.

Assume that there is a constant current “I” flowing through a capacitor “C”. During a time period of \(\Delta t\), the electric charge “\(q_c\)” flowing into the capacitor is:

\[
q_c = I \cdot \Delta t \quad (A-1)
\]

Assume that the current flowing through the capacitor is not constant but varies during the time period from “\(t1\)” to “\(t2\)”. If the current is expressed by “\(i(t)\)”, the total electric charge “\(q_v\)” flowing into the capacitor during this period can be expressed by:

\[
q_v = \int_{t_1}^{t_2} i(t) \cdot dt \quad (A-2)
\]

Assume that the voltage across the capacitor during the same time period from “\(t1\)” to “\(t2\)” is “\(v(t)\)”, the relationship expressed by formula (A-3) holds:

\[
i(t) = C \cdot \frac{dv(t)}{dt} \quad (A-3)
\]

Substituting (A-3) into (A-2) gives:

\[
q_v = \int_{t_1}^{t_2} C \cdot \frac{dv(t)}{dt} \cdot dt \quad (A-4)
\]
Appendix A

Assume “\(v'\)” is used to represent the differential of the voltage “\(v(t)\)”, which can be expressed by (A-5):

\[
v' = \frac{dv(t)}{dt} \quad \text{(A-5)}
\]

Substituting (A-5) into (A-4) gives:

\[
q_v = \int_{t_1}^{t_2} C \cdot v' \cdot dt \quad \text{(A-6)}
\]

It is not difficult to see from equation (A-6) that \(q_v\) is positive when \(v'\) is positive, and negative when \(v'\) is negative. When \(v'\) is positive, the voltage “\(v(t)\)” increases during the period from “\(t_1\)” to “\(t_2\)”, so “positive” here means that the electric charge flows into the capacitor. Accordingly, when \(v'\) is negative, the voltage “\(v(t)\)” decreases during the period from “\(t_1\)” to “\(t_2\)”, so “negative” here means that the electric charge flows out of the capacitor.

When the absolute value of electric charge flowing into and out of the capacitor is considered which means taking both of the electric charge flowing into and out of the capacitor as positive, equation (A-7) holds:

\[
|\Delta Q| = \int_{t_1}^{t_2} C \cdot |v'| \cdot dt \quad \text{(A-7)}
\]

where: \(|\Delta Q|\) means the absolute value of electric charge flowing into and out of the capacitor.

Fig. A-1. The voltage \(v\) across the capacitor.
Appendix A

Assume that the voltage across the capacitor “v(t)” is a simple sine wave as shown in Fig. A-1, from which it can be seen that the voltage “v(t)” includes both periods of increasing and decreasing. During the periods the voltage “v(t)” increase, its differential v’ is positive and during the periods the voltage “v(t)” decrease, its differential v’ is negative. As a result, the electric charges calculated Based on formula (A-6) are positive during the periods the voltage “v(t)” increase and negative during the periods voltage “v(t)” decrease. To calculate the absolute value of electric charge flowing into and out of the capacitor, a negative sign should be added to the electric charges calculated for the periods the voltage “v(t)” decrease. (A-8) expresses the absolute value of electric charge flowing into and out of the capacitor C during the period from 0 to t5 when the voltage across the capacitor is a pure sine wave as shown in Fig. A-1.

\[
|\Delta Q| = \int_{t_0}^{t_1} C v' \, dt - \int_{t_1}^{t_2} C v' \, dt + \int_{t_2}^{t_3} C v' \, dt - \int_{t_3}^{t_4} C v' \, dt + \int_{t_4}^{t_5} C v' \, dt \quad (A-8)
\]

Equation (A-8) presents the general formula to calculate the absolute value of electric charge flowing into and out of a capacitor with the voltage across the capacitor is assumed to be a pure sine wave as an example. The method to calculate the absolute value of electric charge flowing into and out of a capacitor when the voltage across the capacitor is not a pure sine wave is similar. Generally, to calculate the absolute value of electric charge flowing into and out of a capacitor during a fixed period Based on formula (A-8), the voltage across the capacitor should be divided into sections the voltage increases and decreases first. Then the electric charge flowing into and out of the capacitor during each section should be calculated and a negative sign should be added to the electric charges calculated for the sections during which the voltage “v(t)” decrease. Finally, the total absolute value of the electric charge flowing into and out of the capacitor during the whole period is the algebraic sum of all the electric charges calculated for each section with a negative sign added to those sections during which the voltage decreases. It should be noted that the principle to separate the voltage across the capacitor into sections is not based on the sign of the voltage across the capacitor itself but on the sign of the differential of the voltage across the capacitor, i.e. on whether the voltage increases or decreases.
Appendix B

Detailed derivative process for the relationship between the diode conduction period $T_{con}$ and the equivalent resistance $R_c$ of the controlling MOSFET

When the transistor $Q_c$ used in the $TCVC$ as shown in Fig. 4-1 (a) is not a BJT transistor, but a MOSFET as shown in Fig. 4-17, 5-18 and 5-24, the MOSFET $S_c$ cannot be modelled as a current source but can be as an equivalent resistance $R_c$ as shown in Fig. B-1.

Fig. B-1 shows the circuit structure for the theoretical analysis.

The purpose of the analysis is to establish a mathematical model for the relationship between the conduction period of the diode $D_c$-$T_{con}$ and the resistance of the variable resistor $R_c$. To derive the relationship between $T_{con}$ and $R_c$, two exact moments, i.e. the moment the diode starts to conduct ($t_{on}$) and the moment the diode stops to conduct ($t_{off}$) need to be determined first. After that, $T_{con}$ can be calculated with (B-1):

$T_{con} = t_{off} - t_{on}$  \hspace{1cm} (B-1)

It is assumed that the circuit is driven by an ideal sine wave as expressed by formula (B-2):

$V_s = A_s \sin \omega t$  \hspace{1cm} (B-2)
Appendix B

Fig. B-2 shows the typical wave forms of the circuit in steady state. The origin of the coordinate system is chosen at 0. In this way, both of the two moments the diode starts and stops to conduct \( t_{on} \) and \( t_{off} \) fall between \( 0 \sim \pi/2 \), which makes it possible to use anti-trigonometric functions in the derivative process because the domain and range of the anti-trigonometric functions are usually restricted between \(-\pi/2 \sim \pi/2\).

Fig. B-2. Typical wave forms of \( v_s \), \( v_{Cup} \), and \( T_{con} \).

Below is the detailed derivative process for determining the moment the diode stops to conduct (\( t_{off} \)), starts to conduct (\( t_{on} \)) and the relationship between \( T_{con} \) and \( R_c \).

**B.1 Determination of the moment the diode stops to conduct-\( t_{off} \)**

Fig. B-3 shows the equivalent circuit when the diode is conducting.

Fig. B-3. The equivalent circuit when the diode is conducting.
Appendix B

C_up, D_c and R_c are removed from the circuit because an ideal conducting diode amounts to a short-circuit. As a result, it can be seen from Fig. B-3 that the equivalent circuit becomes a simple single-parameter capacitor circuit and the current \( i_s \) is the current flowing through the ideal diode. The diode can be regarded as stopping to conduct when the current \( i_s \) becomes zero.

As is well-known, the current and voltage relationship of the pure capacitor circuit is governed by formula (B-3):

\[
  i_s = C_{dw} \frac{dv_s}{dt} \quad (B-3)
\]

Substituting formula (B-2) into formula (B-3) gives:

\[
  i_s = \omega A_s C_{dw} \cdot \cos \omega t \quad (B-4)
\]

Comparing the expression of \( v_s \) and \( i_s \) in formula (B-2) and (B-4), it can be seen that \( v_s \) is a sine wave and \( i_s \) a cos wave, therefore the phase of \( i_s \) is \( \pi/2 \) ahead of that of \( v_s \) as shown in Fig. B-4.

![Fig. B-4. The phase of \( i_s \) is \( \pi/2 \) ahead of that of \( V_s \).](image)

As it is assumed that the diode stops to conduct when the current in it drops to zero, it can be seen from Fig. B-4 that the moment the diode stops to conduct \( t_{off} \) is \( \pi/2 \) as expressed by formula (B-5):

\[
  t_{off} = \frac{\pi}{2\omega} \quad (B-5)
\]
Appendix B

B.2 Determination of the moment the diode starts to conduct-to

Fig. B-5 shows the equivalent circuit when the diode is not conducting so that regarded as open and removed from the circuit. The diode starts to conduct when the voltage on its anode becomes bigger than that on its cathode. The voltage at the anode of the diode $V_{\text{anod}}$ is $V_{\text{Cup}}$ during the period the diode does not conduct, and the voltage at the cathode of the diode $V_{\text{cath}}$ is zero at the moment before the diode is going to conduct for the autonomous push pull converter, so the moment that the diode starts to conduct is when $V_{\text{Cup}}$ becomes zero.

![Fig. B-5. The equivalent circuit when the diode is not conducting.](image)

**B.2.1 The equation governing $v_{\text{Cup}}$**

The circuit as shown in Fig. B-5 has one known and six unknown variables as follows:

**Known:**
- The driving voltage source $v_S$ as expressed by formula (B-2)

**Unknowns:**
- Currents: $i_{\text{Cup}}, i_{\text{CdW}}, i_{\text{Rc}}$
- Voltages: $v_{\text{Cup}}, v_{\text{CdW}}, v_{\text{Rc}}$

Based on KCL, the following equation holds:

$$i_{\text{Cup}} = i_{\text{CdW}} + i_{\text{Rc}} \quad (B-6)$$

Based on KVL, the following equation holds:
Appendix B

\[ v_S = v_{\text{Cup}} + v_{\text{Cd}} \]  \hspace{1cm} (B-7)

\[ v_{\text{Re}} = v_{\text{Cup}} \]  \hspace{1cm} (B-8)

And the voltage and current relationships of the devices can be expressed as:

\[ i_{\text{Cup}} = C_{\text{up}} \frac{dv_{\text{Cup}}}{dt} \]  \hspace{1cm} (B-9)

\[ i_{\text{Cd}} = C_{\text{d}} \frac{dv_{\text{Cd}}}{dt} \]  \hspace{1cm} (B-10)

\[ i_{\text{Re}} = -\frac{v_{\text{Re}}}{R_c} \]  \hspace{1cm} (B-11)

Substituting formula (B-9), (B-10) and (B-11) into formula (B-6) to eliminate the three unknown current variables \( i_{\text{Cup}}, i_{\text{Cd}}, i_{\text{Re}} \) gives:

\[ C_{\text{up}} \frac{dv_{\text{Cup}}}{dt} = C_{\text{d}} \frac{dv_{\text{Cd}}}{dt} - \frac{v_{\text{Re}}}{R_c} \]  \hspace{1cm} (B-12)

Substituting formula (B-7) and (B-8) into formula (B-12) to eliminate the two unknown variables \( v_{\text{Cd}} \) and \( v_{\text{Re}} \) gives:

\[ C_{\text{up}} \frac{dv_{\text{Cup}}}{dt} = C_{\text{d}} \frac{d(v_s - v_{\text{Cup}})}{dt} - \frac{v_{\text{Cup}}}{R_c} \]  \hspace{1cm} (B-13)

Substituting formula (B-2) into formula (B-13), make differentation and rearrangements gives:

\[ \frac{dv_{\text{Cup}}}{dt} + \frac{1}{R_c(C_{\text{up}} + C_{\text{d}})} v_{\text{Cup}} = \frac{\omega A_s C_{\text{d}} \cos \omega t}{C_{\text{up}} + C_{\text{d}}} \]  \hspace{1cm} (B-14)

Formula (B-14) is the deferential equation governing \( v_{\text{Cup}} \).
Appendix B

B.2.2 The solution of the equation

Assign \( P(t) = \frac{1}{R_c(C_{up} + C_{dw})} \) and \( Q(t) = \frac{\omega A_s C_{dw} \cos \omega t}{C_{up} + C_{dw}} \), formula (B-14) becomes:

\[
\frac{dv_{Cup}}{dt} + P(t) \cdot v_{Cup} = Q(t)
\]

(B-15)

Formula (B-15) is a first order non homogeneous linear differential equation. Its full solution is:

\[
v_{Cup} = e^{-\int P(t) dt} \left( \int Q(t) e^{\int P(t) dt} dt + K \right)
\]

(B-16)

Where: \( \int P(t) dt \) can be calculated as:

\[
\int P(t) dt = \int \frac{1}{R_c(C_{dw} + C_{up})} dt = \frac{t}{R_c(C_{dw} + C_{up})}
\]

(B-17)

Substituting formula (B-17) and \( Q(t) \) into formula (B-16) gives:

\[
v_{Cup} = e^{-\tau} \cdot \left( \int \frac{\omega A_s C_{dw} \cos \omega t}{C_{up} + C_{dw}} \cdot e^{\frac{t}{\tau}} dt + K \right)
\]

(B-18)

Assign \( \tau = R_c(C_{dw} + C_{up}) \), formula (B-18) becomes:

\[
v_{Cup} = e^{-\frac{t}{\tau}} \cdot \left( \int \frac{\omega A_s C_{dw} \cos \omega t}{C_{up} + C_{dw}} \cdot e^{\frac{t}{\tau}} dt + K \right)
\]

(B-19)

Rearrange formula (B-19), gives:

\[
v_{Cup} = e^{-\frac{t}{\tau}} \cdot \left( \frac{\omega A_s C_{dw}}{C_{up} + C_{dw}} \int \cos \omega t \cdot e^{\frac{t}{\tau}} dt + K \right)
\]

(B-20)

As:
Appendix B

\[
\int \cos \omega t \cdot e^{t \tau} \cdot dt = \frac{\omega \tau^2}{\omega^2 \tau^2 + 1} \sin \omega t \cdot e^{t \tau} + \frac{\tau}{\omega^2 \tau^2 + 1} \cos \omega t \cdot e^{t \tau}
\]  \hspace{1cm} \text{(B-21)}

Formula (B-20) becomes:

\[
v_{\text{Cup}} = \left( \frac{\omega A_s C_{\text{dw}} R_c}{\omega^2 \tau^2 + 1} (\omega t \cdot \sin \omega t + \cos \omega t) + K \cdot e^{-t \tau} \right)
\]  \hspace{1cm} \text{(B-22)}

Assign \(k_1 = \frac{\omega A_s C_{\text{dw}} R_c}{\omega^2 \tau^2 + 1}\), formula (B-22) can be reduced to:

\[
v_{\text{Cup}} = (\omega t k_1 \cdot \sin \omega t + k_1 \cdot \cos \omega t) + K \cdot e^{-t \tau}
\]  \hspace{1cm} \text{(B-23)}

**B.2.3 The constant K in the equation**

The constant \(K\) in formula (B-23) can be determined by the initial condition, i.e. the value of \(v_{\text{Cup}}\) (zero) at the moment of \(-3\pi/2\omega\) as shown in Fig. B-2.

Substituting \(t = -\frac{3\pi}{2\omega}\) and \(v_{\text{Cup}} = 0\) into formula (B-23) gives:

\[
0 = \omega t k_1 \cdot \sin \left( -\frac{3\pi}{2} \right) + k_1 \cdot \cos \left( -\frac{3\pi}{2} \right) + K \cdot e^{3\pi \frac{1}{2\omega \tau}}
\]  \hspace{1cm} \text{(B-24)}

Formula (B-24) can be reduced to:

\[
0 = \omega t k_1 \cdot 1 + k_1 \cdot 0 + K \cdot e^{3\pi \frac{1}{2\omega \tau}}
\]  \hspace{1cm} \text{(B-25)}

Finally, the constant \(K\) can be derived as:

\[
K = -\frac{\omega t k_1}{e^{3\pi \frac{1}{2\omega \tau}}}
\]  \hspace{1cm} \text{(B-26)}

Substituting \(k_1\) into formula (B-26) gives:

\[
K = -\frac{\omega^2 \tau A_s C_{\text{dw}} R_c}{(\omega^2 \tau^2 + 1) \cdot e^{3\pi \frac{1}{2\omega \tau}}}
\]  \hspace{1cm} \text{(B-27)}
Appendix B

B.2.4 The moment the diode starts to conduct

Formula (B-23) expresses the voltage $v_{Cup}$ during the period the diode does not conduct. As mentioned at the beginning of Section B.2, the moment the diode starts to conduct $t_{on}$ is when $v_{Cup}$ becomes zero which can be expressed by formula (B-27) through substituting $v_{Cup} = 0$ into formula (B-23):

$$0 = \omega r k_1 \cdot \sin \omega t_{on} + k_1 \cdot \cos \omega t_{on} + K \cdot e^{-\frac{t_{on}}{\tau}}$$ (B-28)

The exponential component $K \cdot e^{-\frac{t_{on}}{\tau}}$ in formula (B-28) relates to the transient response of the circuit which does not change much during a short time period of one or half a cycle of $v_{Cup}$ which is usually much smaller than the time constant of the circuit $\tau$ determined by the product of the capacitor and resistor of the circuit $R_c(C_{up} + C_{dw})$. As a result, $K \cdot e^{-\frac{t_{on}}{\tau}}$ can be set roughly at a constant value $K \cdot e^{-\frac{t_c}{\tau}}$ where $t_c$ can be simply zero. However, the closer $t_c$ is to the moment the diode starts to conduct $t_{on}$, the smaller the error it causes. As a result, the moment the diode starts to conduct $t_{on}$ can be expressed approximately as:

$$0 \approx \omega r k_1 \cdot \sin \omega t_{on} + k_1 \cdot \cos \omega t_{on} + K \cdot e^{-\frac{t_c}{\tau}}$$ (B-29)

where $t_c$ is a constant value. Based on trigonometric formula (B-30):

$$A \cdot \sin \omega t + B \cdot \cos \omega t = \sqrt{A^2 + B^2} \cdot \sin(\omega t + \arctan\frac{B}{A})$$ (B-30)

Formula (B-29) becomes:

$$0 \approx k_1 \sqrt{(\omega r)^2 + 1} \cdot \sin(\omega t_{on} + \arctan\frac{1}{\omega r}) + K \cdot e^{-\frac{t_c}{\tau}}$$ (B-31)

Finally, $t_{on}$ can be derived as:
Substituting $k_1$ into formula (B-32) gives:

$$t_{on} \approx \frac{arcsin \left( -\frac{Ke^{-\frac{\tau}{\tau}}}{k_1\sqrt{(\omega \tau)^2+1}} \right) - \arctan \frac{1}{\omega \tau}}{\omega}$$

(B-33)

### B.3 Determination of the relationship between $T_{con}$ and $R_c$

The period of the diode conducts $T_{con}$ can be found by substituting formula (B-5) and (B-33) into formula (B-1):

$$T_{con} = \frac{\pi}{2\omega} - \frac{arcsin \left( -\frac{\sqrt{\omega^2 \tau^2 + 1} Ke^{-\frac{\tau}{\tau}}}{\omega A_s c_{dw} R_c} \right) - \arctan \frac{1}{\omega \tau}}{\omega}$$

(B-34)

Where: $\tau = R_c (C_{dw} + C_{up})$.

Formula (B-34) expresses the relationship between $T_{con}$ and $R_c$ when the circuit as shown in Fig. B-1 is driven by a fixed frequency voltage source $V_s$. However, when the part of the circuit as shown in the dashed box of Fig. B-1 is applied to the resonant tank of a push pull converter, its driving frequency is not fixed but varies with the instant capacitance of the part of the circuit as shown in the dashed box of Fig. B-1. In such cases, by replacing the angular frequency $\omega$ in (B-34) with relevant values of the capacitor and inductor of the resonant tank based on $\omega = \frac{1}{\sqrt{LC}}$, (B-34) becomes (B-35):

$$T_{con} = \sqrt{\frac{1}{LC_{on}}} \left[ \frac{\pi}{2} - arcsin \left( -\frac{\sqrt{LC_{off} + \frac{\tau^2}{A_s C_{dw} R_c}}} {A_s c_{dw} R_c} \right) - \arctan \frac{\sqrt{LC_{off} \tau}}{\tau} \right]$$

(B-35)

Where $C_{on}$ and $C_{off}$ means the capacitance of the circuit when the diode is on and off respectively, i.e.:
Appendix B

\[ C_{\text{on}} = C_{\text{dw}} \]  
\[ C_{\text{off}} \approx \frac{C_{\text{up}}C_{\text{dw}}}{C_{\text{up}} + C_{\text{dw}}} \]

Here \( C_{\text{off}} \) approximately instead of exactly equals \( C_{\text{up}} \) and \( C_{\text{dw}} \) in series because the branch of the variable resistor \( R_c \) is ignored when calculating \( C_{\text{off}} \) assuming that the resistance of \( R_c \) is much larger than those of the two capacitors \( C_{\text{up}} \) and \( C_{\text{dw}} \) so that the current in \( R_c \) is much smaller than those in \( C_{\text{up}} \) and \( C_{\text{dw}} \) and therefore its influence to the charging and discharging process of the two capacitors can be neglected.

Fig. B-6 shows the relationship curves between \( T_{\text{con}} \) and \( R_c \) got from formula (B-34), (B-35) and simulation together, from which it can be seen that the one got from formula (B-35) is closer to the simulation result than the one got from formula (B-34) because (B-35) considers the difference between the frequencies when the diode is on and off, which is closer to the real circuit situation.

![Fig. B-6. The relationship curve between \( T_{\text{con}} \) and \( R_c \) got from (B-34), (B-35) and simulation.](image)

<table>
<thead>
<tr>
<th>Resistance (( \Omega ))</th>
<th>( T_{\text{con}} ) (us)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2.5</td>
</tr>
<tr>
<td>20</td>
<td>2.0</td>
</tr>
<tr>
<td>40</td>
<td>1.5</td>
</tr>
<tr>
<td>60</td>
<td>1.0</td>
</tr>
<tr>
<td>80</td>
<td>0.5</td>
</tr>
<tr>
<td>100</td>
<td>0</td>
</tr>
</tbody>
</table>

\( T_{\text{con}} \) vs. \( R_c \)

- **Result of simulation**
- **Result of (B-35)**
- **Result of (B-34)**
Appendix C

The detailed derivative process for the equivalent capacitance of a switching mode capacitor from the perspective of its effect on frequency

C.1 General Strategy

As the final purpose of the derivation of the equivalent capacitance is to find its effect on the frequency of the converter, instead of from the perspective of the physical meaning of electric charging and discharging of a capacitor, this derivation of the equivalent capacitance is based on the idea of the effect of the capacitance on the frequency when the capacitor is used as a resonant capacitor in a resonant tank composed of a capacitor and an inductor. Two capacitors are regarded as equivalent when the frequencies of the resonant tanks, in which they act as resonant capacitors, are the same. Of course, the inductors in the two resonant tanks should also be the same in the first place.

The natural oscillating frequency of a resonant tank composed of a capacitor and an inductor is:

\[ f_e = \frac{1}{2\pi\sqrt{LC_e}} \]  

It can be from (C-1) that when the value of the inductor \( L \) is fixed, there is a one-to-one matching relationship between the frequency \( f_e \) and the capacitance \( C_e \), which means that when the frequency \( f_e \) is known, the capacitance is known too and can be derived based on the value of \( f_e \). When \( f_e \) is expressed in the form of \( T_e \) (the duty cycle or the reciprocal of the frequency \( f_e \)), (C-1) becomes:

\[ C_e = \frac{1}{4\pi^2 L f_e^2} = \frac{T_e^2}{4\pi^2 L} \]  

(C-2)
Appendix C

It can be seen from (C-2) that there is also a one-to-one matching relationship between the duty cycle $T_e$ and the capacitance $C_e$, which means that whenever the duty cycle $T_e$ is known, the capacitance $C_e$ is also known and can be derived based on the value of $T_e$. Therefore, the main task for deriving the equivalent capacitance $C_e$ becomes finding the duty cycle $T_e$. In the case of a switching mode capacitor, assume the on and off periods of the switch in the switching mode capacitor are $T_{on}$ and $T_{off}$ respectively during one duty cycle, then $T_e$ can be expressed as:

$$T_e = T_{on} + T_{off}$$  \hspace{1cm} (C-3)

Fig. C-1 shows the situation when two sinusoidal waves with two distinct frequencies $\omega_{on}$ and $\omega_{off}$ are connected together.

The situation shown in Fig. C-1 is similar to that of the voltage across the resonant tank of an autonomous push pull converter, in which the resonant tank is composed of a fixed value inductor and a switching mode capacitor, and the capacitance of this switching mode capacitor changes between two distinct values $C_{on}$ and $C_{off}$. When the capacitance of this switching mode capacitor is $C_{on}$, the frequency of the resonant tank is $\omega_{on}$, and when the capacitance of this switching mode capacitor is $C_{off}$, the frequency of the resonant tank is $\omega_{off}$. This is the background of the derivation of the equivalent capacitance of the switching mode capacitor. As shown in Fig. C-1, the on and off periods of the switch in the switching mode capacitor are $T_{on}$ and $T_{off}$, respectively during one duty cycle $T_e$. It can be seen from (C-2) that
the equivalent capacitance $C_e$ can be calculated when the duty cycle $T_e$ is known. To simplify the situation, assume that the period when the switch is on $T_{on}$ has already been known, to find $T_e$, the task left is only to find $T_{off}$. When $T_{off}$ is found out, $T_e$ can be calculated through (C-3).

The basic idea to calculate the value of $T_{off}$ according to the value of $T_{on}$ is that the height or the Y-coordinates of the two sinusoidal waves (with two distinct frequencies $\omega_{on}$ and $\omega_{off}$) at their jointing points should equal each other; otherwise, the waves will be broken. The height or the Y-coordinates of the two sinusoidal waves at their jointing points can be calculated from the initial value, the frequency ($\omega_{on}$ or $\omega_{off}$) and the length ($T_{on}$ or $T_{off}$) of the curves. Fig. C-1 shows the simplest situation when the initial values of both of these two curves is zero. During the process to derive $T_{off}$ from the height or the Y-coordinates of the two sinusoidal waves, arcsine functions need to be used. The range of arcsine functions is between $-\pi/2$ and $\pi/2$. To guarantee the range of the arcsine functions used falls between $-\pi/2$ and $\pi/2$ and according to the real situation of the conduction period $T_{on}$ of the diode in the DCVC as shown in Fig. 3-1 (a) of chapter 5, the derivation of $T_{off}$ is divided into the three situations as below:

- The Situation when $0 \leq \omega_{on} \cdot T_{on} < \pi$
- The Situation when $\pi \leq \omega_{on} \cdot T_{on} < 3\pi/2$
- The Situation when $3\pi/2 \leq \omega_{on} \cdot T_{on} < 2\pi$

where $\omega_{on}$ is the angular frequency of the voltage across the resonant tank of the autonomous push pull converter when the switch of the switching mode capacitor is on, and $\omega_{on} \cdot T_{on}$ the length of the conduction period $T_{on}$ in the radian form.

Next, $T_{off}$, the length of the period when the switch is off will be derived one by one in these three situations, and based on that, $T_e$ and $C_e$ will be calculated based on (C-3) and (C-2) under the assumption that $T_{on}$ has already been known. It can be found in the end that all the $T_e$ and $C_e$ calculated in these three situations are the same.

**C.2 The Situation when $0 \leq \omega_{on} \cdot T_{on} < \pi$**

The situation when $0 \leq \omega_{on} \cdot T_{on} < \pi$ is shown in Fig. C-2. The conducting period of the switch is from $t_1$ to $t_4$, and the non-conducting period of the switch is from $0$ to $t_1$ and from $t_4$ to $t_5$. The duty cycle $T_e$ is the sum of $t_1$, $T_{on}$ and $t_5$-$t_4$, which can be expressed by (C-4).
Appendix C

\[ T_e = t_1 + T_{on} + (t_5 - t_4) \]  \hspace{1cm} (C-4)

Fig. C-2. The situation when \( 0 \leq \omega_{on} \cdot T_{on} < \pi \).

The solid green curve (top part) from \( 0 \) to \( t_1 \) and the dashed green curve from \( t_1 \) to \( t_3 \) constitute a complete cycle of a sine wave with the frequency of \( \omega_{off} \). As the frequency of the part of the curve from \( t_4 \) to \( t_5 \) is also \( \omega_{off} \) and both the Y-coordinates of \( t_2 \) and \( t_4 \) are \( h_2 \), the part of the sine curve from \( t_2 \) to \( t_3 \) and that from \( t_4 \) to \( t_5 \) are congruent, which means “\( t_3 - t_2 \)” equals “\( t_5 - t_4 \)” as expressed by (C-5).

\[ (t_3 - t_2) = (t_5 - t_4) \]  \hspace{1cm} (C-5)

Substituting (C-5) into (C-4) gives:

\[ T_e = t_1 + T_{on} + (t_3 - t_2) \]  \hspace{1cm} (C-6)

It can be seen from Fig. C-2 that \( t_1 \) plus \( t_3 - t_2 \) equals \( t_3 - (t_2 - t_1) \) which can be expressed by (C-7):

\[ t_1 + (t_3 - t_2) = t_3 - (t_2 - t_1) \]  \hspace{1cm} (C-7)

Because \( t_3 \) is the duty cycle of the sinusoidal wave with the angular frequency of \( \omega_{offs} \), it equals \( 2\pi \) divided by \( \omega_{offs} \) as expressed by (C-8):
Appendix C

\[ t_3 = \frac{2\pi}{\omega_{off}} \]  
(C-8)

Substituting (C-8) into (C-7) gives:

\[ t_1 + (t_3 - t_2) = \frac{2\pi}{\omega_{off}} - (t_2 - t_1) \]  
(C-9)

Substituting (C-9) into (C-6) gives:

\[ T_e = T_{on} + \frac{2\pi}{\omega_{off}} - (t_2 - t_1) \]  
(C-10)

Fig. C-3. How the Y-coordinates of two sinusoidal curves with different frequencies equal each other.

Now, to calculate \( T_e \), the major task becomes finding the value of “\( t_2 - t_1 \)”, which is equivalent to the question of finding the length of the projection of a section of sinusoidal wave on the X-axis and can be seen more clearly on Fig. C-3 (a). The question of finding the value of \( t_2 - t_1 \) in Fig. C-2 is equivalent to finding the length of \( t_2 - t_1 \) in Fig. C-3 (a) when the two heights \( h_1 \) and \( h_2 \) are known. Now the question is converted to how to find the value of the two heights \( h_1 \) and \( h_2 \) as detailed below.
Appendix C

C.2.1 Determination of \( h_1 \)

Actually the determination of \( h_1 \) is very easy. It can simply be found by substituting \( t_1 \) into the expression of the sinusoidal wave in Fig. C-3 (a) as expressed by (C-11):

\[
 h_1 = A_1 e^{i \omega_{0t} t_1} \tag{C-11}
\]

What is a little complex is how to find \( h_2 \), which is detailed as below.

C.2.2 Determination of \( h_2 \)

As can be seen in Fig. C-2, \( h_2 \) can be found by substituting the horizontal ordinate into the expression of the sinusoidal wave with the frequency \( \omega_{on} \) as long as the horizontal ordinate (Note that it is not simply \( t_4 \)) is known. To find \( h_2 \) with this strategy, the above-mentioned horizontal ordinate in a sinusoidal wave with a pure frequency of \( \omega_{on} \) needs to be found first, which can be seen more clearly in Fig. C-3 (b). As shown in Fig. C-3 (b), the question now becomes how to find \( s_2 \), which can be expressed by (C-12):

\[
 s_2 = s_1 + T_{on} \tag{C-12}
\]

As it is assumed that \( T_{on} \) has already been known, now the question becomes how to find \( s_1 \). \( s_1 \) can be found by the value of \( h_1 \) in Fig. C-3 (b) which should be the same as the value of \( h_1 \) in Fig. C-3 (a), otherwise, the two sections of sinusoidal waves cannot be jointed together as shown in Fig. C-3 (c). As having been mentioned previously, the jointing of the two sinusoidal waves with different frequencies require that the heights or the Y-coordinates of these sinusoidal wave sections should be equal at the jointing points.

Substituting \( h_1 \) and \( s_1 \) into the expression of the sinusoidal wave with the frequency of \( \omega_{on} \) as shown in Fig. C-3 (b) gives:

\[
 h_1 = A_2 e^{i \omega_{on} s_1} \tag{C-13}
\]

From (C-13), \( s_1 \) can be solved as:
where, $h_1$ is the same as the $h_1$ as shown in Fig. C-3 (a) as expressed by (C-15):

$$h_1 = A_e \sin \omega_{off} t_1$$  \hspace{1cm} (C-15)

Substituting (C-15) into (C-14) gives:

$$s_1 = \frac{\omega_{off}}{\omega_{on}} t_1$$  \hspace{1cm} (C-16)

Substituting (C-16) into (C-12) gives:

$$s_2 = \frac{\omega_{off}}{\omega_{on}} t_1 + T_{on}$$  \hspace{1cm} (C-17)

As mentioned at the beginning of this section, $h_2$ can be found by substituting the horizontal ordinate $s_2$ into the expression of the sinusoidal wave with the frequency $\omega_{on}$, as expressed by (C-18):

$$h_2 = A_e \sin \omega_{on} \left( \frac{\omega_{off}}{\omega_{on}} t_1 + T_{on} \right) = A_e \sin \left( t_1 \omega_{off} + T_{on} \omega_{on} \right)$$  \hspace{1cm} (C-18)

### C.2.3 Determination of $t_2 - t_1$

With both $h_1$ and $h_2$ are known, the length of $t_2 - t_1$ in Fig. C-3 (a) can be calculated, which is the same as the value of $t_2 - t_1$ in Fig. C-2.

Form (C-11), $t_1$ can be solved as:

$$t_1 = \frac{\text{arcsin} \left( \frac{h_1}{A_e} \right)}{\omega_{off}}$$  \hspace{1cm} (C-17)
Substituting $t_2$ and $h_2$ as expressed by (C-16) into the expression: $A_e \sin \omega_{off} t$ gives:

$$A_e \sin (t_1 \omega_{off} + T_{on} \omega_{on}) = A_e \sin \omega_{off} t_2$$

(C-18)

From (C-18), $t_2$ can be resolved as:

$$t_2 = t_1 + \frac{\omega_{on}}{\omega_{off}} T_{on}$$

(C-19)

From (C-19), $t_2 - t_1$ can be resolved as:

$$t_2 - t_1 = \frac{\omega_{on}}{\omega_{off}} T_{on}$$

(C-20)

C.2.4 Determination of $T_e$ and $C_e$

Substituting (C-20) into (C-10) gives:

$$T_e = T_{on} + \frac{2\pi}{\omega_{off}} - \frac{\omega_{on}}{\omega_{off}} T_{on} = \left(1 - \frac{\omega_{on}}{\omega_{off}}\right) T_{on} + \frac{2\pi}{\omega_{off}}$$

(C-21)

Substituting (C-21) into (C-2) gives:

$$C_e = \frac{\left(1 - \frac{\omega_{on}}{\omega_{off}}\right) T_{on} + \frac{2\pi}{\omega_{off}}}{4\pi^2 L}$$

(C-22)

Formula (C-1) can be rewritten in the radian form as expressed by (C-23):

$$\omega_e = \frac{1}{\sqrt{LC_e}}$$

(C-23)

By substituting $\omega_{on}$ and $\omega_{off}$ into (C-23), the instant capacitance of the resonant tank $C_{on}$ and $C_{off}$ when the frequency is $\omega_{on}$ and $\omega_{off}$, respectively, can be derived as:
Appendix C

\[\omega_{on} = \frac{1}{\sqrt{L C_{on}}}\]  \hspace{1cm} (C-24)

\[\omega_{off} = \frac{1}{\sqrt{L C_{off}}}\]  \hspace{1cm} (C-25)

Substituting (C-24) and (C-25) into (C-22) gives:

\[C_e = \frac{\left(1 - \frac{C_{off}}{C_{on}}\right) T_{on} + 2\pi \sqrt{L C_{off}}}{4\pi^2 L}\]  \hspace{1cm} (C-26)

Formula (C-26) expresses the equivalent capacitance \(C_e\) for the situation when \(0 \leq \omega_{on} \cdot T_{on} < \pi\).

**C.3 The Situation when \(\pi \leq \omega_{on} \cdot T_{on} < 3\pi/2\)**

The situation when \(\pi \leq \omega_{on} \cdot T_{on} < 3\pi/2\) is shown in Fig. C-4.

![Fig. C-4. The situation when \(\pi \leq \omega_{on} \cdot T_{on} < 3\pi/2\).](image)

Similar to the situation \(0 \leq \omega_{on} \cdot T_{on} < \pi\), the overall strategy to get the equivalent capacitance \(C_e\) in this situation is also by calculating the duty cycle \(T_e\), and assuming that the conduction period of the switch \(T_{on}\) has already been known. So based on (C-3), task left is only to find \(T_{off}\).

As can be seen in Fig. C-4, \(T_{off}\) can be expressed by (C-27):
Appendix C

\[ T_{off} = t_1 = \frac{\pi}{\omega_{off}} - \left( \frac{\pi}{\omega_{off}} - t_1 \right) \]  

(C-27)

It can also be seen from Fig. C-4:

\[ \frac{\pi}{\omega_{off}} - t_1 = t_0 \]  

(C-28)

Based on:

\[ h = A_e \sin \omega_{off} t_0 \]  

(C-29)

“\( t_0 \)” can be found as:

\[ t_0 = \frac{\arcsin \left( \frac{h}{A_e} \right)}{\omega_{off}} \]  

(C-30)

Now the task left is how to find “\( h \)”. As can be seen in Fig. C-4, the absolute value of “\( h \)” is the Y-coordinate of the sinusoidal wave with the frequency of \( \omega_{on} \) at the point \( t_1 \). Taking “\( t_2 \)” as the origin of this sinusoidal wave with the frequency of \( \omega_{on} \), the X-coordinate of \( t_1 \) in radian form can be expressed by (C-31):

\[ t_1 = -T_{on} \cdot \omega_{on} \]  

(C-31)

Substituting (C-31) into the expression of a sinusoidal wave with the frequency of \( \omega_{on} \) gives:

\[ h = A_e \sin (-T_{on} \omega_{on}) = A_e \sin (T_{on} \omega_{on} - \pi) \]  

(C-32)

Substituting (C-32) into (C-30) gives:

\[ t_0 = T_{on} \frac{\omega_{on}}{\omega_{off}} - \frac{\pi}{\omega_{off}} \]  

(C-33)
Substituting (C-33) into (C-28) gives:

\[
\frac{\pi}{\omega_{off}} - \tau_1 = T_{on} \frac{\omega_{on}}{\omega_{off}} - \frac{\pi}{\omega_{off}} \tag{C-34}
\]

Substituting (C-34) into (C-27) gives:

\[
T_{off} = \frac{2\pi}{\omega_{off}} - T_{on} \frac{\omega_{on}}{\omega_{off}} \tag{C-35}
\]

Substituting (C-35) into (C-3) gives:

\[
T_e = \left(1 - \frac{\omega_{on}}{\omega_{off}}\right) T_{on} + \frac{2\pi}{\omega_{off}} \tag{C-36}
\]

As can be seen, (C-36) is the same as (C-21) which is for the situation \(0 \leq \omega_{on} \times T_{on} < \pi\), so the equivalent capacitance \(C_e\) finally derived for the situation \(\pi \leq \omega_{on} \times T_{on} < 3\pi/2\) will also be the same as in the situation \(0 \leq \omega_{on} \times T_{on} < \pi\).

**C.4 The Situation when \(3\pi/2 \leq \omega_{on} \times T_{on} < 2\pi\)**

The situation when \(3\pi/2 \leq \omega_{on} \times T_{on} < 2\pi\) is shown in Fig. C-5. Similar to the above two situations, the overall strategy to get the equivalent capacitance \(C_e\) in this situation is also by calculating the duty cycle \(T_e\), and assuming that the conduction period of the switch \(T_{on}\) has already been known. So based on (C-3), task left is only to find \(T_{off}\).

![Fig. C-5. The situation when 3π/2 ≤ ωon × T on < 2π.](image-url)
Appendix C

As can be seen in Fig. C-5, $T_{\text{off}}$ can be expressed by (C-37):

$$T_{\text{off}} = t_0 \quad \text{(C-37)}$$

Based on:

$$h = A_e \sin \omega_{\text{off}} t_0 \quad \text{(C-38)}$$

“$t_0$” can be found as:

$$t_0 = \frac{\arcsin \left( \frac{h}{A_e} \right)}{\omega_{\text{off}}} \quad \text{(C-39)}$$

Now the task left is how to find “$h$”.

As can be seen in Fig. C-5, the absolute value of “$h$” is the Y-coordinate of the sinusoidal wave with the frequency of $\omega_{\text{on}}$ at the point $t_0$. Taking “$t_1$” as the origin of this sinusoidal wave with the frequency of $\omega_{\text{on}}$, the X-coordinate of $t_0$ is $T_{\text{on}}$. Substituting $-T_{\text{on}}$ into the expression of a sinusoidal wave with the frequency of $\omega_{\text{on}}$ gives:

$$h = A_e \sin (-T_{\text{on}} \omega_{\text{on}}) = A_e \sin (2\pi - T_{\text{on}} \omega_{\text{on}}) \quad \text{(C-40)}$$

Substituting (C-40) into (C-39) gives:

$$t_0 = \frac{2\pi - T_{\text{on}} \omega_{\text{on}}}{\omega_{\text{off}}} = \frac{2\pi}{\omega_{\text{off}}} - \frac{\omega_{\text{on}}}{\omega_{\text{off}}} T_{\text{on}} \quad \text{(C-41)}$$

Substituting (C-41) into (C-37) gives:

$$T_{\text{off}} = \frac{2\pi}{\omega_{\text{off}}} - \frac{\omega_{\text{on}}}{\omega_{\text{off}}} T_{\text{on}} \quad \text{(C-42)}$$

Substituting (C-42) into (C-3) gives:
As can be seen, (C-43) is the same as (C-21) and (C-36) for the above two situations, so the equivalent capacitance $C_e$ finally derived for this situation will also be the same as in the previous two situations.
References


