FPGA based Acceleration of FDAS Module for Pulsar Search

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Introduction

The Square Kilometre Array (SKA[1]), currently in the pre-construction phase, will be the world largest telescope array for radio astronomy. The Fourier domain acceleration search (FDAS) module is the sub-module of the Non-imaging Processing Pulsar Search Sub-element (NIP PSS) of SKA1-MID Central Signal Processor (CSP) element. The purpose of it is to minimize the effect of potential cyclic Doppler shift on pulsar signals. Its main function is to execute pre-processed input, by using a correlation technique and then identifying pulsar candidates[2].

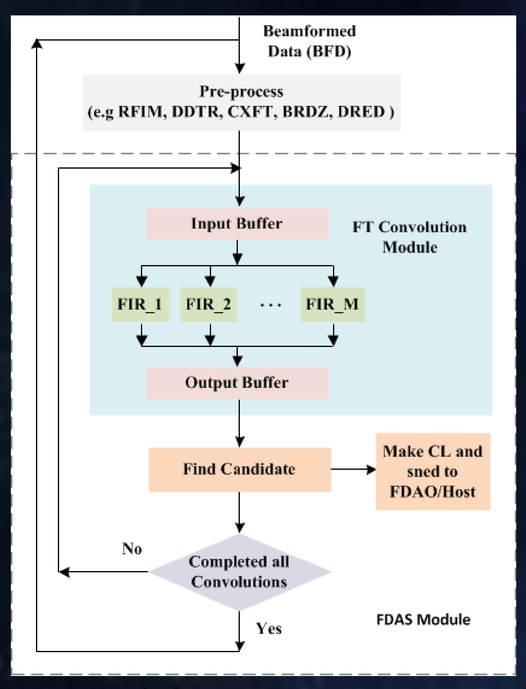

Fig 1. Signal Flow Diagram of FDAS Module

First Performance Estimate

Tab 1. FDAS Module Parameters

Parameter	Description	Value
B	Number of beams	1000~2000
N	Number of complex samples in one data group	2^{22}
M	Number of templates	84
K	Number of average template length	222
W	Overall workload for one beam	6.26 x 10^{11}
P	Performance needed to execute one beam	7.11*TFLOPS*
t_{limit}	Time of executing one sample group of all beams	88*ms*
N_{FPGA}	Number of needed FPGAs to execute one beam	

- Maximum Performance Method:
  $N_{A7\ FPGA}$=65
- Parallelisation of Multiplication Method:
  N_{A7_FPGA}=59

Relaxing Requirements

Tab 2. Influence of Different Relaxation Methods

Factors	Relaxation Methods	Reduced Number
Precision	16+16-bit fixed-point	54.69%
Input Length	$\frac{N}{2}$, x 8	50.77%
Templates # and Length	$\frac{N}{2}\Sigma K_i$	49.23%
Time Limit	$2t_{limit}$	49.23%

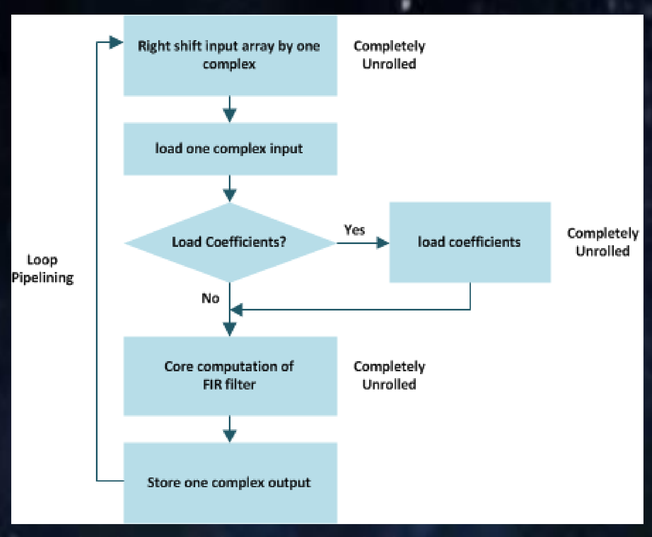

Fig 2. Single Work-item Convolution Kernel Structure

Optimization Techniques

- Regularity in Coefficients
  - Symmetric
  - Conjugate Roots
- Common Sub-expression Elimination (CSE)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H_{n-1}	0	0	1	1	1	0	1	0	1	1	1	1	1	0	1	0
H_n	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0
H_{n+1}	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	1

Fig 3. Example of General 3-bit Binary based Horizontal CSE[3]

Results

- Altera SDK for OpenCL[4] version 15.0.0.145
- Terasic DE5 Board featuring an Altera Stratix V GX FPGA (5SGXEA7N2F45C2)
- 3.7GHz Intel Core i7-4820K CPU, 32GB RAM and SSD
- Ubuntu 14.04 LTS 64-bit

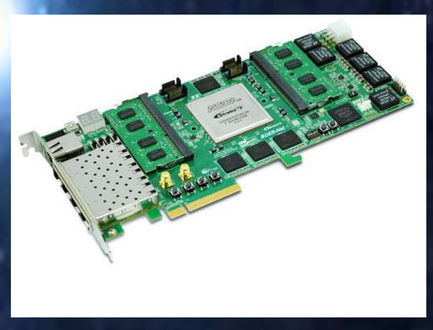

Fig 4. Terasic DE5 Board[5] with Altera Stratix V GXA7 FPGA

Results (Cont'd)

- Performance of general 64-tap FIR filter kernel: 110*GFLOPS*, 80x speedup
- The performance of fixed-point kernel is higher than that of SPF kernel
- By applying all the relaxation methods, up to 93% FPGAs can be saved
- Performance of Conjugate root kernel has 1.5x speedup

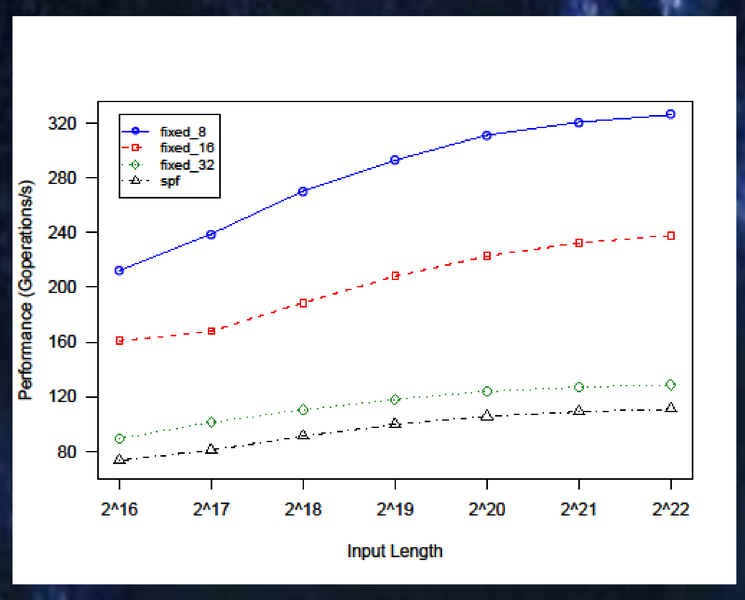

Fig 5. Performance Comparison of SPF Kernel and Fixed-point Kernels

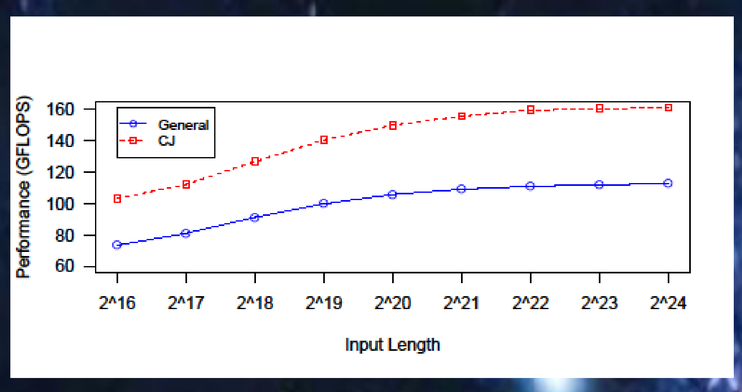

Fig 5. Performance Comparison of General Kernel and Conjugate Roots Kernel

Discussion

- OpenCL based Altera FPGA development is applied
- The number of DSP blocks is a great barrier for SPF multiplications
- Loop pipelining and complete unroll of single work-item kernel are two main factors to achieve high performance
- Future focus is on implementation of large-tap FIR filter and optimization techniques.

Reference

1. http://www.skatelescope.org/
2. S. M. Ransom, S. S. Eikenberry, and J. Middleditch, "Fourier techniques for very long astrophysical time-series analysis," *The Astronomical Journal*, vol. 124, no. 3, p. 1788, 2002.
3. I. Hatai, I. Chakrabarti, and S. Banerjee, "An efficient constant multiplier architecture based on vertical-horizontal binary common sub-expression elimination algorithm for reconfigurable fir filter synthesis," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 62, no. 4, pp. 1071–1080, 2015.
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