Time and Frequency Domain Fault Detection in VSC Interfaced Experimental DC Test System

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***Abstract*—The rapid discharge of DC-link capacitor of the voltage source converter (VSC) based DC system is the primary indication of the fault condition. Apart from the time-domain analysis, frequency-domain analysis of fault current could also be utilized for DC fault detection as the rapidly rising fault current is expected to have high frequency components. This paper proposes two fault detection methods and compares their performances with wavelet transform (WT). The first method is the time-domain analysis of the DC-link capacitor discharge and is termed as capacitive discharge (CD) technique. The relationship between the DC line current and behavior of DC-link capacitor is measured in term of correlation coefficient, whose value can be used to establish a fault basis. The second method is the frequency domain based short-time Fourier transform (STFT) which is used for quantitative analysis of high frequency components in the fault current. These methods are extensively analyzed and compared using a scaled down VSC-based DC system experimental test setup. Comparison has been done based on fault detection time, sensitivity to fault parameters, influence of sampling frequency and computation speed. Furthermore, the selectivity of the fault detection methods is studied on the multi-terminal DC systems of two different topologies (ring and radial), modeled in PSCAD/EMTDC. The experimental and simulation results substantiate the applicability of all the methods to the DC system. Brief comparative analysis with *di/dt* method is also presented to highlight the advantages of proposals.**

***Index Terms*—Fault detection, DC fault, VSC, wavelet transform, DC-link capacitor, short-time Fourier transform**

I. Introduction

Growing energy demand has taken the conventional power system in new direction. With the development of the power electronic converters, the research interest of the VSC based DC power system with application in high-voltage DC (HVDC) has been increasing in recent years. The main reasons being independent control of active and reactive power, easier integration of renewable energy and asynchronous generation sources, with improved input current profiles [1]. However, the DC protection still remains as a critical issue impeding the implementation of meshed DC grid.

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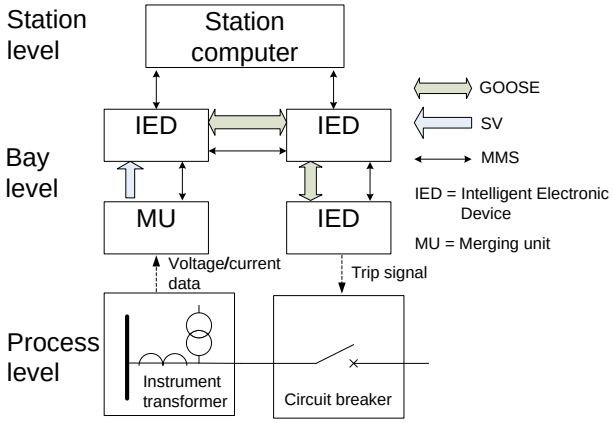


Fig. 1. Example of communication structure in substation according to IEC 61850.

Clear understanding of DC fault detection is required to decide on requirement for communication speed in order to achieve substation automation. While such standard for DC system is still missing, it can borrow the existing framework from IEC 61850 which has served for AC system since 2004 [2]–[5]. In the standard, basic protocol to transfer data between the products from different vendors is defined. There are three types of messages: Manufacturing Mass Specification (MMS), Sampled Values (SV) and Generic Object Oriented Substation Event (GOOSE). Voltage and current data is exchanged in the form of SV between instrument transformer and intelligent electronic device (IED) through merging unit (MU). Then, IED monitors the data and dispatches tripping signal to circuit breaker through GOOSE when fault occurs. Fig. 1 illustrates the communication structure within a substation. IEC 61850 outlines that the transmission time for GOOSE and SV has to be about 3 ms. As for DC system, the speed requirement has not been defined, but arguably the total time delay should be in the order of 1 ms. For this reason, it is empirical to have the fault detection algorithm that can support such a stringent requirement. Apart from speed, the algorithm has to be selective and robust.

DC fault can be identified by the time- and frequency-domain analysis of the DC current. Direct measurement of current is a simple and straightforward method to determine the occurrence of DC fault in time domain [6], [7]. In this method, the DC current is continuously monitored on each DC line and is compared with a threshold. The current derivative (di/dt & d^2i/dt^2) based time-domain analysis of DC current has also been proposed [8]–[10]. In addition to current, Sneath [11] presented a method based on the rate of change of DC

TABLE I
COMPARISON OF FAULT DETECTION METHODS FOR DC TRANSMISSION SYSTEM.

	Method	Advantage	Disadvantage	Ref.
Time domain	Direct measurement	1. Computationally simple	1. Inability to discriminate faulted line in MTDC	[6], [7]
	Rate of change	1. Offer good discrimination without communication	1. Hard threshold required 2. Vulnerable to noise	[8]–[11]
	Traveling wave	1. Highly fast and accurate	1. High sampling rate required 2. Difficult to be implemented on real time	[12], [13]
	Pattern recognition	1. Simple, accurate	1. Large training data set required	[14]
	Capacitor discharge	1. Versatile, independent of hard threshold 2. High tolerance towards influence of fault parameter	1. Dependent on existence of DC-link capacitor	*
Frequency domain	Wavelet transform	1. Accurate 2. Immune to noise	1. High computational burden 2. Filtering introduces time delay	[15]–[17]
	Short time Fourier transform	1. Fast, accurate 2. Mature in embedded system domain	1. Vulnerable to noise	*

* Presented in this paper

voltage. Although these methods offer good discrimination, they are vulnerable to the noise present in the real fault signals. The application of traveling wave to determine the faulted line in a multi-terminal DC system was studied [12], [13]. Farshad proposed a method by comparing the measured voltage with the already known signal [14]. The reference signals are obtained through iterative trainings, considering all possible fault scenarios. As for detection in frequency domain, wavelet transform (WT) has been prominently featured in literature [15]–[18]. This signal processing tool is able to capture high frequency content in the rapidly changing DC fault current. Most of the existing proposals of fault detection only offer theoretical analysis with focus on simulation results. It would be interesting to re-evaluate their effectiveness on real fault signal, in which the noise will become part of the picture.

Two novel fault detection methods, based in time and frequency domains, are presented in this paper. The first method monitors the behavior of DC-link capacitor discharge at the converter station [19]. During pole-to-pole DC fault, the capacitor will discharge immediately and generate large current to the fault point through the DC lines. This phenomenon can be translated into useful information to determine the occurrence of DC fault. The discharging process is independent of the fault parameters (resistance and location), hence this method is very robust. The second method approaches the DC fault detection by using short time Fourier transform (STFT) [20]. The STFT operates over a fixed window length which can provide precise frequency content information for a specified window size, compared to WT which targets certain frequency band. From the implementation point of view, Fourier transform has been well-adapted in the embedded system domain making it a possible alternative to WT. The comparison among the fault detection methods discussed here is summarized in Table I.

A comparative study using WT [21] as benchmark is presented that highlights the advantages of proposals in terms of speed, robustness and selectivity. The fault detection methods are validated by the DC fault current signals obtained from the point-to-point DC experimental test-setup. The ability to identify and differentiate the faulted line in a multi-terminal DC (MTDC) system is also presented in this paper. For this study, the fault signal is obtained from the simulation in PSCAD/EMTDC, as it is unfeasible to create a MTDC setup in laboratory. Furthermore, the parameters influencing the detection speed and computational burden of each method are also discussed. The contribution of this paper can be summarized as follows:

- Analytical calculation of DC fault current is verified with experiment, good agreement is obtained.
- Proposal of CD method to detect fault by monitoring behavior of DC-link capacitor is presented. It is simple, fast and robust, making it a potential alternative to the existing fault detection methods in literature.
- STFT method, which is computationally efficient for implementation, is applied on fault study of DC system.
- Performance comparison with relatively established WT and *di/dt* is presented. These methods are tested on real fault signal and multi-terminal DC model.
- Performance assessment framework is developed using the indices that will be in the interest of future standard, such as detection speed, fault parameter dependency, influence of sampling frequency and computational time.

The remainder of the paper is structured in the following manner. In Section II, the fault analysis, experimental & simulation model of DC system are introduced. The working principles of the three fault detection methods are outlined in Section III. The performances of these method are evaluated and compared using the fault signals obtained from experiment and simulation, as presented in Section IV, followed by discussion on the *di/dt* method and result in Section V. Finally, conclusion is given in Section VI.

II. VSC-BASED EXPERIMENTAL DC SYSTEM AND MTDC SIMULATION MODEL

A. Fault Analysis

The DC faults in DC system can be broadly classified into pole-to-ground (PG) and pole-to-pole (PP) faults. The PP fault is illustrated in Fig. 2. For simplicity, the cable is represented by a π-model equivalent resistor and inductor. The PP fault can be thought as shorting upper to lower line via a fault resistor (R_f). L_{dc} and R_{dc} are the lumped parameters of the sectional line in which the fault current loop is formed. I_{dc} is the current injected from the rectified AC side. Fig. 2(a) shows the initial stage of the PP fault. Depending on the value of R_f, the analytical equation of fault current can be obtained in three different ways. Under the condition $R_{dc}+R_f > 2\sqrt{L_{dc}/C_{dc}}$, the solution will give an overdamped response. Using initial

conditions $V_{dc}(t_0) = V_0$ and $I_f(t_0^-) = I_0$, the fault current is represented in (1).

$$I_f(t) = Ae^{m_1 t} + Be^{m_2 t}, \tag{1}$$

where, δ_1=$\frac{R_{dc}+R_f}{2L_{dc}}$, ω_0=$\sqrt{\frac{1}{L_{dc}C_{dc}}}$, ω_1=$\sqrt{\omega_0^2 - \delta_1^2}$, $m_{1,2} = -\delta_1 \pm \sqrt{\delta_1^2 - \omega_0^2}$, $B = \frac{m_1 m_2}{m_1+m_2}\left(CV_0 - \frac{I_0}{m_1}\right)$ and $A = I_0 - B$.

The DC voltage (V_{dc}) reaches zero when the charges of DC-link capacitor (C_{dc}) are depleted. Now, as shown in Fig. 2(b), the fault current path switches to the three phase-legs of the freewheeling diodes as the corresponding IGBTs are already blocked. As the line inductor (L_{dc}) does not allow sudden change of current, the initial current for this stage is $I_f(t_1) = I'_{f0}$. The circuit is now reduced to a RL circuit with the expression of fault current given as:

$$L_{dc}\frac{\mathrm{d}I_f}{\mathrm{d}t} + R_{dc}I_f = 0. \tag{2}$$

The first order differential equation is solved for:

$$I'_f(t) = I'_0 e^{-\frac{R_{dc}}{L_{dc}}t}, \tag{3}$$

$$I_{D1}(t) = I_{D2}(t) = I_{D3}(t) = I'_f(t)/3. \tag{4}$$

B. Experimental Test System

Laboratory-scale experimental setup of DC system is developed to carry out the steady-state and DC fault studies. This setup aims to replicate the actual DC system operation at scaled-down voltage level. Fig. 3 shows the schematic block diagram of the setup and real hardware. The experiment draws 415 V supply from laboratory and it is stepped down to 85 V (line-to-line rms) by using autotransformer. *VSC1* is assigned to control DC voltage, maintaining at the level of 250 V. *VSC2* is the AC voltage controller, supplying power to 3-ϕ AC load at 50 V. The voltage and current on AC and DC side are measured and converted to signal level using hall effect voltage ($\pm$ 500 V to $\pm$ 15 V) and current ($\pm$ 10 A to $\pm$ 4 V) transducers. These signals are required for the control algorithm developed in Real-Time Interface (RTI) of dSPACE 1103 controller. Then, the pulse-width modulation (PWM) will be generated and fed into the gate driver of the VSCs. All parameters of the setup are given in Table II.

The DC fault involving ground, such as PG fault, is unfeasible to be performed in the experiment. This kind of fault introduces current to the shared earth in laboratory, which might result in tripping of the main CB, creating unnecessary nuisance to other lab users. Thus, only PP fault is studied in this paper. The positive and negative poles of the DC line is short-circuited via a power resistor, which helps to dissipate the energy of fault current. The resistance is adjustable from 1 Ω to 16 Ω. The experiment under steady-state condition is shown in Fig 4(a), recorded in Teledyne LeCroy oscilloscope. Overall, the control structure is functioning normally which could be observed by sinusoidal voltage (V_{a1}) and current (I_{a1}) at generation side; constant DC-link voltage V_{dc1} (250 V) and DC current I_{dc1}.

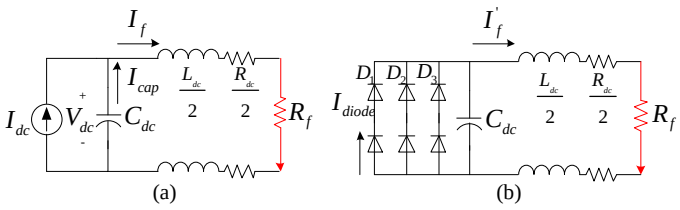


Fig. 2. Equivalent fault circuit. (a) Stage 1: Capacitor discharge, (b) Stage 2: Diode freewheeling stage.

TABLE II
EXPERIMENT SETUP PARAMETERS

Parameters	Values
Supply voltage	3ϕ, 415 V_{rms} , 50 Hz
3ϕ AC Protection Board	40 A, B Type, TP MCB with Shunt trip
3ϕ Variable Transformer	30 kVA, (0-415) V
Converters (VSC1, VSC2)	30 kVA, 400 V
DC Capacitor	C_{dc} = 2350 μF,
DC Bus Voltage	V_{dc} = 120 V,
DC MCB	C60H-DC, C 4 A
Interface Filter Parameters	R_f = 0.1 Ω, L_f = 10 mH
Linear Load	R_l = 20 Ω
Variable Power Resistor	5000 W, (1-16) Ω
DC Solid State Relay	D2D40, 200 V, 40 A
Sampling frequency	10k Hz

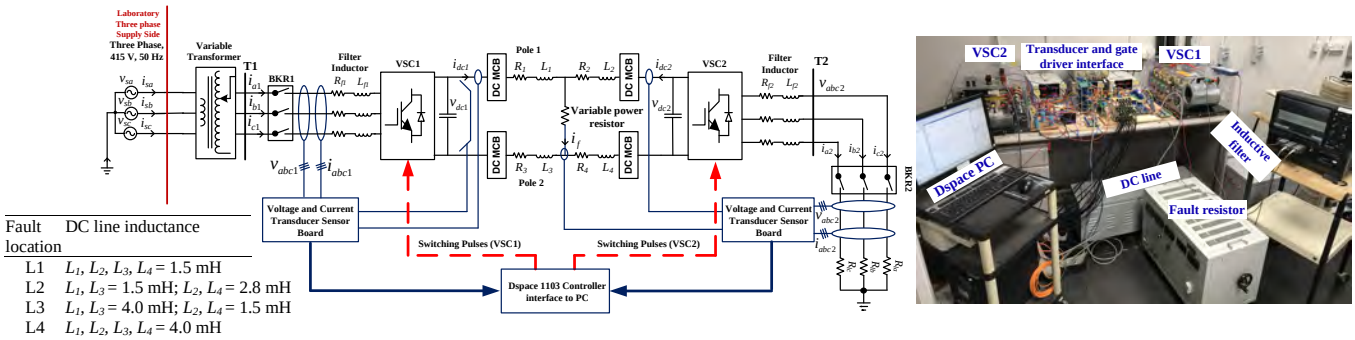
Fig. 4(b) shows the experimental result of 2 Ω PP fault. During steady-state, I_{dc1} and I_{dc2} are 1.5 A but opposite polarity. The PP fault causes the DC currents to increase to 23.5 A. Meanwhile, the DC voltage decreases sharply as a result of the PP fault, signifying the discharging process of the DC-link capacitor. After it is fully discharged, I_{a1} begins to dominate the fault current.

I_{dc1} from experiment is validated with the analytical calculation from (1) and the result is given in Fig. 5. The analytical solution yields 24.01 A peak. With the good agreement between the two results, it is now evident that the DC-link capacitor discharge dominates the first few time-instants of the fault current.

C. Simulation Test System

It is equally important to assess the application of the fault detection method on MTDC system. Due to cost and technical constraint, it is difficult to build such MTDC hardware setup in laboratory, hence it is entirely modeled in PSCAD/EMTDC instead. Fig. 6 depicts the two MTDC grid topologies to be used as test models. They consist of 4 terminals (*VSCi*, i=1,2,3,4). *VSC1* works as the fixed DC voltage controller, the rest being fixed active power controller. The DC lines (*Lij*, *i,j*=1,2,3,4) are represented as single line, and the length is 200 km. The DC currents (I_{dcij}, i, j=1,2,3,4) are measured at each terminal. PP fault on line *L12* is denoted by F_{dc12}.

In the ring network, each VSC station is connected to two neighboring stations, resulting in two DC lines sharing single bus. Although the radial network is more economical in a sense that each station is only connected to one DC line, the downside is that the power exchange is less flexible as compared to ring network. Besides selectivity issue, study has



Fault location	DC line inductance
L1	L_1, L_2, L_3, L_4 = 1.5 mH
L2	L_1, L_3 = 1.5 mH; L_2, L_4 = 2.8 mH
L3	L_1, L_3 = 4.0 mH; L_2, L_4 = 1.5 mH
L4	L_1, L_2, L_3, L_4 = 4.0 mH

Fig. 3. Experimental hardware testbed.

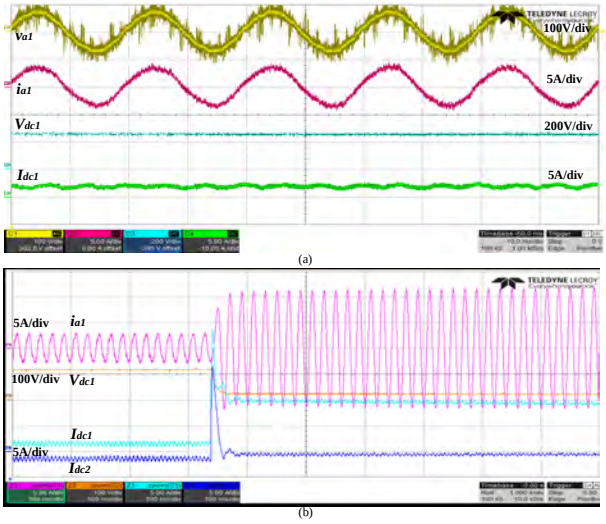


Fig. 4. Experimental result for (a) steady state and (b) PP fault with R_f=2 Ω.

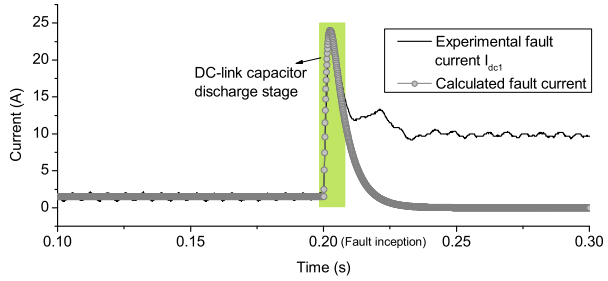


Fig. 5. Comparison between experimental fault current and analytical calculation.

also shown that radial network tends to yield comparatively higher fault current for a given fault location [22]. In the section that follows, it will be presented how the selectivity issue can be overcome when the proposed fault detection methods are applied.

III. Fault Detection Techniques

A. Wavelet Transform Method

1) Concept: Wavelet transform (WT) is a signal processing technique that analyzes non-stationary signal in time and

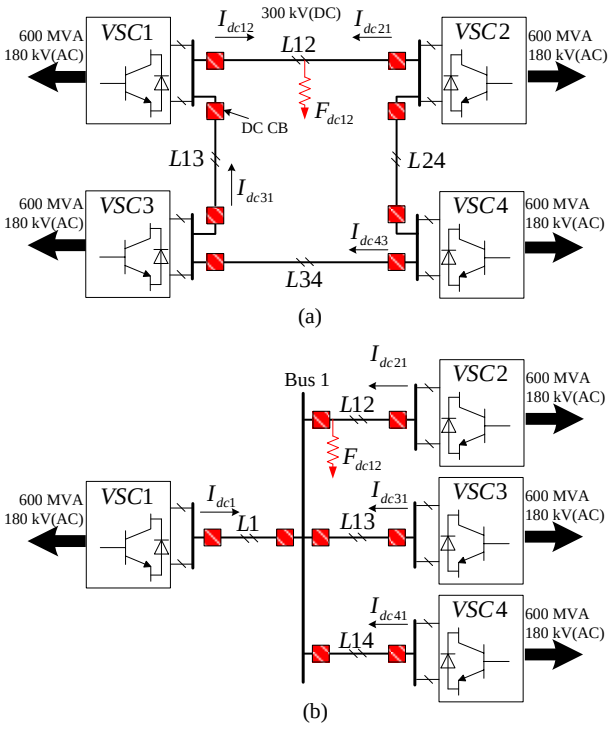


Fig. 6. Two MTDC grid topologies under investigation in PSCAD/EMTDC, (a) ring grid and (b) radial grid.

frequency domain. The window size in WT changes automatically in response to the dynamics of the input signal. Hence, it is able to capture the abrupt change. WT breaks up a signal into the shifted and scaled versions of the original (or mother) wavelet, allowing for simultaneous time and frequency analysis.

2) Implementation: The multiresolution signal decomposition (MSD) [23] technique is applied to decompose a given signal into detailed and smoothed versions. Let $x[n]$ be a discrete-time signal, the MSD technique decomposes the signal in the form of wavelet coefficient at scale 1 into $C_1[n]$, the smoothed (time-domain view), and $D_1[n]$, the detailed (frequency-domain view) coefficients. The decomposition process can be iterated, with successive approximations being decomposed in turn, so that the original signal is broken down into many lower resolution components. MSD technique can

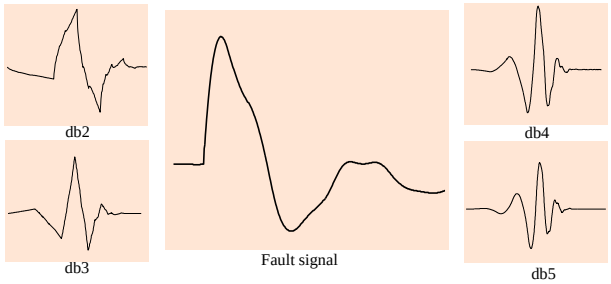


Fig. 7. Fault signal and Daubechies wavelet (db) of varying orders.

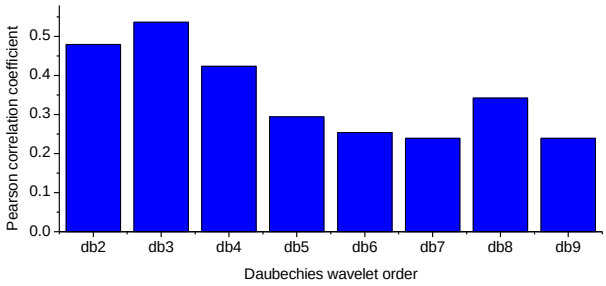


Fig. 8. Correlation coefficient between fault signal and Daubechies wavelet of order 2-9.

be realized with the cascaded quadrature mirror filter (QMF) banks [24]. For example, using 4-scale decomposition, the original signal can be represented as:

$$x[n] = C_4[n] + D_4[n] + D_3[n] + D_2[n] + D_1[n]. \quad (5)$$

The decomposition level has to be selected such that it is able to target the frequency range generated by the fault. For the sampling rate of 10 kHz, the frequency bands corresponding to each level of decomposition is presented in Table III. It is known that the frequency content ranging [416 833] Hz is pronounced in the event of short-circuit fault [25], [26]. In our case, the 4th level detail coefficient will be the most suitable to localize the frequency of interest.

Daubechies wavelets are a family of orthogonal compact wavelets that are useful to analyze short and fast transient. The wavelets of varying orders are available, as shown in Fig. 7. For the fault detection application, the most optimum wavelet is the one whose center frequency matches that of the fault pattern. Alternatively, one can calculate the Pearson product-moment correlation coefficient between the wavelet and the fault pattern, as expressed in (6), and the optimum wavelet is chosen based on the highest correlation coefficient [27].

$$r = \frac{\sum_{i=1}^{n}(X_i - \bar{X})(Y_i - \bar{Y})}{\sqrt{\sum_{i=1}^{n}(X_i - \bar{X})^2 (Y_i - \bar{Y})^2}} \quad (6)$$

where X_i and Y_i are the data sets of the fault signal and the wavelet respectively, their corresponding averages being $\bar{X}$ and $\bar{Y}$.

In this case, X_i is the fault signal as depicted in Fig. 7, while Y_i corresponds to the chosen Daubechies mother wavelet.

The correlation coefficients between the fault signal and the Daubechies mother wavelet of varying order ($db2 - db9$) are computed and depicted in Fig. 8. It is found that $db3$ provides the best match among these candidates for the given fault pattern.

TABLE III
FREQUENCY BAND AT EACH DECOMPOSITION LEVEL

Decomposition level	Frequency band (Hz)	
	Approximation	Detail
1	0 - 2.5k	2.5k - 5.0k
2	0 - 1.25k	1.25k - 2.5k
3	0 - 625	625 - 1.25k
4	0 - 312.5	312.5 - 625
5	0 - 156.25	156.25 - 312.5

B. Capacitive Discharge-based Method

1) Concept: DC fault results in DC voltage drop, triggering the discharging of DC-link capacitor. The proposed detection method attempts to identify DC fault by tracing the content of capacitive discharge in DC line current. To that end, it is assumed that the rising pattern of the DC fault current will resemble that of the discharging current of the DC-link capacitor at the instant of DC fault.

The signals required for this method are the line currents at the VSC terminal and the discharging current of the associated DC-link capacitor. These measurement can be locally obtained at each terminal itself, therefore the communication channel can be opted out.

Fig. 9(a-b) shows the DC line current and discharging current of the DC-link capacitor during PG and PP faults. In the system with symmetric monopole configuration in which the DC-link capacitors are mid-grounded, PG fault causes DC-link capacitor of faulted pole to inject its discharging current into the fault current. As a result, the fault current ($I_{dc}(+)$) and the discharging current of the top capacitor ($I_{cap}(+)$) will have matching rising slope. In contrast, the two currents in the (healthy) negative pole do not exhibit a parallel behavior. Such difference allows the proposed method to differentiate the type of DC fault by examining the patterns of the DC current and the discharging current of the DC-link capacitor.

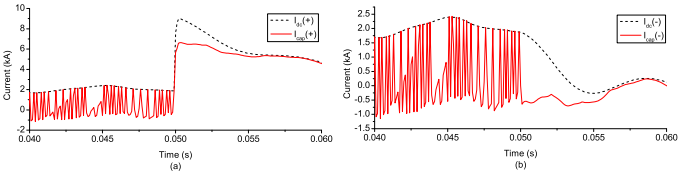


Fig. 9. Fault current and discharging current of DC-link capacitor during PG fault. (a) Positive pole currents; (b) Negative pole currents.

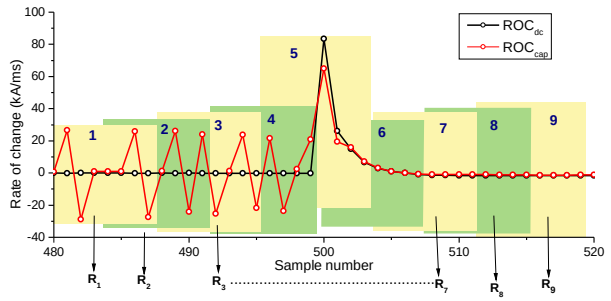


Fig. 10. Computation of correlation coefficient between ROC of fault current and DC-link capacitive discharge.

2) Implementation: To implement the CD method, the rising slope of DC current and DC-link capacitor discharge are computed. During steady-state, the DC-link capacitor undergoes periodical charging and discharging due to converter switching, while the DC current is constant and non-zero. In the event of DC fault. they will have matching rising patterns and equivalent rate of change (ROC). Hence, their ROCs will be compared, and the similarity is quantified by correlation coefficient, using (7).

$$R = \frac{1}{N}\sum_{i=1}^{N}\left(\frac{ROC_{dc,i} - \mu_{ROC_{dc}}}{\sigma_{ROC_{dc}}}\right)\left(\frac{ROC_{cap,i} - \mu_{ROC_{cap}}}{\sigma_{ROC_{cap}}}\right) \tag{7}$$

where μ and σ are mean and variance of the windowed sample.

Fig. 10 illustrates the process of computing the correlation coefficient. The windows denoted by $1, 2, 3...9$ contain fixed size samples from signals $ROC_{dc}(n)$ and $ROC_{cap}(n)$. Each window calculates the correlation coefficient, as represented by $R_1, R_2, R_3...R_9$. The correlation coefficient ranges from -1 to 1. The DC fault is detected as the correlation coefficient close to unity is obtained, whereas 0 means there is no correlation at all. So, for example, the fault emerges in the 5th window, resulting in equivalent ROC_{dc} and ROC_{cap}. In that window, we will get $R_5 \approx 1$. Wrong detection can possibly happen in the 1st window, as ROC_{dc} and ROC_{cap} in 4th through 6th sample show fairly similar correlation, even without noticeable sign of the DC fault. To resolve this, a threshold (ROC_{thr}) is set in order to correctly capture the surge of fault current.

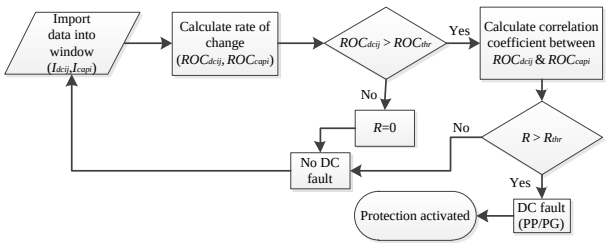


Fig. 11. Flowchart of the proposed method.

The working mechanism of the proposed method can be summarized in the flowchart shown in Fig. 11. The algorithm starts by loading data from the signal into window of predefined size. Within that window, the ROC of I_{dcij} and I_{capi} will be calculated. If the obtained ROC_{dc} is smaller than R_{thr}, the algorithm will return R=0, suggesting no fault condition, before proceeding to the next window. However, if it is larger than the threshold, there is a possibility that the DC fault has occurred. The calculation of R between ROC_{dc} and ROC_{cap} will be executed thereafter.

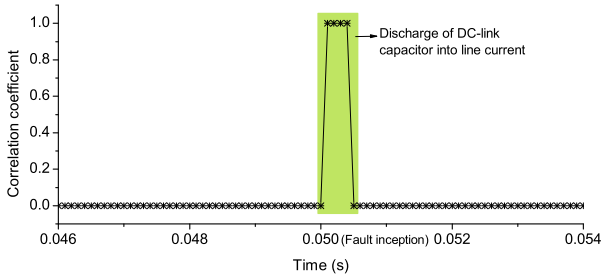


Fig. 12. Computation of R for fault current during pole-to-ground fault.

To illustrate the outcome of this method, the signal from Fig. 9(a) is exported to MATLAB for post-processing and the result is shown in Fig. 12. The algorithm yields a correlation coefficient close to 1 at the time when the $I_{dc}(+)$ and $I_{cap}(+)$ rise at the same rate. With that, it can be interpreted that the detection of DC fault succeeds.

C. STFT-Based Method

1) Concept: STFT is the Fourier Transform (FT) of a function $f(t)$ incorporating a real and symmetric window function $w(t)$, which is translated by time (τ) and modulated at frequency (ω). Mathematically, the continuous STFT of a function $f(t)$ is represented in (8).

$$F(\tau, \omega) = \int_{-\infty}^{+\infty} f(t)w(t-\tau)e^{-j\omega t}dt. \tag{8}$$

The equation above infers that the STFT determines the frequency components (ω) present in the local section of the signal as it changes over time (τ). In other words, it provides information of the frequency components existing in a signal as well as the time-instant at which the frequency emerges. As the fault signal evolves in an unpredictable way, the STFT is suitable to examine the change of frequency content caused by fault. Unlike WT, the window size of STFT is fixed which implies that a longer time window results in good frequency resolution at the expense of time resolution, and vice versa. The STFT provides quantitative analysis of frequency components which can not be inferred from WT analysis of DC fault current.

2) Implementation: To implement the discrete version of the STFT, the signal will be sampled with fixed sampling frequency and processed with the discrete Fourier transform (DFT), which can be efficiently computed using the fast Fourier transform (FFT) algorithm. Thus, (8) can be modified in discrete space yielding (9).

$$X[m,k] = \sum_{n=0}^{N-1} x[n]w[n-mH]e^{-i\frac{2\pi nk}{N}}, \tag{9}$$

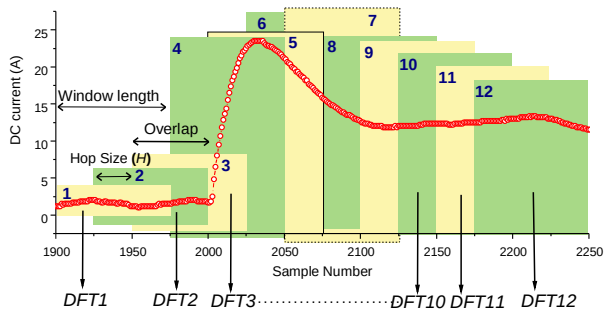


Fig. 13. Computation of STFT on fault signal.

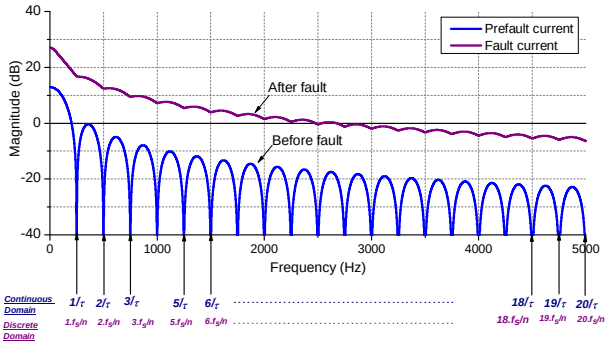


Fig. 14. Frequency spectrum of pre-fault and fault signal.

where, N=the number of FFT points, m=position of window, k=frequency index and H=hop size between successive windows.

There are several parameters that determine the property of the STFT:

1) *Sampling frequency (f_s)*: High f_s means more samples available for STFT analysis, contributing to better time and frequency resolution.
2) *Number of FFT points (N)*: N is typically at the power of 2. It reflects the frequency resolution in the STFT.
3) *Type of window function ($w[n]$)*: Different window functions have their unique frequency spectrum. Hanning window is utilized for fault detection here.
4) *Window length (n)*: Window length is proportional to the time resolution in the STFT output. As far as fault detection time is concerned, small window length is recommended. The length is typically at the power of 2.
5) *Hop size (H)*: H determines how much proportion of a window is overlapped with the successive one as it slides. Small H effectively helps to improve the time resolution. Here, H is chosen to be 2 samples.

Fig. 13 illustrates the operation of the STFT on the fault signal. A number of samples according to window length is captured and read into a window. In that window, the samples will be multiplied with window function ($w[n]$), subsequently proceeding to computation of the DFT. After that, the window is hopping to successive set of sample by H and DFT is computed again. The process repeats until it reaches the end of signal. The windows are denoted by $1, 2, 3...12$ and the corresponding outputs are $DFT1, DFT2, DFT3...DFT12$.

During normal operation, the DC current $I_{dc}(t)$ is presumably constant. Hence, the STFT of $I_{dc}(t)$ using rectangular window ($w[n] = 1$) can be written as follows:

$$|I_{dc}(\omega)| = \left| \int_{-\tau/2}^{\tau/2} I_{dc}(t) e^{-j\omega t} dt \right| = I_{dc} \left| \frac{sin(\omega\tau/2))}{\omega\tau/2} \right|. \quad (10)$$

It can be seen that the frequency spectrum of pre-fault current essentially resembles a *sinc* function. As shown in Fig. 14, it has the main-lobe with peak at a value depending on the steady-state DC current, and side-lobes that decrease in magnitude as it goes along with increasing frequency. The *sinc* function crosses zero periodically at frequencies denoted by $1f_s/n$, $2f_s/n$, $3f_s/n$...$20f_s/n$, or known as *zero-crossing frequency bins*. The frequency spectrum of the fault current is obtained from the DFT computation of 4th window in Fig. 13. The fault-induced transient injects high frequency content into the signal, causing the distortion across the side-lobes. The transition from pre-fault to fault demonstrates change in the frequency spectrum, one observable sign is the increased magnitude at each zero-crossing frequency bin. Using this as an indicator, we design a fault detection method based on STFT.

IV. Experimental and Simulation Validation

The proposed fault detection methods are validated and compared using the experimental and simulation results. Their performance is evaluated by considering the procedure shown in Table IV.

TABLE IV
Procedure of Comparison of Various Performance Indicators

Performance Indices	Procedure	Test System
Detection Time	F_{dcl2}, R_f=2 Ω, Location=L1, f_s=10 kHz	Experiment
Sensitivity to Fault Resistance	F_{dcl2}, R_f=2∼10 Ω, Location=L1, f_s=10 kHz	Experiment
Sensitivity to Fault Locatione	F_{dcl2}, R_f=2 Ω, Location=L2, L3, L4, f_s=10 kHz	Experiment
Selectivity in MTDC system	F_{dcl2}, R_f=0.1 Ω, f_s=10 kHz	Simulation
Influence of Sampling Frequency	F_{dcl2}, R_f=2 Ω, Location=L1 f_s=[10, 8, 5] kHz	Experiment
Computation Time	F_{dcl2}, R_f=2 Ω, Location=L1, f_s=10 kHz	Experiment

As per discussion in Section III, the properties for each fault detection method are:

- Wavelet transform (WT) method: $\psi[n]$ = db3, 4th decomposition level
- Capacitive discharge (CD) method: ROC_{thr} = 1 kA/ms
- STFT method: $w[n]$ = Hanning, n = 32, H = 2.

A. Detection Time

Fig. 15 depicts the fault analyses of three fault detection techniques for the 2 Ω PP fault performed in experiment (I_{dc1} of Fig. 3). The fault inception time is 3 s.

For WT method (Fig. 13(a)), I_{dc1} generates the highest wavelet coefficient at 1878th sample number. So, at the 4th

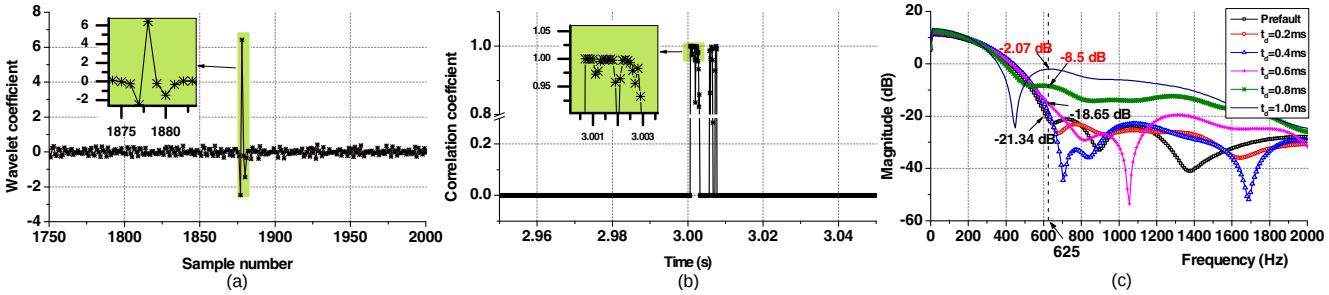


Fig. 15. Analysis of I_{dc1} for experimental PP fault by (a) WT method, (b) CD method, (c) STFT method.

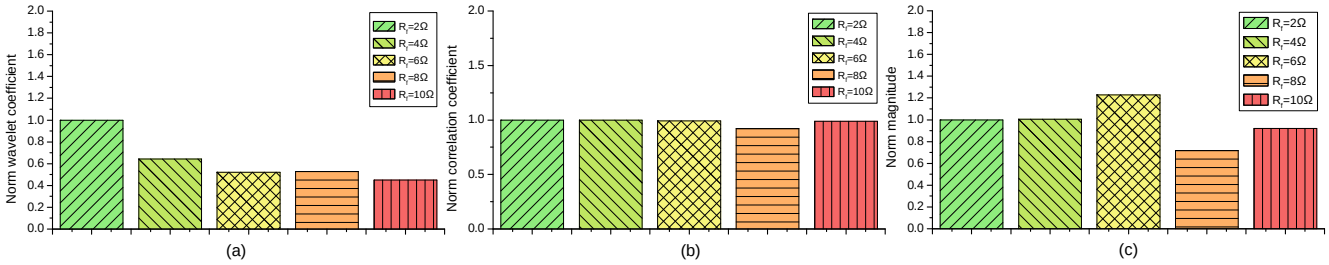


Fig. 16. Sensitiveness to experimental fault resistance (a) WT method, (b) CD method, (c) STFT method.

level of decomposition, the WT can be said to have identified the fault with the time delay (t_d) of 1.6483 ms. For CD method (Fig. 13(b)), the fault is detected at t_d=0.7 ms, at which time the correlation coefficient close to 1 is obtained. For STFT method (Fig. 13(c)), assuming that the trip setting for zero-crossing frequency bin is -10 dB, the fault is considerably detected at t_d=0.8 ms.

To sum up, the capacitive discharge method provides the fastest detection, closely followed by the STFT method. Because the WT method has to undergo 4 levels of filtering, it is logical that its detection time is comparatively longer.

B. Sensitivity to Fault Resistance

The rising slope and the peak magnitude of fault current are influenced by the fault resistance (R_f). Under the condition of high R_f, the fault signature can become too diminished that the fault detection might fail to capture it. Thus, it is important to assess the sensitivity to fault resistance of each fault detection methods.

Fig. 16 demonstrates how the fault detection methods perform on PP faults with various fault resistances. The parameter is now normalized using the R_f = 2 Ω as the base. It is clear that the wavelet coefficient follows a downward trajectory as the fault resistance is increased. STFT method appears to be relatively more robust, but the influence of fault resistance is visible, given that it suffers drop in sensitivity in detecting R_f = 8 Ω. The wavelet coefficient and the magnitude of zero-crossing frequency bin are closely related to the fault-induced transient, therefore their performances is affected with high fault resistance. Because CD method only monitors the behavior of DC-link capacitor, it provides the most resilient detection. For all the fault resistances evaluated, the correlation coefficients consistently stay above 0.95.

TABLE V
SENSITIVENESS OF EACH METHOD TO VARIOUS FAULT LOCATION.

Fault location	WT method	CD method	STFT method
	Norm. coef.	Norm. coef.	Norm. mag.
L2	1.13669	0.9993	0.9694
L3	0.481297	0.90128	0.5294
L4	0.419264	1.0001	0.6718

C. Sensitivity to Fault Location

Three fault locations (L2, L3, L4) are adjusted in the experiment by changing the DC line inductance, which is depicted in Fig. 3. The fault signal will be processed with the three fault detection methods to evaluate their sensitivity to this fault parameter.

Table V summarizes the performance of the three fault detection methods under various fault locations. The parameters are normalized using L1 as the base. PP fault in L2 is detected by all methods with reasonable reliability. In L3 and L4, where the fault is now further away from *VSC1*, I_{dc1} has less steep rising slope and lower peak magnitude. WT and STFT methods are affected by this change of location, both seeing the parameters drop by almost half. The normalized correlation coefficient, on the other hand, is maintained above 0.9 in all cases. This shows that CD method is the most resilient to the influence of fault location.

D. Selectivity in MTDC System

1) Ring network: Fig. 17 shows the fault analyses using the three fault detection methods for F_{dc12} in the MTDC ring grid (see Fig. 6(a)). The fault is set to occur at 0.25 s. I_{dc12} and I_{dc21} are the line currents directly affected by the fault while I_{dc31} and I_{dc43} are the *healthy* currents.

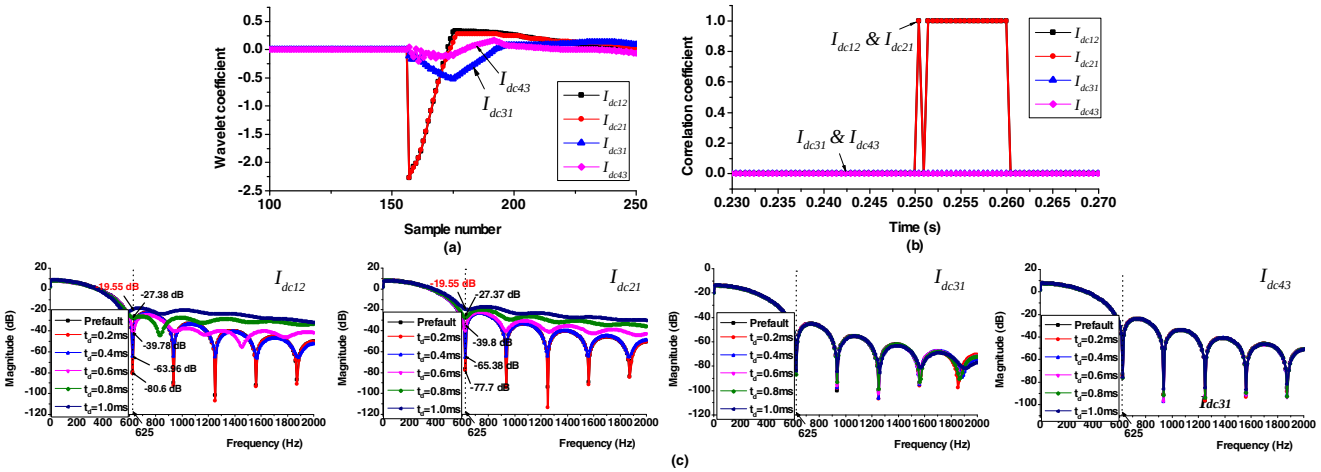


Fig. 17. Fault analyses in simulated MTDC ring network. (a) WT method, (b) CD method, (c) STFT method.

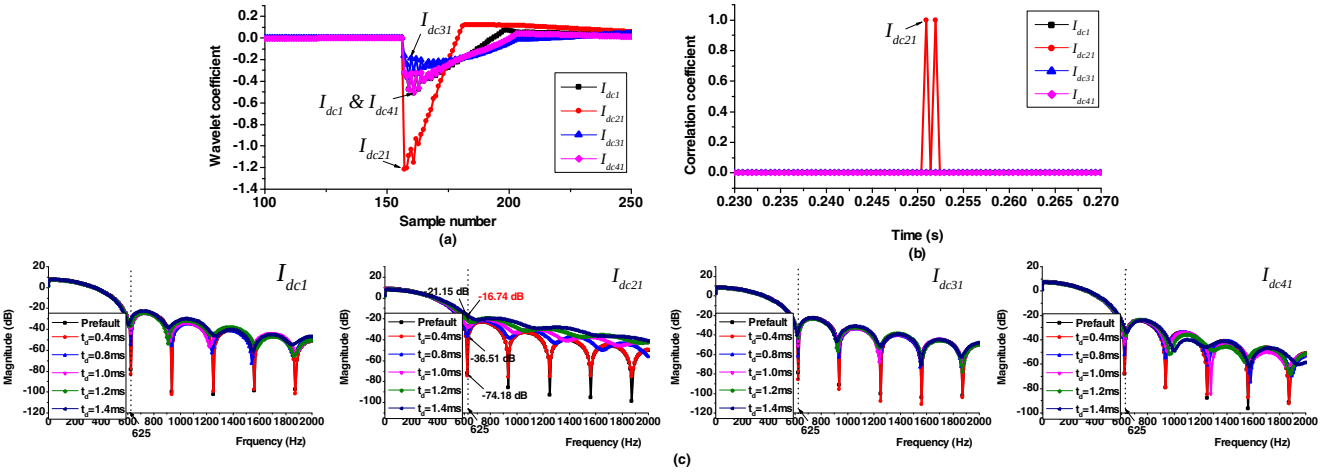


Fig. 18. Fault analyses in simulated MTDC radial network. (a) WT method, (b) CD method, (c) STFT method.

WT, CD and STFT methods are able to detect the fault in their own way. I_{dc12} and I_{dc21} record high wavelet coefficient at 157th sample (equivalent to 0.2509 s). The DC-link capacitors at *VSC1* and *VSC2* release the charges into the two line currents, respectively, resulting in correlation coefficient close to one at the instant of fault. Assuming -20 dB as the trip setting, STFT method detects the fault with time delay of 1 ms, as the zero-crossing frequency bin increases in magnitude to -19.55 dB for both currents. As for I_{dc31} and I_{dc43}, the three detection methods do not show any noticeable sign of fault.

2) Radial network: The similar fault (F_{dc12}) is created in the MTDC radial network. To present a challenging fault condition, the fault is now placed at the line termination of *L12* near Bus 1. Because there is no electrical difference as seen from *VSC1*, *VSC3* and *VSC4* (100 km away) as the fault is very close to the same bus they are connected to, the proposed methods would render all the terminals to trip their associated CBs. As a result, selectivity issue might arise.

One way to impose the "electrical distance" between two DC lines connected to Bus 1 is employing inductive fault current limiter (FCL). The size of FCL is selected based on the requirement of DC CB. For example, the ABB's DC CB is able to tolerate maximum current of 16 kA. Assume the operating time to be set as 2 ms, the rated current derivative is 8 kA/ms [28]. In this paper, 3 kA/ms is considered instead, which requires the FCL of 100 mH.

Fig. 18 shows the result with the FCL being employed. I_{dc21} exhibits the sign of DC fault when analyzed with the proposed methods. It yields high wavelet coefficient at the instant of fault. The high correlation coefficient obtained in CD method indicates the discharging of DC capacitor at *VSC2* to the fault point. The frequency spectrum of I_{dc21} becomes distorted at t_d=1.4ms, with the zero-crossing frequency bin crossing the trip setting, confirming that the fault is on line *L12*. As the other line currents show no sign of fault, their associated terminals will not proceed with protective action. Hence, it can be said that the employment of FCL helps improving the selectivity of the proposed method in radial network.

E. Influence of Sampling Frequency

The influence of sampling frequency (f_s) on the detection time delay is investigated here. The fault signals from the

experiment sampled in f_s=[10, 8, 5] kHz are processed with the proposed fault detection methods. The result is given in Table VI. The first sample that indicates the fault appears later with lower sampling frequency, resulting in longer detection time for all methods. CD method is able to detect the fault within 1 ms. For STFT method, there is no noticeable sign that the sensitivity drops due to lower sampling frequency. However, the performance of WT method is greatly compromised by lower sampling frequency, seeing the largest drop in sensitivity and longer detection time.

TABLE VI
INFLUENCE OF SAMPLING FREQUENCY.

f_s (Hz)	WT method		CD method		STFT method	
	Norm coef.	Time (ms)	Norm coef.	Time (ms)	Norm mag.	Time (ms)
10000	1.0	1.65	1.0	0.7	1.0	0.8
8000	1.332	2.05	0.99993	0.75	1.2153	1.3
5000	0.37064	4.89	1.00002	1.0	1.7620	2.0

F. Computation Time

The algorithms of the three fault detection methods are written in MATLAB R2015b and computed in the Intel Core i5 CPU with 4.0 GB of RAM. The average computation time to output a sample for WT, CD and STFT methods are 41.25 μs, 41.43 μs and 24.27 μs, respectively. In short, the STFT method is computationally efficient followed by WT and CD based methods. The requirement of cascade filtering in WT method and processing two signals in CD method (DC current and discharging current of DC-link capacitor) increase the burden on computation, resulting in longer calculation time.

V. DISCUSSION

It has been demonstrated that the DC fault detection can be approached by using capacitive discharge (time domain) and STFT (frequency domain). Their performances are compared with WT, showing that the proposals are better in most of the performance indices evaluated. Another well-established method but in time domain is using DC current derivative as the indicator.

Fig. 19 shows the result of *di/dt* method for the experimental fault signal. The raw signal has to be filtered to provide improved performance. The highest rate of change is obtained with time delay of about 0.75 - 0.92 ms, approximately similar to CD and STFT methods. The calculation of *di/dt* is computationally simple, as it takes 0.98 μs to generate the output (excluding filtering time). However, the rate of change decreases greatly from fault resistance 2 Ω to 10 Ω, suffering 48.64% drop in sensitivity. This suggests that the influence of fault parameter is a prominent issue for *di/dt* method. In this regard, the proposed methods offer better performance considering robustness.

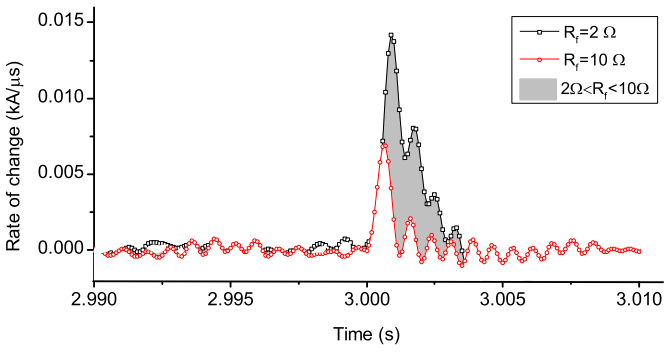


Fig. 19. Rate of change of DC current for fault experiment.

The following comments are cited on the proposed fault detection methods and difference in their performances:

1) The proposed CD and STFT methods identify faulted line in MTDC by only sourcing locally accessible measurement. From the technical point of view, the elimination of communication facility cuts down the complexity of designing protection system, as well as the cost. Besides that, current sensor alone is sufficient to provide the necessary measurement, instead of voltage sensor which is arguably more expensive due to size and added insulation.
2) Time domain-based method provides faster DC fault detection than its counterpart in frequency domain. In real-time application, the signal is essentially sampled in time domain. Hence, to analyze the signal in frequency domain using FFT, or multi resolution analysis for WT, involves convolution and complex number resulting in time delay. In this case, the fault signature is captured the fastest by the CD method.
3) The capacitive discharge, as a fault phenomenon itself, is unaffected by the fault parameters (resistance and location). Therefore, the CD method is very reliable with respect to fault detection. That being said, it can only work on the VSC-based DC system in which the DC-link capacitor is inherently available.
4) The experimental validation showcases the performance of each method in the presence of noise. The STFT method appears to be especially vulnerable to noise as it can be seen that frequency spectrum is already distorted to certain extent during normal operation, as opposed to the simulation result. To resolve this issue, one can consider to filter out the high order frequency component while preserving the one associated with fault.
5) The choice of sampling frequency is closely tied to the frequency to be targeted by WT and STFT, thus they experience drop in performance when the sampling frequency is reduced. CD method, on the other hand, is barely influenced by this factor. One would prefer to use lower sampling frequency for the reason of cost, hence CD method is the most economically effective in that sense.
6) The FFT algorithm allows the STFT method to execute the fault detection most efficiently. For WT method, the computational delay is caused by the cascaded filtering process. $db3$, which is used in this paper, has 6 coefficients in the filter. The algorithm to calculate the correlation coefficient in CD method (see (7)) involves

shifting signal along x-axis, in a fashion similar to cross correlation, resulting in high computational burden.

7) The CD method detects the fault by comparing the patterns of DC line current and capacitive discharge based on their mutual similarity, hence the same threshold is applicable in both experimental and simulation validations. In contrast, the WT and STFT methods adopt hard threshold, which means that the value tends to vary when used in different system.
8) The comparison and ranking of WT, CD and STFT methods are presented in Table VII.

TABLE VII
PERFORMANCE COMPARISON OF FAULT DETECTION TECHNIQUES.

Performance Indices	WT Method	CD Method	STFT Method
No. of Signals Required	1	2	1
Detection Time (1=fastest)	3	1	2
Sensitivity to Fault Resistance (1=most robust)	3	1	2
Sensitivity to Fault Location (1=most robust)	3	1	2
Selectivity in MTDC ring network	√	√	√
Selectivity in MTDC radial network	√	√	√
Influence of Sampling Frequency (1=least affected)	3	1	2
Average Computation Time (1=most efficient)	2	3	1

VI. CONCLUSION

Strict requirement for DC protection has to be supported by fast, accurate and robust fault detection algorithm. In this paper, two fault detection methods based on time-domain (capacitive discharge (CD) method) and frequency-domain analysis (short-time Fourier transform (STFT)) have been proposed. The correlation coefficient is adopted to trace the content of capacitive discharge in the line current. If the coefficient is close to 1, the DC fault is assumed to have happened. As for STFT method, it is found that window length of 32 samples is optimum for fast and accurate fault detection, undermining the influence of noise. The frequency spectrum of line current is distorted in the event of DC fault, with magnitude of first zero-crossing frequency bin showing increase in value.

Their performances are validated and benchmarked against wavelet transform (WT) using the fault signals obtained from a laboratory-scale DC system experimental hardware and a multi-terminal DC system built in PSCAD/EMTDC. In term of speed, the CD method provides the fastest detection, followed by STFT, and lastly WT. The CD method stands out to be the most resilient to the influences of fault resistance and location, whereas the WT method is significantly affected. It is demonstrated that all methods evaluated are able to identify the faulted line in the ring and radial multi-terminal DC system without relying on inter-terminal communication. Sampling frequency can be an issue for the WT method as far as the sensitivity and detection time are concerned. Lastly, STFT method is more computationally efficient than the WT and CD methods. Comparison with *di/dt* method also shows that the proposals perform better under the influence of fault parameter.

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