Short-Circuit Fault Management in DC Electric Ship Propulsion System: Protection Requirements, Review of Existing Technologies and Future Research Trends

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***Abstract*—Ease of integration of the variable speed diesel generators resulting in substantial reduction of the fuel consumption is the key motivation for the development of the dc shipboard power system (SPS). One of the impediments to the widespread adoption of the dc SPS, however, has been the lack of comprehensive fault management strategies during the short-circuit faults. Such strategies comprise of fault detection, fault isolation, and reconfiguration of dc SPS. In the existing literature, all these aspects of fault management are dealt independently and mostly assuming ideal conditions. All the strategies are of utmost importance and it is needed to study them under a common framework which is the aim of this paper. This paper starts with a brief discussion on the characteristics of dc SPS along with recent modeling techniques. Subsequently, the paper describes the short-circuit fault studies, fault characteristics and protection requirements. Finally, the paper outlines the working principle, advantages and limitations of the fault detection, isolation and reconfiguration strategies developed for the dc power system and analyses their suitability to the dc SPS. The paper is concluded by identifying the future research trends needed for the development of the short-circuit fault management strategies of dc SPS for critical marine missions.**

***Index Terms*—DC Fault Detection, DC Fault Isolation, DC Fault Studies, DC Protection, DC Shipboard Power System, Fault Tolerant Converters, Platform Supply Vessel, Ship Reconfiguration.**

I. Introduction

Marine vessels integrated with the electrical propulsion have conventionally been based on fixed voltage, fixed frequency (50/60 Hz) ac generation and distribution system [1]–[4]. In recent years, a variety of alternative power generation and distribution arrangements have been introduced. Of these, the dc based shipboard power systems (SPSs) have become of particular interest as they are able to integrate the prime movers operating at optimal speed resulting in reduced fuel consumption and increased fuel efficiency [5]–[7]. The dc SPSs might play a pivotal role in ensuring continuity of the electrical supply for vessels [8], which carry out critical marine missions such as offshore dynamic positioning [9]–[11], ice-breaking [12] etc. The dc distribution bus is powered by one or more ac/dc converters with the ac side being interfaced directly to the ac generator. The ac/dc converter may be either a current source converter (CSC) or voltage source converter (VSC). The common converter topology is the six-switch two level VSC (2L-VSC) with the dc-link voltage in the range of 1.5 kV to 3 kV [13].

One of the prime constraints encountered in the design of dc SPS is the lack of standards and guidance on the implementation of comprehensive short-circuit fault management within such systems. Short-circuit fault management of dc SPS essentially includes fault detection, fault isolation, and post-fault reconfiguration. Fault detection and isolation are required to segregate the faulty part from the healthy section of the dc SPS. The reconfiguration of the dc SPS is required to modify the system architecture to ensure that the power flow to the critical loads is not unnecessarily interrupted. The challenges of fault detection and fault isolation in the dc ships are comparable to those encountered in land-based dc power systems and dc micro grids. There are however significant differences in the load profiles of these systems [14], [15]. The reconfiguration of dc SPS is very much influenced by the criticality of marine propulsion loads and in this respect is different from the land-based dc power systems. Unlike dc microgrids and the high voltage dc (HVDC) transmission systems which have reasonably predictable load profiles, the dc SPS is equipped with widely varying propulsion loads that may represent some 80% of the generation capacity.

The challenges encountered in the development of dc SPS have been taken up by various academic and industrial research foundations. One of the prominent research groups is Electric Ship Research and Development Consortium (ESRDC) which is based in the USA and comprises of several university labs

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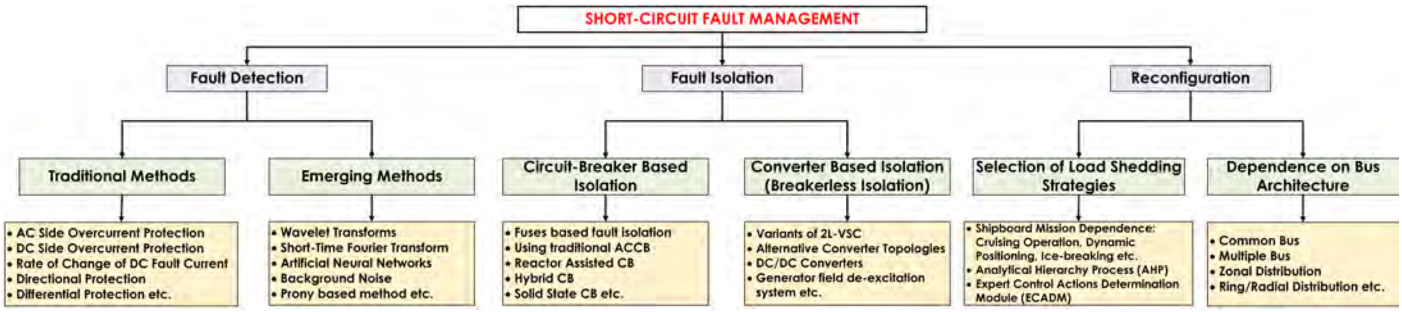


Fig. 1. Overview of Fault management of dc SPS.

dedicated to the development of dc ships [16]. Many industrial establishments, such as ABB and Rolls-Royce, have started investing their resources for developing the technologies required for future dc ships. One significant milestone in this area has been the deployment of the battery operated passenger liner *MF Ampere* [17]. This innovative vessel was commissioned in 2014 and has been operating in Norway. In spite of such advancements, the adaptation of the dc SPS for longer voyages including the critical marine missions can only be realized after devising comprehensive fault management system.

The overview of the fault management of dc SPS is shown in Fig. 1. Short-circuit in dc SPS is characterized by rapid increase in current and decrease in voltage. This huge surge in the fault current is caused by the discharge of the dc-link capacitor, which poses challenges to devise suitable fault detection algorithms. Since the rise time of the fault current is very low, the fault detection algorithms must be able to detect the fault in very short period of time. Moreover, this stringent time constraint results in poor coordination between the primary and the secondary (back-up) protection algorithms [18]. Apart from the challenges in fault detection; fault isolation remains other biggest hurdle. The faulty section must be isolated which can be realized by using circuit breaker (CB) or having breakerless (fault tolerant) architecture. Due to lack of current zero crossing, the ac circuit breakers (ACCBs) cannot be suitably used. The emerging DCCBs and the hybrid CBs [19] are proposed in the literature which however are limited by the size and cost. During the fault, freewheeling diodes of the 2L-VSC experience huge short-circuit current which is sufficient to damage them. The ability of the diode to withstand the fault current is specified by the adiabatic heating that occurs in the diode during the fault currents and is specified by the I^2t-value [20]. The reconfiguration of the dc SPS comes after the fault is detected and isolated. Reconfiguration can be realized by analyzing the load shedding strategies and adopting the bus architecture of highest reliability.

Hence, it can be observed that the fault management of dc SPS is not a straightforward problem which can be addressed in a single attempt. Researchers are working independently in fault detection, isolation, and reconfiguration of dc SPS. This paper aims at integrating all these approaches to understand the future needs with a brief introduction of dc SPS. The paper is divided into seven sections. Section II covers a detailed background information of the dc SPS. It comprises of the evolution of the dc SPS, its advantages over its ac counterpart, the available standards, grounding condition requirements along with modeling of the representative dc SPS. Section III describes the protection challenges and the practical issues and requirements for short-circuit fault management in dc SPS. The short-circuit fault studies and the response of the converters to the external fault condition is also covered in this section. A review of fault management of dc SPS, i.e., fault detection, fault isolation and reconfiguration are covered in Sections IV, V and VI respectively. The conclusions and future research needs are covered in Section VII.

II. Background Information of DC SPS

A. *Evolution of DC SPS*

The evolution of the electrical shipboard system can be traced back to the 1880s. According to the records, *SS Columbia,* was the first commercial ship with onboard dc system [3]. With the advent of more rugged induction machines and the diesel engines, the topology and operation of SPS changed accordingly. *Vandal* was the first diesel electric powered vessel developed in 1903 and *USS Jupiter* was first naval ship developed in 1912. Although ac was developed in early 19th century, *SS Canberra* was the first passenger vessel to use ac propulsion systems in 1960 [3]. With the development of power electronic devices in the subsequent years [21], the research, and development to achieve all-electric ship increased substantially. The aim of the all-electric ship is to achieve increased fuel efficiency, better manoeuvrability, and emission control. *Queen Elizabeth* was developed as the first ship powered with diesel-electric integrated propulsion, inaugurated in 1987 [3]. The development of advanced thruster systems such as azimuth and bow thrusters resulted in better manoeuvring capability of the offshore vessels [22].

B. *Advantages of DC SPS*

One of the major push towards the dc SPS is the development of power electronic interfaces for integration of the variable speed drives. There are certain advantages of dc SPS over its ac counterparts which are described below:

1) *Fuel economy:* Unlike ac system, the variable speed diesel generators can be conveniently integrated with the dc SPS. The variation of the speed of the diesel engine in accordance to the load demand limits the consumption of the fuel, hence increasing the fuel efficiency. This operation is explained further in Section II-F.
2) *Regeneration:* As compared with the ac drives with diode front ends, the regenerative energy in dc power systems can be absorbed to other loads connected to the same dc-link.
3) *Distribution loss and power factor:* As compared to the ac systems, the absence of power factor and skin effect in the dc distribution results in reduction of cable size.
4) *Space and weight reduction:* DC SPS may be more compact than the ac SPS because of less number of transformers used. The reduced cable sizing in dc SPS also adds to weight reduction.
5) *Integration with energy storage system:* Various emerging energy storage systems [6], [7], [23] may be conveniently interfaced with the dc-bus using bi-directional dc-dc converters.
6) *Quick synchronization:* Critical phase and frequency synchronization are not required in dc SPS. Thus, in the event of "loss of generator", a reserve generator may be quickly brought on line and connected to the dc bus.

C. Comparison with the Land-Based DC Microgrids

The dc SPS can be compared with the land-based dc microgrids. Both are isolated finite inertia power systems having a high penetration of power electronic interfaces. Depending on the application areas, the land-based microgrids can have different distribution topologies; the common topologies being the radial system and ring-bus. Similarly, the dc SPS can have different topologies depending on the operational requirements. The dc ships operating as passenger ferries can have simple topologies employing generating sources and loads connected to a dc bus [17]. Zonal type distribution system [24] is required in the warships because of the stringent reliability and survivability requirements as compared with the passenger ferries.

In the event of generation failure, the land-based microgrid can be connected to the stable utility grid. The SPS can only be connected through a 'ship-to-shore' interface [25] when it is in the dock. The dc SPSs are designed to be more reliable than the land-based dc systems for increased safety of the passengers and crews. The land-based dc microgrid is subjected to the integration of a large number of renewable energy sources, whereas due to space limitations the dc SPS is envisaged to be operating mainly with variable speed diesel or gas turbines. The loads in land-based systems are conventional, continuous and generally predictable based on the past events and data. On the contrary, loads in dc SPS can be unpredictable. The propulsion loads in the SPS depends on the operating modes, weather conditions, etc., making it in general unpredictable. Further the presence of pulsed type transient loads [26] in the emerging warships aggravates the prediction of marine loading conditions. In the event of generator loss, load shedding is required in both the land-based and SPSs to prevent inadvertent black-out conditions. However, the load shedding algorithm in each case is somewhat different. Load prioritization and load shedding negotiation are generally done in advance in case of land-based power systems [14]. The load prioritization in the SPS is dependent on the operating modes of the ships [15]. One of the other major difference between the land-based power system and SPS is the grounding requirements. Generally, solid grounding is used in the land-based microgrids for early detection of the earth fault, whereas in the SPS the high resistance grounding is preferred [13], [27] as the marine vessels are expected to run with single earth fault. The characteristics associated with of different grounding schemes are listed in Table I [28].

TABLE I
CHARACTERISTIC ASSOCIATED WITH DIFFERENT KINDS OF GROUNDING

Characteristic	**Solid**	**Ungrounded**	**High Resistance**
High ground fault current	Yes	No	No
Arc flash hazard risk level	High	Very Low	Very Low
Continuity of service	No	Yes	Yes
Approx. transient over-voltage	2.5	>6	2.7
Cable insulation requirement	1	1.73	1.73

D. Standards Associated with DC SPS

Although the dc ship is still in the research and development phase, few standards are available which should be referred to while designing and analyzing the dc SPS. The IEEE Standard 1709-2010 [13] deals with the design steps indicating the technical problem assessment. The IEEE Std 1662-2008 [29] covers the guidelines and specifications of the power converters which are to be utilized in the dc SPS. If zonal distribution system is used in the system, then IEEE Std 1826-2012 [30] and MIL STD-1399 [31] section 300 and section 680 should be referred to. IEC/ISO/IEEE Std 80005-1 [25], [32] deals with the high voltage shore connections when the ship is at the dockyard.

E. Voltage Level of DC SPS

The system voltage of the target dc SPS should be based on the desired generator voltage, propulsion motor drive voltage, converter design, load requirements, cable & bus-bar rating and the fault energy [13]. According to the IEEE Std 1709-2010 [13], the various medium voltage dc (MVDC) voltage levels are listed in Table II.

F. Representative DC SPS: Platform Supply Vessel

To understand the structure of a typical dc SPS, platform supply vessel is considered in this paper [6]. Fig. 2 represents a dc SPS operating as a platform supply vessel which is expected to execute complex marine missions such as dynamic

TABLE II
VOLTAGE LEVEL OF DC SPS

	MVDC Class kV	Nominal MVDC Rated Voltage (kV)
Established Classes	1.5	1.5 or ±0.75
	3	3 or ±1.5
Future Design Classes	6	6 or ±3
	12	12 or ±6
	18	18 or ±9
	24	24 or ±12
	30	30 or ±15

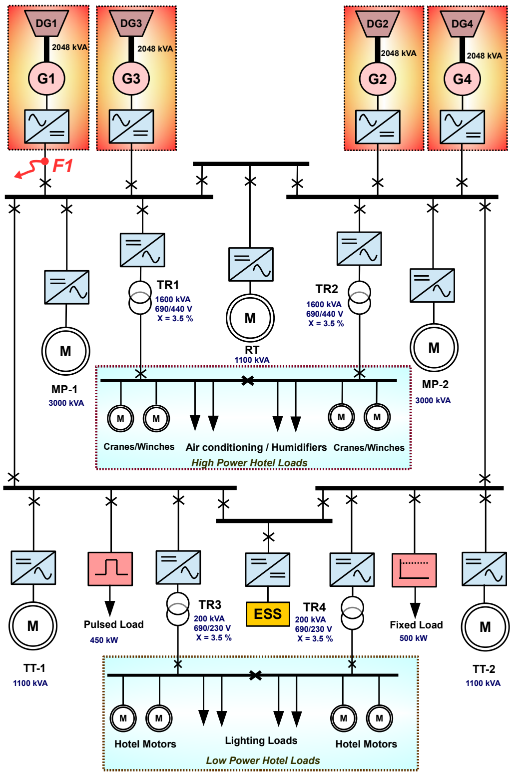


Fig. 2. Schematic of the representative dc platform supply vessel [6].

positioning and cruising operation. The generation system comprises of synchronous generators driven by a diesel engine [6], [33] which could be operated in variable speed. The loads of the dc platform supply vessel comprises of main propulsion (MP) to perform the cruising operation and tunnel thrusters (TT) and retractable thrusters (RT) to accomplish the dynamic positioning operation. The high and low power hotel loads are also modeled, which comprise of the fixed frequency ac loads such as cranes/winches, air conditioning systems, lighting loads, small motors, etc.

The motivation to adopt the dc marine vessel is to operate the interfaced DG in variable speed to minimise the specific fuel oil consumption (SFOC). The operating regions of the DG running with fixed and variable speed are marked in Fig. 3(a) [5], [6]. Fig. 3(b) and (c) shows the trajectory of the operating points of the SFOC of the DG when there is a sudden decrease in dynamic positioning and cruising loads. For comparison, the SFOC of the DG when running at fixed speed is also shown in Fig. 3(b), and (c). From both operations, it could be inferred that the fuel consumption is minimal when operating at optimised variable speed [6]. This is possible as the speed is decreased with the change in power (torque demand), thus enabling the DG to consume lower fuel.

III. FAULTS IN DC SPS

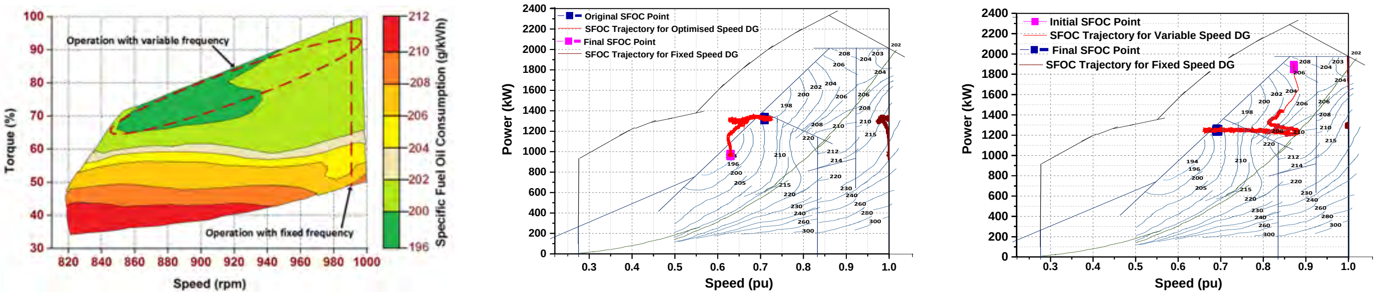
A. Short-Circuit Protection Challenges of the DC SPS

The compact dc SPS is contemplated to be sharply impacted by the short-circuit faults. Thus, in spite of the significant advantages offered by the dc SPS, lack of comprehensive fault management techniques to mitigate the short-circuit faults are the major set-backs to adopt it for the critical marine missions. The prime challenges while designing the fault management system are:

1) *Severe transient discharge:* In the dc SPS, the current is limited by a very low ohmic resistance. During the short-circuit, the entire grid is affected by almost same intensity of fault current [34] which challenges the selective operation of the fault detection algorithm thus resulting in limited fault localization.
2) *Lack of current zero crossing:* The arc extinguishing becomes a difficult task due to the lack of zero current crossing in the dc system. As a result, the traditional AC-CBs cannot be used and new fault isolation techniques must be developed.
3) *Dependence on converter topology:* The short-circuit current is dependent on the chosen converter topology [34]. For current controlled thyristor bridge topology, the current can be reduced to zero, preventing the generator from feeding into the fault location [35]. In case of IGBT-based VSC, the generator continues to feed the fault through the freewheeling diodes till its own ac protection is activated [36], [37].
4) *Effect of output filter:* The output filter connected with the converter (*'C-filter' for VSC* and *'L-filter' for CSC*) stores a considerable amount of energy during the fault which needs to be dissipated [34].
5) *System grounding:* The grounding considerations in the dc SPS is comparable with the ac system but the location of the grounding is different. Since the dc ship is expected to survive single earth faults, high resistance dc-link mid-point grounding is conceived to be utilized [13].

B. Short-Circuit in DC SPS

The generation system of dc SPS would comprise of synchronous generators interfaced with the 2L-VSC as shown in Fig. 2. Thus, the short-circuit fault current on the dc SPS will be characterized by two responses: one is the transient discharge current from the dc-link capacitors of the interfaced converters, and the other one is steady-state discharge current



(a) (b) (c)

Fig. 3. (a) Regions of the SFOC of the diesel engine with variation of engine speed and engine torque. Variation in SFOC of the DG during (b) dynamic positioning and (c) cruising operation [6].

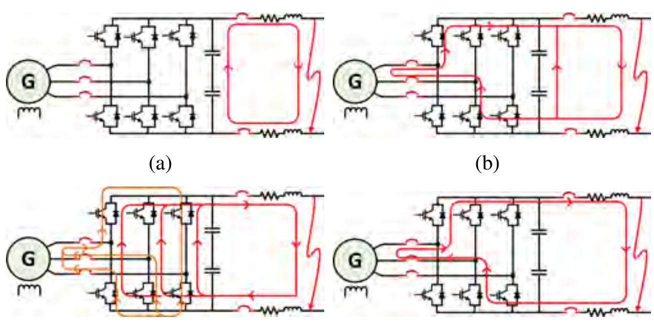
from the generating sources and motors [38]. This high capacitive discharge current alone may cause thermal damage to the components in the fault path (especially the dc-link capacitor itself), mechanical damage caused by magnetic forces exerted on conductors and overvoltage damage. A low impedance fault in the dc SPS is identified as the most severe single point fault. The response of the 2L-VSC in dc generation system to the external fault condition is typically a 4-stage process, as shown in Fig. 4 and explained below.

Stage 1: The dc-link capacitor discharges almost instantaneously during the fault hence reducing the dc-link voltage.

Stage 2: The ac generator starts feeding the fault current after the dc-link voltage dips below the line-to-line voltage and the freewheeling diode is forward biased. The IGBT could be turned-off due to the overcurrent protection.

Stage 3: All the freewheeling diodes are conducting and the generator is essentially in short-circuit condition.

Stage 4: Steady-state fault current flows from the ac generator to the line resistance, leakage inductance and the stray capacitance.



(a) (b) (c) (d)

Fig. 4. Different stages of fault current, (a) Stage 1, (b) Stage 2, (c) Stage 3 and (d) Stage 4.

C. DC Short-Circuit Fault Current Calculation

Short-circuit fault studies and fault current calculation are essential for understanding the aftermath of the fault and accordingly devise the necessary protection algorithms. The nature of the fault current would be useful in selecting the type of fault detection and isolation techniques. To illustrate the fault current calculation for the dc SPS, a preliminary analytical evaluation has been done with the system comprising of one generator interfaced converter connected with an inverter fed propulsion load as shown in Fig. 5(a). The fault current comprises of the dc-link capacitor discharge followed by fault current supplied by the ac source as depicted in Fig. 5(b). This is in accordance with the various stages of fault current as described in Section III-B.

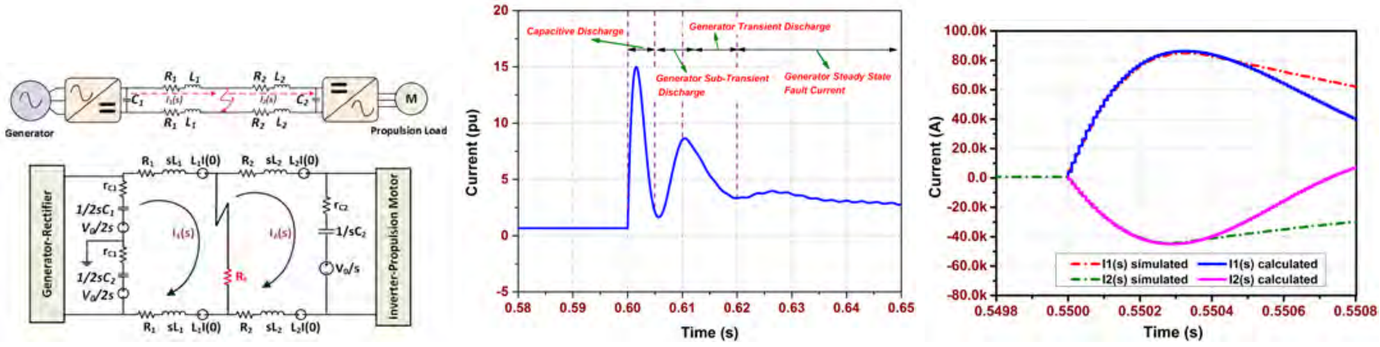
As the dc-link capacitor is the first element to discharge into the fault point, it becomes the prime identification of the fault occurrence in the dc SPS. It is thus important to analyze the dc-link discharge to understand the fault detection requirements. Referring to Fig. 5(a), the Laplace transform of the bolted short-circuit fault current $I_1(s)$ and $I_2(s)$ resulting from capacitive discharge of the generation system and propulsion load can be expressed as:

$$I_1(s) = \frac{\dfrac{V(0+)}{2L_1} + I(0+)}{s^2 + s\dfrac{R_1 + r_{c1}}{L_1} + \dfrac{1}{2L_1C_1}}, \tag{1}$$

$$I_2(s) = \frac{\dfrac{-V(0+)}{2L_2} + I(0+)}{s^2 + s\dfrac{2R_2 + r_{c2}}{2L_2} + \dfrac{1}{2L_2C_2}}. \tag{2}$$

The nature of the fault current from the dc-link can be underdamped or over-damped depending on the fault resistance, fault location and circuit configurations. Table III illustrates the analytical expression for the fault currents during bolted short-circuit as a result of capacitive discharge from generation system ($i_1(t)$) and propulsion loads ($i_2(t)$).

The steady state fault current discharge from the ac side generally has slow rising slope as compared to the capacitive discharge owing to the reactances of the interfaced generator. The analysis of the fault currents resulting from ac side is available in the literature [36], [37], [39]. The ac side fault current is able to damage the freewheeling diodes of the 2L-VSC once its thermal capability is exceeded.



(a) (b) (c)

Fig. 5. (a) DC SPS comprising of one generation and one load unit with its equivalent circuit during capacitive discharge, (b) typical short-circuit current and (c) comparision of simulated and calculated values of $I_1(s)$ and $I_2(s)$ during bolted short-circuit fault.

TABLE III
FAULT CURRENT CALCULATION

Current	Damping Conditions	Current Expression	Parameters
$i_1(t)$	Overdamped : $(\frac{R_1+r_{c1}}{L_1})^2 > \frac{2}{L_1C_1}$	$\frac{e^{-\alpha_1 t}}{2\beta_1}\left[\frac{V(0)}{L_1}(e^{\beta_1 t}-e^{-\beta_1 t})+\beta_1 I(0)(e^{\beta_1 t}+e^{-\beta_1 t})\right]$	$\alpha_1 = \frac{R_1+r_{c1}}{2L_1}$, $\beta_1 = \sqrt{(\frac{R_1+r_{c1}}{2L_1})^2-\frac{1}{2L_1C_1}}$
	Underdamped : $(\frac{R_1+r_{c1}}{L_1})^2 < \frac{2}{L_1C_1}$	$e^{-\alpha_1 t}\left[\frac{V(0)}{\omega_{d1}L_1}sin(\omega_{d1}t)+I(0)cos(\omega_{d1}t)\right]$	$\omega_{d1} = \sqrt{\frac{1}{2L_1C_1}-(\frac{R_1+r_{c1}}{2L_1})^2}$
$i_2(t)$	Overdamped : $(\frac{2R_2+r_{c2}}{2L_2})^2 > \frac{2}{L_2C_2}$	$\frac{e^{-\alpha_2 t}}{2\beta_2}\left[-\frac{V(0)}{L_2}(e^{\beta_2 t}-e^{-\beta_2 t})+\beta_2 I(0)(e^{\beta_2 t}+e^{-\beta_2 t})\right]$	$\alpha_2 = \frac{2R_2+r_{c2}}{4L_2}$, $\beta_2 = \sqrt{(\frac{2R_2+r_{c2}}{4L_2})^2-\frac{1}{2L_2C_2}}$
	Underdamped : $(\frac{2R_2+r_{c2}}{2L_2})^2 < \frac{2}{L_2C_2}$	$e^{-\alpha_1 t}\left[-\frac{V(0)}{\omega_{d2}L_2}sin(\omega_{d2}t)+I(0)cos(\omega_{d2}t)\right]$	$\omega_{d2} = \sqrt{\frac{1}{2L_2C_2}-(\frac{2R_2+r_{c2}}{4L_2})^2}$

These events demands stringent timing requirements for dc fault detection and isolation which are discussed elaborately in Section III-D.

D. Practical Issues & Requirements for Protection of DC SPS

1) Current sensor requirements: Current sensor is one of the vital element for the successful operation of the fault detection algorithm of the power system and converter controls [40]–[42]. An ideal current sensor should be able to measure and track the fault current accurately. In traditional ac power systems, current transformer is used for measurement of currents during steady-state and transient conditions. Such current transformers have limited bandwidth which ranges till few kHz. Exceeding these limits results in non-linear operation with potential resonance problems [43], [44]. Further, the current transformer is prone to saturation while measuring high fault currents. Apart from traditional current transformer, there are a variety of current sensors available for the measurement of fault currents such as shunt resistors, hall-effect sensors, and Rogowski coils. The comparison of the various current sensors are depicted in Table IV.

Of all these available current sensor, Rogowski coil can measure the fast changing high frequency ac and pulsed loads. Moreover, its lower cost, negligible dc offset and saturation problem along with its linear operation, low power consumption and capability to measure high current, makes them suitable for the fault detection application in the dc SPS where the dc fault current is expected to rise almost instantaneously due to discharge of dc-link capacitor. One of the major disadvantages of implementing Rogowski coil is the requirement of integrator to translate the voltage induced across the coil into equivalent current value. The integrator requires additional power supply and its choice is dependent on the target application and required frequency bandwidth. Moreover, the Rogowski coil is useful in determining the change of dc current, which makes it ineffective for monitoring currents during the steady-state condition. The saturation problem of Rogowski coil is primarily mitigated by constructing the coil over air-core thus having relative permeability $\mu_r \approx 1$. The sensitivity of the output thus depends on the construction of the Rogowski coil (number od turns, geometry of the coil etc.) along with the chosen integrator. Thus a detailed study on the construction of Rogowski coil with accurate modeling is required to address these hindrances and before deploying it for the dc fault detection application.

2) Timing and fault isolation requirements: The dc fault current rises rapidly as the system impedance is low as compared to the ac system. In the ac systems, steady state fault currents are used for relay settings and calculation of the protection devices. However, in the dc system the steady-state fault currents can damage the interfaced converters [45]. It is thus required that the fault detection and isolation must be

TABLE IV
COMPARISON OF DIFFERENT CURRENT SENSORS

Current Sensing Technology	Low Resistance Current Shunt	Current Transformer	Hall Effect Sensor	Rogowski Coil
Cost	Very Low	Medium	High	Low
Linearity over measurement range	Very Good	Fair	Poor	Very Good
High Current measuring capability	Very Poor	Good	Good	Very Good
Power Consumption	High	Low	Medium	Low
Current saturation problem	No	Yes	Yes	No
Output Variation with Temperature	Medium	Low	High	Very Low
DC Offset problem	Yes	No	Yes	No
Saturation and Hysteresis Problem	No	Yes	Yes	No

completed within < 10 ms.

In the traditional ac systems, circuit-breakers (CBs) are employed to isolate the faulty section. In such systems, the current and voltage waveforms have zero crossing which helps in extinguishing the arc while breaking the fault current. AC-CBs have dedicated arc chutes which help in arc extinguishing and energy dissipation during breaking the fault current. The time required for this operation depends on the type of CB employed in the system. The selection of arc quenching media is dependent on the power and voltage level. For higher power applications, vacuum and SF_6 based CBs are typically employed. The complete fault detection and isolation in a 50-Hz ac system usually takes around 80 ms.

Due to absence of natural current/voltage zero in dc systems, additional arrangements need to be done for arc extinguishing and subsequent fault current isolation. If CB-based fault isolation is employed, then additional resonance techniques can be used, which induce zero-crossing in the dc current. Further, an additional energy absorption circuit is needed to drive the dc current to zero whose rating depends on the speed of operation, rating of CB and inductance present in the system [46]. Apart from the CB-based fault isolation, breaker-less approach could be employed, which utilizes the interfaced converters as fault isolating devices. The detailed discussion of the various fault isolating techniques are covered in Section V.

3) Selectivity requirements and challenges in relay co-ordination: In addition to the fault detection; fault isolation would be carried out by selective operation and co-ordination among the protective relays. In the existing ac systems, non-unit and unit-based protections are instrumental in achieving such selective operation and relay co-ordination. Non-unit protection is carried out by measurement of the current or voltage at the local end, while the unit protection is executed by processing the current and voltage signals at both ends of the circuit. For multi-terminal systems, current and voltage signals of all ends are processed [47]. Non-unit protection in the ac system is executed by the current or time grading operation where the selective operation is ensured by intentional time delays (in the order of hundreds of milliseconds) in the relays. For the dc SPS, such gradings cannot be implemented due to fast-rising fault currents and stringent timing requirements [18]. Distance protection based non-unit protection is also popular for long distance ac transmission lines which seems not to be applicable for the compact dc SPS.

The unit protection based selective operation could be carried out by differential or zone based directional relaying operations. If such unit protection was implemented, dc SPS would require transmission of time-stamped current/voltage signals over a high-bandwidth communication channel. On the contrary, the non-unit protection requires the exchange of logical signals which is enabled by the low-bandwidth communication infrastructure. In addition to the coordination between the protective relays, coordination with the interfaced converters is also preferred which would ease up the selective operation.

4) Communication and automation infrastructure: It is pertinent to install the communication and automation architecture to supplement the fault management strategies in the dc SPS. In the ac substations, data acquisition and transfer is carried out by adhering to the IEC 61850 standard. Data transfer is carried out between the merging units and the intelligent electronic devices (IEDs), while the tripping signals are transmitted by generic object oriented substation event (GOOSE) messages. The GOOSE messages in ac systems take, 3 ms which is certainly not acceptable in dc networks where such delay should be limited to 1 ms. There have been significant advantages in the communication infrastructure of the ac substations by adopting the optical fibre communication hence reducing the propagation delay. This delay is further dependent on the packet size and bandwidth of the communication channel [46], [48].

5) Standardization and interoperability requirements: The requirements for the short-circuit fault management in dc ships are quite different from the ac counterpart. Unlike ac power systems, the dc SPS along with HVDC and dc microgrids are custom made mostly by a single manufacturer/vendor. On the contrary, multi-vendor system fosters innovation and enhances competitiveness which can be seen in the ac power systems where a variety of fault detection, isolation devices are available from different manufacturers. Although, there are standards for the development of dc SPS from the power electronics perspective (see Section II-D); there have been lack of codes, fault detection & isolation guidelines and communication protocols. These gaps in the interoperability requirements if addressed would attract multiple vendors to venture in the area of dc fault management.

Such standardization would be possible with enhanced cooperation and successful implementation of the working groups. Cigré has been the front runner in the HVDC protection. Cigré B4-56 [49], Cigré B4/B5-59 and Cigré JWG A3-B4.34 are the working groups studying on the grid codes for muti-terminal HVDC system, control and protection of HVDC grid and requirements for switching devices respectively. Apart from Cigré, CENELEC TC8x WG6 has also been instrumental for working on dc grids. Communication protocols for the dc systems are expected to be modified version of the IEC 61869, IEC 60255, IEC 61850 and IEC 60834, which are widely implemented in ac systems. These advancements could facilitate the multi-vendor based dc grid protection solution.

IV. Fault Detection and Localisation in DC SPS

Short-circuit fault detection and localisation in dc SPS is expected to be the modified version of that of land-based dc grid system. Due to compact nature of the dc SPS, the short-circuit faults may severely impact the SPS operation. Hence extra precaution must be taken while designing the protection design for dc SPS. Researchers have been trying to devise suitable algorithms for quick fault detection and localisation in the land-based dc power system. Failure mode and effect analysis (FMEA) [50] & fault analysis has been carried out for low voltage dc (LVDC) [38], [51], [52], medium voltage dc power systems (MVDC) [53] and HVDC [36], [37], [54]–[56]. This section briefly reviews a few notable advancements in the field of dc fault detection and localization methods developed for land-based power system and explores whether these methods would be suitable for the dc SPS.

A. Traditional Fault Isolation and Localisation Methods

1) Protection from the ac side: There are several fault detection algorithms available in the literature for the dc power systems. The simplest of all is the protection from the ac side [35], in which the circuit breaker isolates the ac generation system from feeding into the fault location. This method works well as the ac side protection is matured enough, but the main drawback is the time of operation. The ACCB takes 1-2 cycles to isolate the faulty section, which is excessively long for dc SPS. The handshaking technique can further be utilised for the fault localisation in ring type bus architecture using the direction of the flow of current. This operation results in power outage till the faulty section is isolated, thus making it inept for the vessels undergoing critical marine missions and requiring reliable and continuous power supply.

2) Protection based on dc side overcurrent and rate of change of dc current: Overcurrent (OC) fault detection and relay coordination have been popular choices for ac power systems [57]. Due to the compact nature of dc SPS, OCs cannot be preferably used because of similar fault current magnitudes across all the sections of dc ship. As a result, OC based primary protection is more suitable for point-to-point dc system and as a backup protection in multi-terminal dc systems [58]. Instead of OC, rate of change of dc current or di/dt has been very popular for fault detection in dc grids [59], [60]. The fault is identified by setting limits on the di/dt value which has also been experimentally verified [61], [62]. In multi-terminal dc systems, the fault selectivity is further supported by the addition of inductances which alters the di/dt profiles across the dc grid [63], [64]. This di/dt of the current can also be useful for determining the fault location as well. With the help of measured di/dt and the measured terminal voltage, the value of inductance of the protected section [62], [65] can be estimated. For the faulted condition, the estimated inductance differs from the original value thus localising the fault point. However, the prime drawback of this method is the requirement of high bandwidth sensor as it measures high di/dt and faster calculation with accurate determination of pre-fault line inductance. The effectiveness of the di/dt based fault localisation in meshed dc SPS is questionable and thus would be an interesting study to make.

3) Differential and directional based protection: Fault detection and localisation is generally possible with the differential and directional based unit-protection schemes. The directional protection where the change in current direction indicates the fault condition is most likely to be adopted from the experience in ac power systems [57], [66]. The requirement of this type of protection is to have suitable DCCB to isolate the faulty section [67]. The differential protection used in the ac system can also be applied to the dc system. The basic method remains same in which the current entering the node equals the current leaving the node [57]. Since the rate of rise of fault current is too high, implementation of differential protection requires extremely fast and high fidelity current sensors [41] and communication requirements [18], [68], [69].

B. Emerging Fault Isolation and Localisation Methods

1) Signal processing based methods: Signal processing tools such as wavelet transform [61], [70]–[72] and short-time fourier transform [45], [73], [74] based fault detection algorithms have also been applied to dc power systems. Along with the wavelet transform, high precision fault classification method using artificial neural networks (ANNs) have been proposed by researchers [72]. Although these methods provide sufficiently accurate results these are not devoid of challenges. The selection of suitable wavelets and training of the ANN algorithm sometimes might be difficult. Moreover, these methods introduce significant computational burden. Data mining [75] approach is also used by the researchers to determine the threshold values of the relays which are useful for relay coordination. This is applied in multiple distributed generation systems. The suitability of such signal processing techniques while mitigating the practical challenges (Section III-D) and considering the operating profile of dc SPS would be an interesting area to venture in.

2) Protection based on converter operation: The converter based fault detection has also been suggested by researchers. The capacitor dc circuit breaker (CDCCB) have been proposed, which limits the capacitive discharge current during the fault [76]. The freewheeling diodes of the IGBT based VSC might be replaced with suitable turn-off devices (such as thyristors) which can limit the fault current from ac side [76], [77]. Although the method seems viable if implemented, it would result in bulkier converter design. The solid state defender has been proposed which is designed to operate during the bus faults, load fault and power system transients [78]. Moreover, the solid state defender can also act as an impedance transformer to cope up with the negative impedance instability. However, the requirement of high input capacitor is the major drawback of this method. Moreover, the equivalent series resistance of the capacitor might affect the operation.

3) Other miscellaneous techniques: Apart from the above-mentioned methods, some other interesting methods have been proposed for dc fault detection and localisation. The travelling wave based fault detection technique which measures the time difference between incident and reflected wave is widely used in the HVDC systems [79], [80]. Similarly, electromagnetic time reversal (EMTR) techniques have been proposed for the fault localisation of HVDC systems [81]. Both methods might not be suitable for dc SPS for its compact size as compared to the HVDC system. Other interesting fault detection techniques include prony based fault detection algorithm [82], and algorithm based on background noise of the converter [83]. Although the methods provide better results, they are still in the development phase and need substantial investigation. The transient impedance based methods are also proposed for the protection of dc power system [84], while the active impedance based methods have been popular for determining the fault location in the zonal distribution systems [85].

Several signal injection based offline methods have also been proposed for the fault location where an external signal is injected and from the return response the fault location is identified [86], [87]. Communication assisted centralised protection has also been proposed where the entire dc microgrid is divided into sub-microgrids. The fault localisation is performed by isolating these entire sub-microgrid once the relay detect the fault. This method needs high-bandwidth communication networks and it has the drawback of power outage during the process [88]. The fault localisation based on the steady state fault current and voltage consisting of sixth harmonic components are also suggested [89].

The existing fault detection methodologies along with suitable references have been indicated in Table V. From the above discussion, it can be inferred that fault detection technique helps in locating the fault. However, fault isolating techniques are required for quick fault isolation, which is described in the subsequent sections.

V. Fault Isolation of DC SPS

After fault detection and localization, fault isolation is an important aspect of the dc fault management strategy [95], [96]. The dc fault isolation technique must be established, which can work in conjunction with the dc fault detection and localisation algorithms thus ensuring selective tripping operation. Tripping of the ACCB to isolate the dc fault results in power outage for a significant amount of time. Thus, protection of dc SPS can be broadly classified into breaker-based and breaker-less protection. On the contrary, in ac systems, ACCB is widely used for fault isolation. ACCB uses the natural zero crossing in the current and voltage to extinguish the arc generated while breaking the ac fault current. In the breaker-based protection of dc SPS, dc circuit breakers (DCCBs) would be utilised to segregate the faulty section from the healthy section. Due to the absence of natural zero crossing in dc systems, additional arrangements need to be done while extinguishing the dc fault current. For such applications, dc circuit breakers (DCCBs) with passive/active resonating circuit [97], [98], solid-state circuit breakers (SSCBs) [99]–[101] or hybrid circuit breakers (HCB) [102]–[104] could be employed to extinguish the fault current. It should be ensured that the isolation of the faulty section would result in minimum power interruptions to as many loads as possible. In addition to these, dc/dc converters [105] and Z-source converters [106] could also be used to isolate the fault sections.

A. Fault Isolation using Circuit Breaker

1) Resonance type DCCB (modification of ACCB): Modification of the existing ACCB to break the dc fault current is enabled by addition of commutation and surge arrester units. Passive and active commutation can be employed to operate the ACCB as a DCCB. The passive commutation based DCCBs operates with limited performance and is able to extinguish low breaking current but taking longer time to operate [46]. The active resonance based DCCBs have relatively better performance and are able to break high values of fault current and are faster than the passive DCCBs. The schematic of the passive and active resonance based DCCB is shown in Fig. 6 [97].

In normal operating conditions, the dc current flows through the ‘main path’ as shown in Fig. 6. After fault identification, a tripping command is issued to the main-breaker of the main path and a switching arc is generated. Subsequently, a current oscillation is generated between the commutation circuit RLC_{res} and the switching arc. These events create artificially current zero crossings passing through the main-breaker thus helping to diminish the switching arc and breaking the fault current [46], [97], [107]–[109]. For the active resonance based DCCB (in Fig. 6(b)), additional operation of switch S_1 and S_2 are ensured. S_2 pre-charges the commutation capacitor and is normally closed during normal operation. During the tripping commands, S_2 is opened while S_1 is closed to activate the active resonance operation.

TABLE V
REVIEW OF FAULT DETECTION & LOCALISATION METHODS

Method	Operation	Limitation	Ref.
Protection from ac side*	1) During the faults, the ACCB trips. 2) The faulty section is isolated by no load isolating switches.	1) Time consuming as the ac circuit breaker takes 1-2 cycles to operate. 2) Power outage during isolation of faulty section.	[35]
Current Differential Protection*	1) Matured technology in ac systems. 2) Measures the current difference of the input and the output.	1) Stringent communication requirements. 2) High bandwidth sensor requirements.	[18], [68], [69]
Directional Protection*	1) Based on magnitude and direction of current/voltage. 2) Intelligent electronic devices (IEDs) used for monitoring, control and communication functions. 3) Solid state circuit breakers (SSCBs) used for fault isolation.	1) High bandwidth sensor requirements. 2) Low bandwidth communication requirement.	[67], [90], [91]
VSC as current limiter	1) Capacitive dc circuit breaker (CDCCB) proposed to limit the current discharge from the capacitor. 2) Anti-parallel freewheeling diodes replaced by turn-off devices.	1) The CDCCB should be of higher rating and should be fast. 2) Bulky converter set with complicated control.	[76]
Converter based Protection	1) Solid state defender developed to operate during bus fault, load fault and power transients. 2) Also operates as impedance transformer to avoid negative incremental instabilities.	1) Requirement of high input capacitance. 2) Equivalent series resistance of the capacitor poses problems during operation.	[78]
Protection using initial di/dt*	1) Uses rate of current discharge from dc-link capacitor to detect and estimate the fault location. 2) Simpler concept to implement.	1) High bandwidth, non-saturable sensor requirements. 2) Presence of high frequency noise in the capacitive discharge current.	[59]–[65]
Fault detection by master-slave control§	1) Slave controller monitors the current flow and master controller monitors the current difference in the slave controllers.	1) Assumes the passive type loads. 2) Stringent communication requirements between master and slave controller.	[86], [87]
Using Wavelet Transform and Artificial Neural Networks (ANN)	1) Wavelet transform for fault detection and ANN for fault classification. 2) Independent of fault duration and no requirement of injecting external signal.	1) Choice of wavelet function and decomposition level is important and crucial. 2) Consumption of large memory and increased computational time.	[72], [92]
Using Background Noise	1) Switching transients of the converters are used for fault location estimation.	1) Complicated control algorithms. 2) Might be difficult to localise fault for multiple paralle generation system.	[83]
Travelling wave based approach*	1) Measure small difference between incident and reflected wave arrivals. 2) Have high accuracy.	1) Might not be useful for compact dc SPS. 2) Dependent on the topology of the distribution system.	[79], [80], [93]
Prony based method	1) Faulty section identified and isolated by comparing the fault current direction. 2) Prony algorithms applied to extract the characteristic frequency.	1) Immature technology.	[82]
Co-ordination of Converters and Bus-Tie switches*	1) The converter setpoint is set to zero for fault current mitigation. 2) System is suitably reconfigured when the converter output is set to zero.	1) Power outage during the re-configuration might affect the marine loads and marine operation.	[35], [94]
Sixth-harmonic based method§	1) Simple concept and easier to implement. 2) Limited to VSC based dc distribution system.	1) Requires higher number of steady-state fault current data for better performance.	[89]

∗: Can do fault localisation as well. §: For fault localisation.

For the resonance operation based DCCB, it is deduced that the arc in the path of the main-breaker becomes unstable to make the current oscillating and hence induces the zero-crossing condition. This condition is achieved when du_{arc}/di_{arc} is negative and larger than the absolute value of the resonating resistor (R_{res}) in the commutating path [107]. Thus, for development of resonating based DCCB, detailed modeling and study of the arc need to be done. The surge arrester ensures that the voltage across the DCCB does not exceed the rated threshold.

With the mentioned advantages and limitations, resonant type DCCBs have been developed in laboratories with prototypes being tested under varying fault conditions. Active participation of working groups have been instrumental to understand and develop such switching devices [110]. Earliest development on testing resonating DCCB was performed using SF_6 in the main breaker [111]. The passive resonance based DCCB has been employed for fault isolation in point-to-point dc system with operating time of 20 ms and rated at 5.3 kA [46]. In laboratory premises, the passive DCCB has been prototyped and is able to break the fault in 10 ms [107]. On the other hand, commutation with the active resonance based DCCB is faster, which can be achieved in 5-8 ms and have breaking capacity of 10.5–16 kA [46].

2) Solid-state circuit breaker (SSCB): With the rapid development of semiconductor devices, solid-state switches could be employed for the fault current current isolation and is generally termed as solid-state circuit breaker (SSCB) [19]. In recent years the applicability of SSCBs for dc ships has

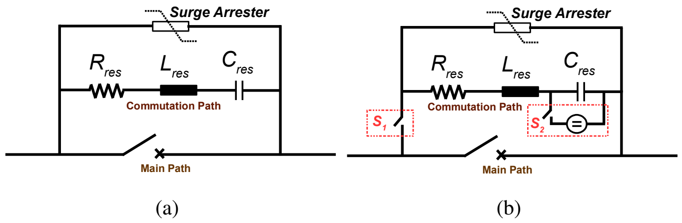


Fig. 6. Schematic of dc circuit breaker with (a) passive and (b) active damping [97].

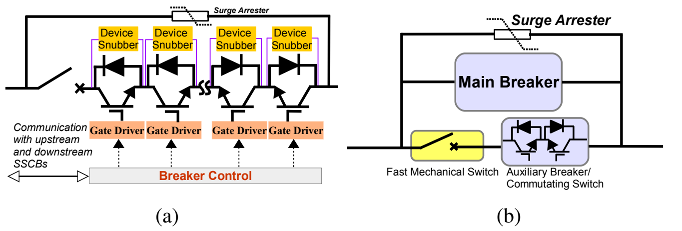


Fig. 7. Schematic of (a) solid-state circuit breaker (SSCB) and (b) hybrid circuit breaker (HCB).

been discussed [99], [100], [112]. These SSCBs are primarily conceived to be based on the operation of IGBTs and IGCTs [99]. Fig. 7(a) shows the SSCB capable of interrupting the fault current in both directions. This is enabled by the connection of two sets of semiconductor devices in anti-series configuration [112]. Additional mechanical disconnector is also present for galvanic isolation. The power and voltage level of the SSCB can be determined by the connected semiconductor switches. Apart from SSCBs, solid-state fault current limiter (SSFCL) has also been proposed [113] which breaks the fault current using the resonating LC tank circuit. SSFCL with self-triggered interruption capability with ability to handle a large amount of energy dissipation has also been proposed [114]. The operation of SSFCL is similar to fuses as they are one-shot devices, moreover, SSFCL is not suitable for higher voltage operation. The SCR based ACCB is developed, which can be used primarily for the ac systems and are not suitable for dc systems [95]. IGBT/IGCT based ACCB is able to detect the fault and turn-off in several micro-seconds and are capable to limit the fault energy [95]. However, the on-state losses of IGBTs are more than the SCR based ACCB.

3) Hybrid circuit breaker (HCB): Thus it can be seen that the resonance type DCCBs take longer time to isolate the fault whereas the SSCBs are fast enough and are expected to have smaller turn-off time. However, one of the disadvantages of SSCB is steady-state conduction losses of the semiconductor switches which will lower the efficiency of the system. Hence, a combination of both systems is needed and is termed as hybrid circuit breaker (HCB)[19], [115], [116]. The generic structure of the HCB is shown in Fig. 7(b) [102]. The main research has been focussed on the development of the *'main breaker'* with reference to Fig. 7(b). For example, the main breaker utilising SiC emitter turn-off thyristor [102], [103] and fast thyristors [104] has been developed for the application in MVDC ships and dc power systems, respectively. Apart from the experimental verification, detailed modeling of HCB in a real-time simulation environment [117] and fault studies [118] are also being done for HVDC applications.

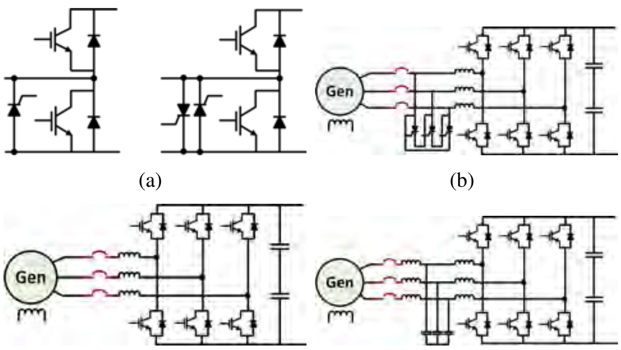
4) DC/DC converter isolation system: Fault isolation using dc/dc converter topologies with active bi-directional power control has also been suggested for the dc fault isolation. These topologies require controllable switches to handle the fault current. For such applications, the coordination between the fault detection algorithms and the converter controllers are critical design parameters, which is certainly different than in the case of DCCB based protection systems. The theoretical analysis of the resonant dc/dc converter has been done considering external dc faults [119], [120]. The study has been done for a 200-MW HVDC system interconnecting $\pm$ 44 kV with $\pm$ 250 kV dc bus. However, the drawback is the lack of galvanic isolation. Fault isolation using bi-directional dual active bridge (DAB) converter seems a promising option as it is able to restrict the flow of current while ensuring galvanic isolation during the worst pole-to-pole dc fault [121], [122]. The size of the converter might be reduced if operated in higher switching frequency. However, the DAB based dc/dc converter requires additional significant cooling arrangements. The dc/dc bridge with LCL filter [123] reduces the fault to a specified level, and the size might be reduced if operated at a higher frequency. However, the size of the passive components is a major concern and the operation is dependent on the selected passive parameters. Bi-directional buck-boost converter is another type of dc/dc converter [124], [125] which might be used for fault current limitation. The harmonic distortion on the phase currents is lowered but communication is required for control purpose. Using such dc/dc converters restricts the flow of fault current supplied by the source, but the terminal dc-link capacitor is always discharged. Most of the dc/dc converters employed for fault isolation are studied theoretically, and are supported only by scaled down experimental test setups. This is done to test the feasibility study of the dc/dc converters for the purpose of fault isolation. For higher power applications, it is assumed that parallel operation of the dc/dc converters would be carried out instead of single stage dc/dc unit. Future research and experimental studies are expected to be aligned towards the fault tolerance of the parallel dc/dc converter architecture.

The existing fault isolation techniques with suitable references are compared in Table VI.

B. Breakerless Operation: Fault Tolerant Generation System

The breaker-less protection or the converter based protection of the dc SPS is essentially achieved by interfacing the fault tolerant (FT) converter across the generation system. The FT converter obstructs the fault current contribution from the generation side to the fault location thus safeguarding the semiconductor switches of the converter and also the interfaced ac generator. The faulty section can be subsequently isolated using no-load isolating switches or low speed mechanical circuit-breakers [96]. In the dc SPS, 2L-VSC is envisaged to be widely utilised. Thus, the FT converter can be broadly classified into two categories: variants of 2L-VSC and emerging converter topologies. As per Section III-C, IGBTs will be turned-off owing to the over-current protection initiated by its gate driver circuit. Thus, the variants of 2L-VSC primarily aim in safeguarding the freewheeling diodes of the IGBTs till the generator circuit breaker (GCB) isolates the interfaced ac generator from feeding the fault current. The emerging FT converter restricts the flow of dc fault current till the fault is isolated. It is to be noted that the FT converter operates in conjunction with suitable fault detection algorithm as described in Section IV. The fault tolerant technologies are discussed in subsequent sections. A comparative study with suitable references has been listed in Table VII.

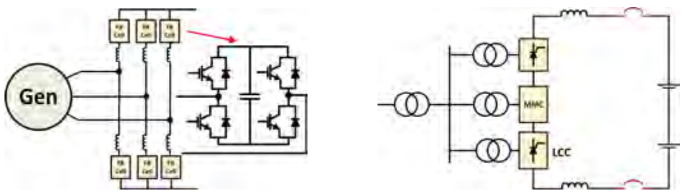
1) Variants of 2L-VSC: The freewheeling diode of the 2L-VSC is susceptible to damage by the fault current contribution by the generation systems. The variants of 2L-VSC have been designed to protect these diodes which is shown in Fig. 8. Single/double thyristor switches (Fig. 8(a)) might be connected in parallel with the freewheeling diodes which help in sharing the fault current and hence lowering the I^2t of the diodes [126]. Although this method reduces the current flow, the dv/dt of the switches is high during the fault conditions [127]. Thyristor assisted crowbar circuit (Fig. 8(b)) is another method that is a quite mature technology and is used in industries [127], [128]. However, this technique requires sufficient cooling arrangements and is dependent on the operation of the generator circuit-breaker. High inductance choke connected in the ac side (Fig. 8(c)) reduces the current intensity but increases the size and weight of the converter system. LCL filter in the ac side (Fig. 8(d)) [96], [129] has been proposed, which limits the fault current to a certain value while maintaining unity power factor. However, this method is limited by the bulkier size of L and C, and has complicated control. The protective inductor in the dc side can also be used to limit the fault current, but the determination of optimal inductance value remains a major concern [130].



(a) (b) (c) (d)

Fig. 8. Variants of 2L-VSC: (a) Parallel connection of freewheeling diodes, (b) crowbar circuit in the ac side, (c) high inductance choke in the ac side and (d) LCL filter in the ac side.

2) Emerging converter topologies: Apart from the variations in the 2L-VSC, emerging converter topologies have been proposed which can be useful in mitigating the fault current. The 4Q modular multilevel converter (4Q-MMC) and 2Q-MMC can suitably be used to limit the fault current [133], [134]. The capacitive discharge can completely be restricted by using 4Q-MMC. The cascaded H-bridge converters and H-bridge cells in the ac side [135], [136] is a mature technology and can be used to restrict the fault current contribution from the generator side. The alternate arm converter [137] and series VSC-LCC systems [138], [139] are some of the emerging converter topologies which can be used for the current limiting purpose. In spite of all the advantages, the emerging converter topologies are more suited for point-to-point HVDC transmission system. This is because of the significant power outage during their operation. In recent years, battery operated dc ferries have emerged for test purpose and covering shorter voyages [17]. A new converter topology employing current-fed buck-boost feature has been proposed which has fault tolerance capability [140]. Only simulation study has been reported, and experimental verification is yet to be done to confirm its performance under steady-state and transient conditions.



(a) (b)

Fig. 9. Emerging converter topologies (a) 4Q-MMC circuit and (b) series VSC-LCC circuit.

3) Choice of the interfaced generator: The selection of the generator can alter the characteristic of the fault current supplied from the ac side. The induction generator (IG), permanent magnet synchronous generator (PMSG) and the wound rotor synchronous generators (WRSG) are the traditional choices for the generation system of the dc SPS. The requirement of reactive power and additional power electronic interface hinders the adoption of the IG. The PMSG offers significant advantages but supplies huge fault current due to constant rotor flux. With all these limitations, WRSG with external field excitation is expected to be suitable for the generation system of dc ships. For such systems, the fault current contribution is dependent on the internal voltage of the WRSG. One of the prime factors responsible for maintaining this internal voltage is field excitation system. Suitable field de-excitation of the WRSG can be implemented to decrease this internal voltage hence lowering the fault current contribution. The fixed resistance de-excitation system is widely used in the industries to break the field current during the faults in the generator [141]–[144]. The schematic is shown in Fig. 10(a) where the switch

TABLE VI
REVIEW OF FAULT ISOLATION TECHNIQUES

	Method	Advantages	Disadvantages	Ref.
Modification of AC CB	Conventional ACCB	1) Already commecially available. 2) Uses arc quenching media like oil, SF_6 and vacuum. 3) Requires auxiliaries like arc chutes for arc extinguishing.	1) Might be larger in size. 2) Might not work properly for larger fault currents.	[98]
	Fuses	1) Simple operation and well known technology. 2) Fuse melts when the current exceeds a defined set-point.	1) After operation fuse must be replaced. 2) Cannot be used for protection co-ordination purpose.	[131]
	Reactor Assisted AC CB	1) Addition of reactor causes oscillation of fault current. 2) LC oscillator circuit required to induce zero crossing. 3) Provides galvanic isolation.	1) Initial current surge cannot be prevented. 2) Operation dependent on ACCB operating time.	[109]
	Hybrid CB	1) Combination of both electromechanical switches and power electronic components. 2) Current commutation is done using the power electronic switches.	1) In research and development stage. 2) Not yet economical.	[19], [95]
DC/DC Converter based Fault Isolation System	Dual Active Bridge	1) Limits the discharge from the dc-link capacitor. 2) Offers galvanic isolation. 3) High frequency operation resulting in reduction in transformer size.	1) Cooling arrangements for transformer. 2) Requires control of two units of 2L-VSC.	[121], [122]
	DC/DC Bridge with LCL filter	1) Fault current reduction is readily achieved at specified level. 2) Operation at higher frequency allows for reduction in inductor sizing.	1) The size of the passive components is concern. 2) Definitive selection of passive components for particular operating voltage and frequency.	[123]
	Bi-directional Buck Boost Converter	1) Low harmonic distortion on phase currents. 2) Low switching frequency of 2L-VSC resulting in high efficiency.	1) Capacitor current control. 2) Requires communication for control purpose.	[124], [125]
Solid State Circuit Breaker	Solid State Fault Current limiter (SSFCL)	1) Self triggered interruption capability. 2) Handles large amount of energy dissipation.	1) Not suitable for higher voltages. 2) One shot operation like fuses.	[19], [114]
	SCR based ACCB	1) Anti-parallel connection of SCR used for ac systems. 2) Performance improvement to overall power distribution system.	1) Significant thermal losses. 2) Not suitable for dc application.	[19], [95]
	IGBT/IGCT based ACCB	1) Series connection of the IGBTs/IGCTs. 2) Ability to detect the fault and turn-off in micro-seconds. 3) Limiting the fault energy.	1) More losses than the SCR based breaker. 2) Contacts must be opened as fast as possible.	[95]
	Bus Clamp Arrangement	1) Load side clamp is a simple freewheeling diode. 2) Ability to detect the fault and turn-off in micro-seconds. 3) Can have bi-directional control.	1) Long current decay time for inductive loads.	[95], [132]

$S1$ is opened after the fault is detected and the current in the inductive field circuit is dissipated through the fixed de-excitation resistance R_d. R_d should be chosen judiciously as using higher resistance could result in overvoltages across field windings and field circuit breaker.

To mitigate these overvoltages, nonlinear voltage dependent resistor (VDR) has been proposed which clamps the field voltage to a defined setpoint. For the field de-excitation systems, SiC and ZnO based VDRs are commonly used whose characteristics are shown in Fig. 10(b) [143]. ZnO based VDRs are mostly utilised for the low power field excitation systems. For high power systems, parallel combination of VDR is expected to be employed. Due to sharp transition of the V-I characteristics, parallel operation of ZnO based VDR is difficult hence paralleling of the SiC based VDRs are employed for high power applications. Further, the ZnO based VDR tends to explode when its energy absorption limits are exceeded. On the contrary, SiC based VDR cracks on reaching the upper limit [143]. Thus, the ZnO based VDR should be installed in an explosion proof chamber.

The values of the fixed resistance and VDR for field de-excitation is selected based on the ANSI/IEEE Std C37.18-1979 [142]. It has been observed that the higher value of

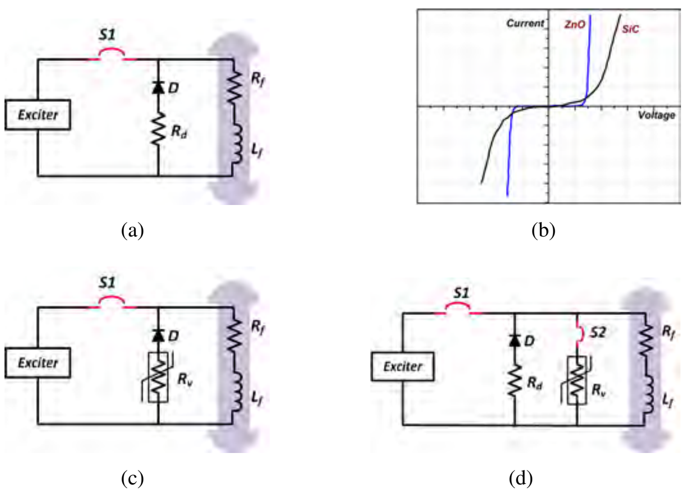


Fig. 10. De-excitation of generator using (a) fixed resistance, (c) voltage dependent resistance; and (d) combination of fixed resistance and VDR. (b) V-I characteristic of SiC and ZnO based VDRs.

discharge resistance is able to suppress the impact of the fault current but is limited by field overvoltage. The VDR maintains the field voltage thus having limited control over generator output current. If the fixed resistance and VDR are combined as shown in Fig. 10(d), their respective advantages can be harnessed and fault current can be reduced more appropriately. A higher value of fixed resistance can be used in Fig. 10(d) as compared to Fig. 10(a). During the fault $S1$ is opened and higher fixed resistance restricts the flow of field current thus reducing the generator output current. When the field voltage exceeds the prescribed limits, $S2$ is switched on to bring the VDR in-line thus restricting the field overvoltage. A preliminary result on the thermal capability (I^2-t) of the freewheeling diode during fault $F1$ in Fig. 2 with fault resistance of 0.01 Ω and comparing all the three types of de-excitation system is shown in Fig. 11. It can be seen that the fixed resistance and VDR based de-excitation has similar operating characteristics. The I^2-t value is reduced by 10% when the combination of fixed resistance and VDR is employed.

Although the fault current reduces with the de-excitation system, it is still enough to damage the freewheeling diodes as shown in Fig. 11 where the green line is the upper limit [45], [73]. The reduction of generator fault current is limited by the field inductance and higher time constant. Thus, de-excitation of the generator should be used in tandem with the FT converters. This could in-turn help in de-rating of the fault isolating devices such as DCCBs and FT converters.

VI. Reconfiguration of DC SPS

After the fault detection and isolation described in Section-IV and Section-V respectively; the reconfiguration becomes another important aspect of the fault management of dc SPS. Reconfiguration ensures continuity of power supply for the vessels undertaking complicated marine missions such as cruising [22], dynamic positioning [9]–[11], ice-breaking [12], naval warfare [8] etc. The reconfiguration of dc ship is governed primarily by selection of highly reliable bus architecture and load shedding techniques. The reconfiguration methods are described in the subsequent sections.

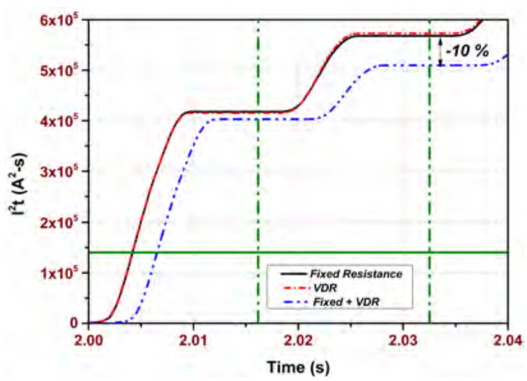


Fig. 11. Comparison of the I^2-t of the freewheeling diodes for fixed resistance, VDR and fixed resistance + VDR based field de-excitation system.

A. Bus Architecture of DC SPS

The dc common bus is the simplest architecture a dc SPS can have. This is a kind of radial distribution scheme where all the generation systems and the loads are connected to the common dc bus. The schematic of this topology is shown in Fig. 12(a) [6], [147], [148]. Other topologies include ring bus topology where the dc bus is running across the perimeter of the marine vessel which is shown in Fig. 12(b) [149]. The incoming generation systems and the outgoing loads are connected to the buses running along the port and starboard sides of the ship. The breaker and a half scheme [149] which is popularly used in the ac transmission systems (Fig. 12(c)) can also be considered for dc SPS. DC zonal electric distribution system has also been conceived where the ship is sectionalised into a number of electrical zones. The voltage of the main bus-bar is stepped down within the zone and then converted into three phase ac and dc. The emergency and vital loads are connected to both ports and starboard side of the bus via automatic bus transfer process [147], [150]. The schematic is shown in Fig. 13(a). The dc zonal electric distribution system offers the electrical isolation of the faults within an electrical zone through the use of converters [150]. As compared with the ac distribution system, dc zonal electric distribution system is able to switch uninterruptible dc loads on the healthy bus using auctioneering diodes [151].

In terms of reliability, dc zonal electric distribution system is most reliable architecture hence is employed for the naval applications. Following this is the breaker and a half topology which is more reliable than the ring bus but requires roughly 1.5 times as many circuit breakers as the ring bus. The common dc bus is least reliable and should not be used for the ships undertaking critical marine missions because of its poor post-fault reconfiguration capability. The ring bus distribution system has higher losses but lower transient over-currents. Further, the imbalances in the line impedances can result in common-mode currents and electromagnetic interference at switching frequencies. On the contrary, the radial network is prone to higher transient over-currents while offering lower system losses. Reliability and redundancy of the dc SPS can further be increased by using multiple buses [152]. Apart from the dc SPS, mixed ac/dc architecture shown in Fig. 13(b) is also proposed where the bulky line frequency transformers are removed by using dc distribution [148], [153], [154]. Further the integration of energy storage systems in the downstream converters could aid in minimizing the impact of de-energizing the dc bus during the fault detection, localization, isolation, and reconfiguration processes.

B. Load Shedding Methods

The reliable bus architecture of dc SPS ensures continuous power supply from the generator to the loads. However, during the faults, there is a significant mismatch of generation and loads. The voltage stability of the system can further

TABLE VII
REVIEW OF FAULT TOLERANT GENERATION SYSTEMS

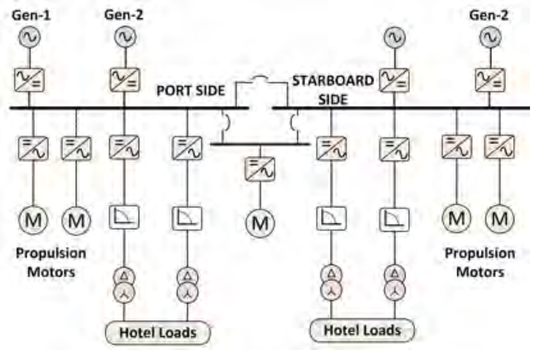
	Method	Advantages	Disadvantages	Ref.
Variants of 2L-VSC	Single/Double Thyristor Switches	1) Fault current gets divided hence saving the freewheeling diodes. 2) Easy to operate.	1) IGBT module becomes bulky. 2) The dv/dt remains same as before.	[126]
	Thyristor Activated Crowbar Circuit	1) Smaller size and lower weight. 2) Inexpensive thyristors. 3) Mature technology, used in industry.	1) Devices to be cooled down before re-starting. 2) Dependent on operation of GCB. 3) Susceptible to dv/dt.	[127]
	High choke in ac side	1) Mature technology. 2) Reliable component and easy to maintain. 3) Also reduces current ripple of the machine.	1) Possibly heavy and larger in size. 2) Increased cooling requirements. 3) Increased reactive power exchange and core losses.	[130]
	LCL in ac side	1) Limit fault current at specified value while maintaining unity power factor. 2) Reduction of harmonics.	1) Substantial size of L and C. 2) Complicated control.	[129]
	Protective Inductor in dc side	1) Limits the discharge from the dc-link capacitor. 2) Limits the fault current contribution from the generation side.	1) Difficult to determine exact value. 2) Possibly larger size.	[130]
Emerging Converter Topologies	2Q/4Q MMC	1) Less weight, transformerless design with high efficiency. 2) Capacitors do not discharge in case of 4Q-MMC. 3) Modular design thus minimising cost.	1) Complicated control circuit for voltage balancing. 2) Inductors required which adds weight and cooling burden. 3) High speed communication requirement for control purpose.	[133], [145]
	Cascaded H-Bridge Configuration	1) Modular design minimising production cost. 2) Capacitor does not discharge during faults. 3) Mature technology, used in industry.	1) Difficult to control and requires communication. 2) Higher initial cost due to additional components.	[135], [136], [146]
	H-Bridge cells in ac side	1) Low harmonic distortion on phase currents. 2) Low switching frequency of 2L-VSC resulting in high efficiency.	1) Capacitor current control. 2) Requires communication for control purpose.	[136]
	Series VSC-LCC converter	1) Combines the advantage of VSC and LCC. 2) Reliable component and easy to maintain. 3) Also reduces current ripple of the machine.	1) Complicated control algorithms. 2) Useful for point to point HVDC systems.	[138]
	Bipolar dc/dc Converter	1) Able to provide very high gain. 2) Able to restrict the fault current.	1) More suitable to integrate battery energy storage systems. 2) Increased number of circuit components.	[140]
Generator de-excitation System	Fixed Resistance based De-excitation System	1) Faster decay of generator current. 2) Limits the overcurrent contribution of the connected generators. 3) Mature technology and is used in the industry for rapid field de-excitation.	1) Higher de-excitation resistance might cause overvoltages across field windings. 2) Field circuit breaker also experiences over-voltage for higher de-excitation resistance.	[141], [144]
	Voltage dependent resistance (VDR) based de-excitation System	1) Limits the induced voltage across the field windings and field circuit breaker.	1) New technology hence immature. 2) Choice of type of VDR is a concern. 3) Difficult to operate in parallel operation.	[143]
	Fixed Resistance + VDR based de-excitation System	1) Better field de-exciting capability than fixed resistance and VDR based system.	1) Needs one additional switch. 2) The voltage setpoint at switch the switch connecting the fixed resistance needs to decided.	**

$**$: Proposed in this paper.

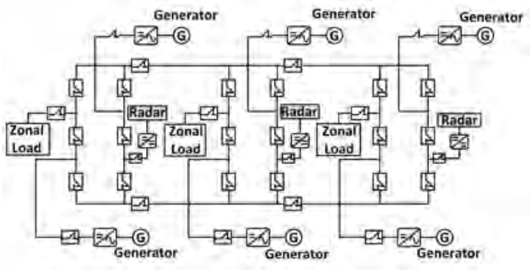
be jeopardized by the high bandwidth constant power loads (CPLs) [15]. This destabilization of the load might result in complete system blackout. One way to protect the system from collapsing is by implementing real-time load shedding algorithms [6], [155]. Unlike the land-based dc power systems, the loads in SPS are prioritized according to the marine missions [156]. Generally, the loads are classified in three groups namely vital; semi-vital and nonvital loads which are dependent on the ship mission. A variety of real-time load shedding algorithms are developed by prioritization of load for a particular mission [157]. Analytical hierarchy process (AHP) and expert control actions determination module (ECADM) has been developed to prioritize the load [158].

VII. CONCLUSIONS AND FUTURE RESEARCH NEEDS

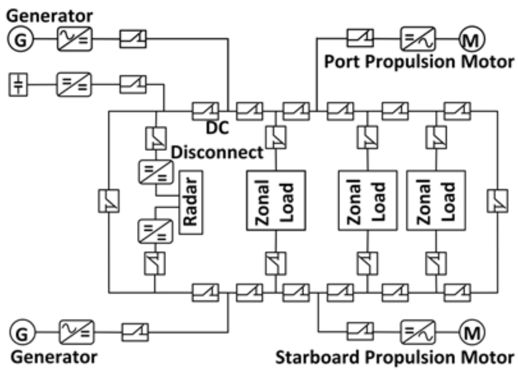
In the existing literature, the dc short-circuit fault management strategies are available primarily for the land-based dc microgrids and HVDC transmission systems. This paper reviews the operation, advantages and limitations of these strategies for the applicability in the dc SPS. It is seen that the different aspects of fault management such as fault detection, fault isolation, and reconfiguration are of equal importance and these are needed altogether to develop robust and comprehensive protection systems. The dc SPS being different from land-based dc systems, the requirements of the protection system would be dependent on various shipboard operating factors such as system configurations, marine missions and load conditions. Based on this, the following conclusions have been made for the future research needs:



(a)

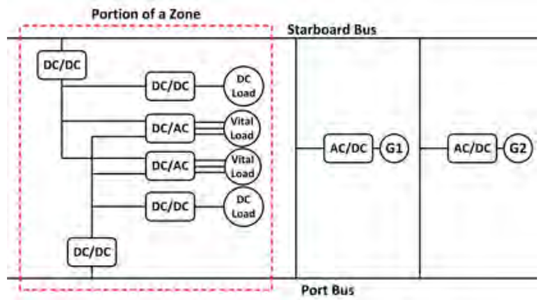


(b)

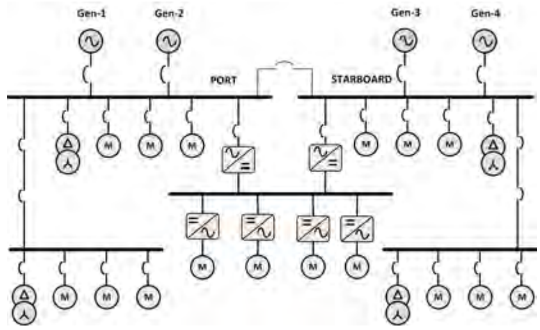


(c)

Fig. 12. Typical schematic of dc SPS (a) common dc bus topology, (b) breaker and half topology and (c) ring bus topology.



(a)



(b)

Fig. 13. Typical schematic of dc SPS in (a) zonal topology and (c) mixed ac/dc topology.

- The operation of the dc SPS is different from the land-based dc power systems such as dc microgrids and HVDC transmission system. Thus, before devising the required short-circuit fault management techniques, detailed modeling of the dc SPS is important to study its various operating modes and requirements. The detailed model of dc platform supply vessel [6], [159], [160] representing the representative dc SPS would be useful for such fault management strategies.
- After modeling of the dc SPS, fault study would be the next step to understand the transient responses. Due to rapid discharge of dc-link capacitors during the short-circuit, fault response in dc system is significantly different from the ac counterpart. In the ac systems, steady-state fault currents are used for protective relaying. However, for dc systems, transient discharge current is used for fault detection. Hence, a fault study is important before investigating the fault detection techniques [40], [51], [91].
- The selection of grounding for the dc SPS is one of the major concern. The high resistance ground schemes and isolated grounding conditions may be implemented to survive single earth fault. The solidly grounded system has its advantages although it results in severe fault currents during short-circuit faults.
- The dc SPS is also envisaged to be comprised of primary and secondary protection algorithms enabled with the selective operation as present in the ac power system. Although the ac protection algorithms cannot be directly applied to the dc SPS due to different fault current responses, some of the basic time-domain based ac protection systems such as directional protection [73], [91] and differential [18], [58] could be implemented in dc SPS. These algorithms require time-stamped current signals for their operation, thus requiring high-bandwidth communication infrastructure. Instead, noncommunication based frequency-domain analysis of the fault currents can be implemented, which has additional benefits of being immune to the noise present in the current/voltage signals [45], [61], [71]. However, due to compact nature of dc SPS, the frequency-domain methods have limited selective operating capability. Thus, there is a need of

communication for the fault management in dc SPS. Since there are no available standards of the communication networks to be implemented for dc protection [46]; the future trend could be focussed on the development of these protocols.

- Most of the fault detection techniques in the literature assume the ideal operation of the current sensor and the voltage sensor. Due to rapidly rising high fault current in dc SPS, these sensors might be damaged or become saturated. The sensors also introduce time-delays or may not accurately replicate the fault current waveforms. In this regard, Rogowski Coil could be one feasible option to adopt in dc SPS [40], [73]. However, it requires detailed modeling and additional integrator as discussed in this paper.
- The fault isolating devices pose another biggest challenge in implementing fault management systems in dc SPS. The modified ACCB with additional resonating branch takes longer time to operate whereas the SSCB has more conduction losses. As a result, the hybrid circuit breaker could be a feasible option. However, these DCCBs are conceived to be bigger in size with significant cooling arrangements. Since the dc SPS has space and weight limitations, breaker-less topologies might be preferred. In recent years, battery operated dc ferries have emerged. Such class of dc SPS could be integrated with the fault tolerant topologies to integrate the battery. In recent literature several FT converters are available. Of these the voltage-fed and current-fed dc/dc converter with buck boost and bipolar feature could be used to integrate battery energy storage systems. The additional feature of being able to restrict the fault current becomes another reason to adopt this topology [140].
- The reconfiguration of the dc SPS is dependent on the desired mission of ships. It is necessary to have an in-depth understanding of the shipboard missions before developing any reconfiguration algorithms [6]. Real-time testing of the reconfiguration algorithms along with the operation of fault detection and isolation techniques must be done to achieve a comprehensive fault management system.

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