AN EPROM CELL WITH A MAGNESIUM ELECTRONIC INJECTOR

Sik On Kong [1], Chee Yee Kwok[2], Sai Peng Wong[3]

[1] *Department of Electrical and Electronic Engineering, University of Auckland, New Zealand*
[2] *Department of Electronics, University of New South Wales, Australia*
[3] *Department of Electronic Engineering, Chinese University of Hong Kong, Hong Kong*

Abstract: By using Mg as the tunnelling electrode for an EPROM cell, it is shown in a control experiment that the tunnelling current is much enhanced while the tunnelling field is much reduced after a sintering procedure in which Mg reacts with the SiO_2 dielectric. Potentially, this may lead to faster programming, lower programming voltages and better programming endurance. An experimental EPROM cell has been made and has demonstrated programability.

Fowler-Nordheim (FN) tunnelling through a SiO_2 layer is a major mechanism for programming EPROM or EEPROM. The Fowler-Nordheim tunnelling current in a MOS structure is related to the barrier height (Φ) of the cathode material/SiO_2 interface by the usual FN equation [1]:

$$J = \frac{q^3 E^2 m_r}{8\pi h \Phi m_o} \exp\left[-\frac{4(2m_r)^{1/2}\Phi^{3/2}}{3\hbar qE}\right], \qquad (1)$$

where J is the current density; m_o is the rest mass of electron; m_r is the effective mass of electron in silicon dioxide; h is Plank's constant and $\hbar$ is $h/2\pi$.

The usual cathode materials used in EPROM or EEPROM are polysilicon or n+ single crystalline silicon. The barrier heights of these materials are about 3.2eV. By using magnesium, a low work function material, as the cathode, a previous experiment [2] has shown that the barrier height, with thermal oxide, is 2.2eV. It can be reduced to 1.2eV after sintering at 260°C. With a reduced barrier, the tunnelling current can be enhanced and the tunnelling field can be reduced simultaneously. Potentially, the enhanced current increases the programming speed and the reduced field relaxes the programming voltage requirement, and enhances the endurance of the EPROM/EEPROM in terms of the number of programming cycles achievable before failure.

Since Mg has a relatively low melting point (648.8°C), it has to be deposited after all the high temperature steps in an integrated circuit manufacturing process have taken place. Therefore, tunnelling has to be done in the upper layers, preferably through a polysilicon-oxide layer into the polysilicon floating gate (Fig. 1(a)).

As the polysilicon oxide surface is rough because of polysilicon grain boundary, another reduction of the applied tunnelling field is expected because of the sharp point field enhancement effect. Stronger sharp point effect and lower applied field can be achieved by overlapping the Mg electrode with one or more edges of the polysilicon floating gate.

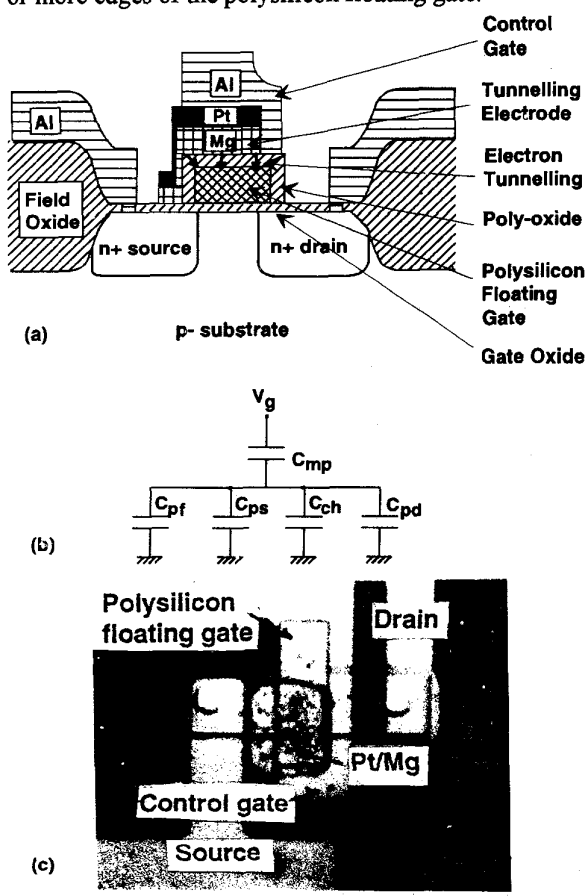

Figure 1 The EPROM cell with a Mg injection electrode: (a) the structure, (b) the equivalent circuit during the write operation, (c) Microscopic photograph of the cell fabricated.

Under such rough surface conditions, the observed current densities (J) becomes:

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Since SiO_2 has a very high bandgap of 8.1eV, it is likely that the band gaps of the three products are smaller than SiO_2, a reduced barrier at the interface is expected. Free silicon is always formed in the possible reactions. It should segregate out as submicroscopic bits. Tunnelling is therefore enhanced, again by the sharp point effect. It is a well known phenomenon that tunnelling is enhanced from a Si rich SiO_2 film [5].

Figure 3 is the depth profile of Auger Electron spectroscopy of a sintered sample. It can be seen clearly that MgO gradually decreases while SiO_2 gradually increases at the interface.

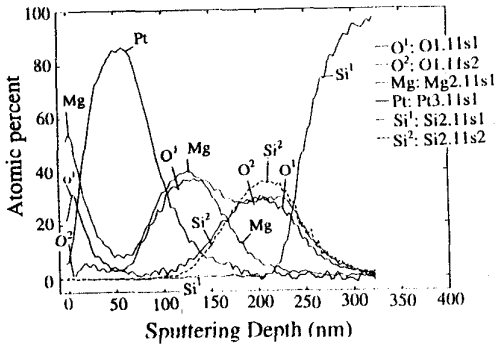

Figure 3 The depth profile of Auger electron spectroscopy of a Pt/Mg/SiO_2/Si sample, sintered at 260°C for 65 min.

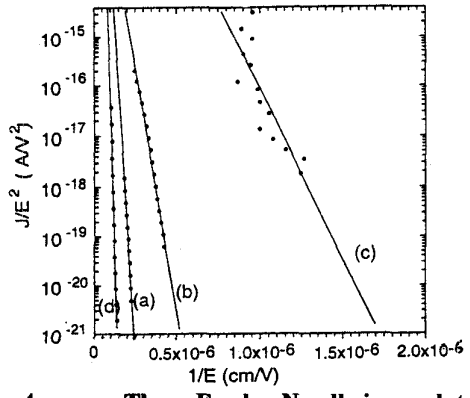

Figure 4 The Fowler-Nordheim plots of different samples, as in Fig. 2

Figure 4 shows the FN plots of the different samples. For the sintered Mg sample with an overlapped polysilicon edge. The values of the α and β for the simulation of the EPROM cell are evaluated to be 6.12×10^{-10} A/V^2 and 15.8 MV/cm respectively. A field enhancement factor of 3.6 and a tunnelling area ratio (A_r) of the order of 0.0012 is estimated from eq.(2).

The EPROM cell was fabricated by the following procedure. After a standard LOCOS process for NMOS up to the gate oxidation step, a layer of polysilicon was deposited, and was followed by a polysilicon-gate photomasking process and a polysilicon etching process. A phosphorus diffusion process was done to dope the drain, source and the polysilicon, with a solid diffusion source at a temperature of 950°C for 30 min. Then, a dry oxidation for the polysilicon and the source/drain region at a temperature of 1000°C for 25 min. was done.

The contact holes to the source/drain regions were defined by a contact photomasking process, followed by a dry etching step. A tri-level photomasking (photoresist/SiO/ photoresist) process was done to define the Mg electrode areas (holes in the three layers). A layer of Mg was thermally evaporated on the wafers, to a thickness of 300nm, followed by an E-beam evaporation of Pt with a thickness of 90nm. The metal layers on the resist layers were lifted off.

Another tri-level resist lift-off process was done to define the Al inter-connection layer, which was evaporated by an E-beam process to a thickness of 1μm. 10μm of Si was removed from the back side of the wafer. An Al layer was evaporated on the back side for the substrate contact. Finally, the wafer was sintered in N_2 ambient at 260°C for 185 min., to reduce the barrier height of the Mg/Polysilicon oxide interface. The microscopic photograph of the fabricated cell is shown in Fig. 1(c)

The wafers were then exposed to UV light in an EPROM eraser, to clear up the charge in the floating gate. It was then probed in a probing station connected to a curve tracer, for the erased characteristics. Square pulses of -25V with different duration was applied to the control gate, while the source, drain and the substrate were grounded. The wafer was then reprobed for the written characteristics.

Following a similar mathematical derivation as described by Kolodny et. al. for FLOTOX EEPROM [6-8]. The threshold voltage (V_{tw}) as a function of time is given by:

$$V_{tw}(t) = V_{ti} - V_g - \frac{\beta X_{mp}}{K_w \ln\left\{\left(\frac{A_{tun}\alpha\beta}{X_{mp}C_{total}}\right)t + \exp\left[\frac{\beta X_{mp}}{K_w\left(-V_g + V_{ti} - V_{tw}(0)\right)}\right]\right\}} \quad (4)$$

where A_{tun} is the tunnel window area where the Mg overlaps the floating gate, V_{ti} is the threshold voltage with zero charge in the floating gate, V_g is the applied programming voltage. K_w is the coupling constant of the cell and is given by:

$$K_w = \frac{C_{ps} + C_{ch} + C_{pd}}{C_{total}}, \quad (5)$$

$$J = A_r \frac{q^3 (E_r E)^2 m_r}{8\pi h \Phi m_o} \exp\left[-\frac{4(2m_r)^{1/2} \Phi^{3/2}}{3\hbar q (E_r E)} \right] \quad (2)$$

where E_r is the field enhancement factor that depends on the radii of the sharp points, and A_r is the reduced area ratio, which accounts for the fact that the tunnelling area of a rough surface at the asperities is much smaller than that of a flat surface.

The above equation can be put into a simpler form as shown below

$$J = \alpha E^2 \exp\left[-\frac{\beta}{E} \right] \quad (3)$$

To find the values of α and β, Pt/Mg/Polysilicon oxide/n-polysilicon MOS structures were made [3]. The polysilicon oxide layer was grown with dry oxygen at a temperature of 1000°C for 25 min. The thickness of the oxide was 48nm. Circular dots of Mg (200nm) covered by Pt (9nm) of area 0.05mm^2 were made by evaporations and photolithographic lift-off technique. The Pt layer protected the Mg layer from oxidation. Part of the wafer was sintered in N_2 at 260°C for 185 min. The IV characteristics of the samples were measured by a force current-measure voltage technique [2], and is shown in Fig.2.

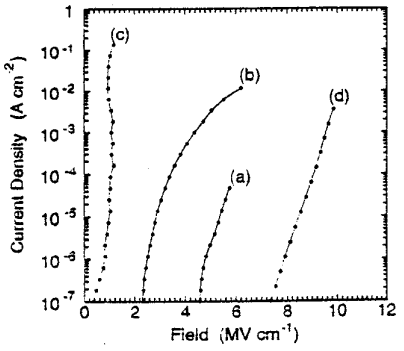

Figure 2 The current density versus field plots of Fowler-Nordheim tunnelling from (a) unsintered Mg/polysilicon oxide interface, (b) Mg/polysilicon oxide interface, sintered at 260°C for 185 min. (c) The Mg/polysilicon oxide interface, sintered and overlapping a polysilicon edge (d) n+polysilicon /thermal oxide interface in a n+ poly/thermal oxide/p-Si structure

The highest point of each curve in Fig.2 is the maximum current before oxide breakdown. It can be seen that the starting field (J=10^{-7} A/cm^2) of the original Mg/poly-oxide sample is 4.6 MV/cm. It is reduced to 2.3MV/cm after sintering (reasons to be discussed later), and is further reduced to 0.8 MV/cm when the Mg dot overlaps a polysilicon edge. These figures compared favourably with the starting field (7.3MV/cm) of the polysilicon/thermal oxide control sample, which simulates the injection interface of a conventional EPROM.

By sintering the Mg/poly-oxide sample, the maximum current density increases from 5x10^{-4} A/cm^2 to 1x10^{-2} A/cm^2, and further increases to 1.5x10^{-1} A/cm^2 when the injection electrode overlaps a polysilicon edge. This is because the reduced field produces less damage to the oxide during FN tunnelling. The maximum current density of the polysilicon/thermal oxide sample is higher than that of the sintered Mg/polysilicon oxide sample despite the higher tunnelling field of the former. This is because sample (d) was prepared in a better clean room while samples (a)-(c) were prepared in uncontrolled environment.

The reduction of the tunnelling field due to sintering of the Mg layers can be explained as follows: From the thermochemical point of view, the possible reactions that can occur between Mg and SiO_2 at the interface at 260°C can be determined by a negative change in the Gibb's free energy (ΔG), which can be calculated from the data listed in the Janaf table [4]. The possible reactions are listed below:

$2Mg+SiO_2 \rightarrow 2MgO+Si$	ΔG= -65.4 KCal, {1}
$2Mg+2SiO_2 \rightarrow Mg_2SiO_4+Si$	ΔG= -80.6 KCal, {2}
$2Mg+3SiO_2 \rightarrow 2MgSiO_3+Si$	ΔG= -82.8 KCal, {3}
$Mg+2SiO_2 \rightarrow MgSiO_3+SiO$	ΔG= +20.4 KCal,{4}
$2Mg+3SiO_2 \rightarrow Mg_2SiO_4+2SiO$	ΔG= +43.1 KCal,{5}
$Mg+SiO_2 \rightarrow MgO+SiO$	ΔG= +29.1 KCal,{6}
$2Mg+SiO_2 \rightarrow Mg_2Si+O_2$	ΔG=+177.6KCal.{7}

It can be seen that among the seven reactions, only {1-3} have negative ΔG values and are, therefore, possible. ΔG values of the three possible reactions are close to each other, therefore it is likely that all three reactions occur to some degree. The products of the three reactions: MgO, Mg_2SiO_4, $MgSiO_3$ can be described as $(MgO)_x.(SiO_2)_y$. The oxidation-reduction (redox) reaction {1} can, therefore, be viewed as the "principle reaction", where Mg is oxidised to MgO, and SiO_2 is reduced to Si. Reactions {2-3} can be viewed as the redox reaction, followed by the association of MgO into the SiO_2 lattice in the form of magnesium silicate complexes. As the ratios of y/x follow the ascending order from the first product to the third one, the interface layers should therefore be Mg/MgO/ Mg_2SiO_4/$MgSiO_3$/SiO_2.

where C_{ps} is the floating gate/source overlap capacitance; C_{ch} is the channel capacitance; C_{pd} is the floating gate/drain overlap capacitance; C_{pf} is the floating gate/field oxide overlap capacitance, and $C_{total}=C_{ps}+C_{ch}+C_{pd}+C_{mp}$, where C_{mp} is the metal/floating gate overlap capacitance (see Fig 1b).

Figure 5 shows the Igs/Vg curves of the erased and the written cell. The latter is taken after a write operation with a square programming pulse of -25V and 2.8ms duration. It can be seen that the threshold voltage of the erased cell was -4V, and was changed to 6V after the write operation. The threshold voltage did not change after the written cell was left at room temperature for 2 weeks. However, the cell was erased after heating in an oven at 150°C for 10 min.

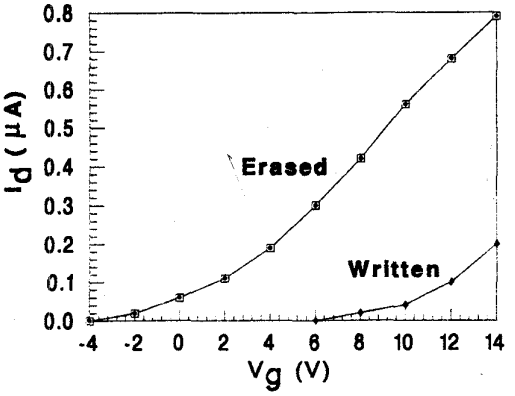

Figure 5 The I_d/V_{ds} characteristics of the erased and the written cell

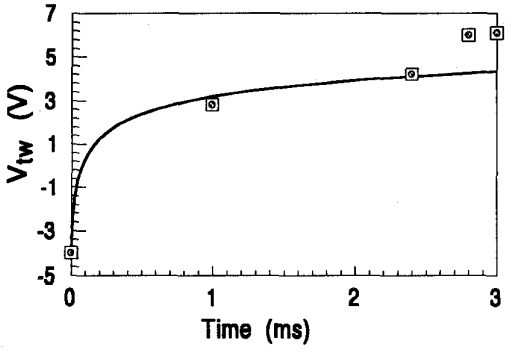

Figure 6 The experimental (dots) and the simulated (line) threshold voltage change during the write operation (V_{tw})

Fig. 6 shows the experimental and simulated values of and V_{tw} versus time during the write operation. The V_{tw} graph shows reasonable agreement between the experimental and the simulated data.

The experiment was only aimed to have the first working Mg EPROM cell fabricated. The structure and the parameters of the cell were quite conservative. the advantages of the Mg EPROM cell have not been fully demonstrated. The thicknesses of the gate oxide and the poly-oxide were limited by the dust particle content of the laboratory environment, which can be improved if the cell is fabricated in a better clean room.

The programming speed of the cell is limited by the large cell geometry, relatively low current density level used and the square programming waveform. The latter produces a non-uniform current density which decreases drastically after the start. Computer simulation shows that a programming time of 11μs is achievable, using cell parameters compatible with up-to-date technology, a programming current density of 0.1 A/cm^2, and a trapezoidal programming waveform [9].

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