Tunnel Diode-Transistor Binary Scaler

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(Received 6 October 1967; and in final form, 27 November 1967)

This paper describes a new type of tunnel diode-transistor binary scaler which is very simple in concept and in design. It is capable of operating reliably at input pulse repetition rates in excess of 200 MHz. A significant feature of the scaler is that there is no maximum input pulse width restriction. Input and output circuits which allow the scaler to operate over a wide range of input driving conditions and to be cascaded directly with similar scalers are also presented.

INTRODUCTION

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CALERS capable of operating with input pulse repetition rates greater than 100 MHz are common but most require input pulses of width less than a specified maximum. A simple scaler which operates reliably with no maximum input pulse width restriction is described in this paper. The basic arrangement of the scaler is shown in Fig. 1. Essentially it consists of a long-tailed pair with regenerative feedback from the collectors to the opposite bases via level-shifting Zener diodes. The tunnel diodes in the emitter leads provide the necessary memory elements of the binary. This circuit technique was originally devised by K. L. Tan1 and employed by him in a binary scalar of somewhat similar circuit configuration but completely different design philosophy and mode of operation.

PRINCIPLE OF OPERATION

In the two steady-state conditions either T1 or T2 is conducting. Assuming that initially T1 is on, then TD1 is biased in the low voltage state A by the current I3 flowing through it (see Fig. 2). The collector potentials Vc1 and Vc2 are (I1+I3)R and I2R, respectively. When an input current ΔIin is supplied to the long-tailed pair it raises Vc1, and consequently Vc2, by ΔIinR. If ΔIin is large enough, TD1 switches to the high voltage state B and Vc3 rises by about 0.5 V (Vt for Ge tunnel diodes). By selecting the value of R such that

Vc3< Vc2 + Vt

when ΔIin switches TD1 to state B and

Vc2> Vc2 + Vt

when ΔIin is removed and TD1 is in state C, T2 is forced to remain off until ΔIin is removed. Vt is the emitter-base voltage when T2 commences to conduct. On removal of ΔIin, T2 starts to conduct and I3 is transferred from T1 to T2, the process of transfer being assisted by the regenerative feedback loops. Tunnel diode TD1 reverse switches when its current falls below Ia. In the other condition T1 is off and T2 is on and TD2 is biased in the low voltage state A. The next input pulse will return the scaler to its initial condition of T1 on and T2 off.

From the above description it is evident that there is no maximum input pulse width restriction. The minimum width is that necessary to ensure the switching of the tunnel diodes. Figure 3 shows the variation of Vc1 and Vc3 when input pulses are applied to the scaler. Either collector potential change can serve as an output for the scaler.

DESIGN CONSIDERATIONS

In any scaling circuit there are two sets of design conditions, one set necessary for proper operation and the other set desirable for optimum performance. With reference to the notation of Figs. 1 and 2, the necessary design conditions for the scaler are as follows:

(1) The input current ΔIin must be sufficient to switch

Fig. 1. Basic arrangement of scaler.

Fig. 2. Static characteristic diagram of tunnel diode.

2 To avoid unnecessary complexity the α's of the transistors are assumed to be equal to unity.

This voltage is assumed to be 0.3 V below Vbe, the emitter-base 'knee' voltage. For Ge transistors Vt=0 and for Si transistors Vt=0.5 V.
either TD1 or TD2, depending on which is biased by the current $I_b$, i.e.,

$$ (I_b + \Delta I_{in}) > I_{p \text{ max}}. $$

(2) The off-transistor must remain non-conducting when $\Delta I_{in}$ is present and commence conducting when it is removed, i.e.,

$$ (I_x + I_B + \Delta I_{in}) R + V_x + V_i > (I_x + I_b) R + V_x + V_i, $$

which, on substitution of $(I_x R + V_x + V_{eb} + V_f)$ for $V_i$, reduces to

$$ (I_x + \Delta I_{in}) R + V_x > V_{eb} + V_f > I_x R + V_i $$

and since $(I_x + \Delta I_{in})$ must be greater than $I_{p \text{ max}}$,

$$ I_{p \text{ max}} R + V_x > V_{eb} + V_f > I_x R + V_i. $$

(3) When $\Delta I_{in}$ is removed, the switched tunnel diode must remain in the high voltage state to allow the off-transistor to conduct and establish a complete transfer of the current $I_b$ in the long-tailed pair, i.e.,

$$ I_b > I_{v \text{ max}}. $$

(4) For fast rise input pulses the switching time (i.e., delay time + rise time) of the on-transistor must be greater than that of the switching tunnel diode to ensure that the off-transistor does not start to conduct when $\Delta I_{in}$ is applied.

Conditions (1), (2), and (3) can be satisfied by the choice of values for $I_b$, $\Delta I_{in}$ and $R$. Figure 4 summarizes conditions (2) and (3) by graphically showing permissible values for $R$ and $I_b$ (shaded region) for a scaler employing Ge transistors and tunnel diodes. Typical values of 0.3 V and 0.5 V are assumed for $V_{eb}$ and $V_f$ respectively, $V_i$ in this case is zero. Condition (4) can be met by appropriate selection of transistor and tunnel diode types.

The following are desirable for optimum performance:

(1) High speed transistors and tunnel diodes should be used for maximum speed of operation.

(2) Voltage swings should be kept small to minimize the effects of circuit capacitances. It is desirable therefore for $\Delta I_{in}$ and $R$ to be small.

(3) The current switched in the long-tailed pair is $I_b$ so that a small value of $I_b$ improves the speed of the current transfer and also reduces delay in reverse switching the tunnel diodes.

(4) Zener diodes with equal $V_x$'s should be used. However, if matched Zener diodes are not available, one of the $I_x$'s may be varied to achieve the necessary equalization of the minimum levels of $V_{al}$ and $V_{bl}$.

**PRACTICAL CIRCUIT**

The practical circuit of the scaler is shown in Fig. 5. An examination of Fig. 4 indicates that a 10 mA tunnel diode is a reasonable choice, as a 5 mA type tends to
dictate a rather high value of \( R \), and a 20 mA type demands large input and bias currents. The practical values of \( I_b \), \( \Delta I_{in} \), \( R \), etc. are selected in accordance with the stipulated conditions. It should be noted that although npn transistors are used in the long-tailed pair, pnp types, with appropriate bias changes, will serve just as well. When the latter type transistors are used, negative input pulses are necessary. Ancillary long-tailed pairs are employed as input and output coupling circuits. The use of npn transistors in these circuits eliminates any level-coupling problems, thus allowing direct connections to be made. The final output is a current pulse capable of driving another scaler directly.

**PERFORMANCE**

With GE 1N3719 tunnel diodes, the scaler operates very reliably up to a maximum input repetition frequency of about 120 MHz. It is insensitive to changes (±10%) of power supply levels. Practical waveforms showing the scaler operating at input repetition rates of 10 and 100 MHz are shown in Figs. 6(a) and 6(b), respectively. If reference is made to the notations used in the practical circuit these figures are self-explanatory.

**ACKNOWLEDGMENTS**

The authors would like to thank Dr. J. B. Earnshaw for his comments and continual encouragement. The generous financial support of the New Zealand Universities’ Research Grants Committee for the authors’ current research program is gratefully acknowledged.

\(^4\) The 2N976’s used were the fastest switching transistors locally available at the time of the scaler’s development.