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Adaptive Protection for Smart Grids

by

Craig M. Smith

A thesis submitted in fulfillment of the requirements for the degree of Master of Engineering

in the
Department of Electrical and Computer Engineering
University of Auckland
New Zealand

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“The important thing is not to stop questioning; curiosity has its own reason for existing. One cannot help but be in awe when contemplating the mysteries of eternity, of life, of the marvellous structure of reality.”

Albert Einstein (1879 - 1955)
Abstract

Traditionally, distribution networks only have a single source upstream with loads connected downstream so the network parameters are well known and the network can be protected using relatively inexpensive devices such as fuses. With the advent of distribution generation (DG), storage, microgrids and scenarios such as islanding in distribution networks new protection schemes will be required. The advent of smart grids also creates opportunities for improved protection schemes.

The main goal of this research was to investigate future smart grids with regards to the challenges they will face with protection. To achieve this the distribution network was investigated in terms of its topology, protection devices and protection schemes which are currently implemented. Next, new advances such as smart grids, distributed generation and the challenges and opportunities this will create in the distribution network were investigated. To investigate the type of faults and fault waveforms likely to be encountered by protective devices in future distribution networks a distribution feeder was simulated in PSCAD with distributed generation (DG). The types of faults that may occur were analysed and fault waveforms generated and analysed. It was observed that a decaying DC offset is a significant component in the fault waveforms when DG was added to a distribution network. The level of the decaying DC offset was shown to be inversely proportional to the series impedance between the source and fault to ground which includes the impedance of the source, the distribution line and the fault impedance. The instant in which the fault occurs also has a large effect on the peak level of the decaying DC offset in the fault current waveform with the highest peaks occurring at a phase offset of $\frac{3\pi}{4}$ and $\frac{3\pi}{2}$.

The presence of decaying DC offset in the fault waveform has implications for protection devices such as overcurrent relays as the algorithms they use can be susceptible to errors in estimating phasors when decaying DC offset is present in the fault waveform. In current distribution networks the protection is not required to act quickly which means that extensive filtering can be implemented to remove the decaying DC offset as the additional time delay it causes will not be a problem. However with increased amounts of DG being connected to the grid there is expected to be a requirement for faster acting protection. Protection will need to be fast enough to act quickly in this scenario to protect the DG sources so there is a requirement for faster, more accurate phasor estimation algorithms for digital relays that can filter out DC offset.

A test platform was designed and implemented to assess protection algorithms. Phasor estimation using the Discrete Wavelet Transform has been proposed as an alternative to
the Discrete Fourier Transform and both of these algorithms were implemented to run concurrently in a digital relay. A method for overcoming a limitation of the proposed phasor estimation using the DWT algorithm by using a second reference waveform with a phase offset was found and implemented. It was determined that the computation power required to implement phasor estimation using the DWT is similar to the current DFT algorithm and in some cases is likely to be even less so can be implemented on current hardware.

The phasor estimation algorithms were critically assessed using fault waveforms simulated from a distribution feeder with DG and from mathematically generated waveforms. The performance of the Haar, Daubechies 4, 8 and 10 wavelets and different decomposition levels of the DWT were assessed. When the waveform contains harmonic components there is no significant advantage of phasor estimation when using the DWT over the DFT. Changing the wavelet type or the recursion level of the DWT also had little effect. When a decaying DC offset is present in the fault waveform the DWT is heavily affected in both half cycle and full cycle implementations. In comparison the DFT is able to filter the majority of it out with a full cycle implementation. In regards to convergence, the DWT has an advantage over the DFT and reaches the new set point 82% faster with the half cycle implementation. It was found that higher levels of recursion of the DWT have a positive impact on the rate of convergence. There was no advantage found when there is an error in fundamental frequency, phasor estimation using both the DWT and the DFT had significant errors.

From this we can determine that phasor estimation using the Discrete Wavelet Transform does not offer any significant advantage to justify its use over the existing standard algorithm, the Discrete Fourier Transform. There is potential however for its use to increase accuracy when there is a variation of frequency of the fundamental. On a future distribution network that is expected to include Distributed Generation, the decaying DC offset present during faults would cause large inaccuracies in the phasor estimation when using the Discrete Wavelet Transform. If phasor estimation were to be implemented, a method of removing the decaying DC offset would need to be applied before the signal was passed to the algorithm.
I dedicate this thesis to my family and to my friends in the Auckland University Tramping Club and the Auckland University Rock & Alpine Club. Without the encouragement, inspiration and support I received from all of you I would never have got this far.
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This research has been carried out in fulfilment of the requirements for the Master of Engineering degree at the University of Auckland in the Department of Electrical and Computer Engineering.

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Craig M. Smith
8th January 2010
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Abbreviations

ADC    Analogue to Digital Converter
Codec  Coder-Decoder (typically containing one or more ADCs and DACs)
CT     Current Transformer
CTI    Coordination Time Interval
DAC    Digital to Analogue Converter
Db4    Discrete Wavelet Transform using the Daubechies 4 Wavelet
Db8    Discrete Wavelet Transform using the Daubechies 8 Wavelet
Db10   Discrete Wavelet Transform using the Daubechies 10 Wavelet
DFT    Discrete Fourier Transform
DG     Distributed Generation
DSP    Digital Signal Processor
DWT    Discrete Wavelet Transform
FFT    Discrete Fourier Transform using the Fast Fourier Transform algorithm
FIR    Finite Impulse Response filter
Haar   Discrete Wavelet Transform using the Haar Wavelet
IDMT   Inverse Definite Mean Time
IEEE   Institute of Electrical and Electronic Engineers
I²S    Integrated Interchip Sound
IP     Intellectual Property
PC     Personal Computer
PLL    Phase Locked Loop
SPI    Serial Peripheral Interface
TCP/IP Transmission Control Protocol/Internet Protocol
VT     Voltage Transformer
Chapter 1

Introduction

1.1 Background Study

Although much research has been reported for protection of transmission networks using digital relays, there is enough scope to assess issues in distribution networks. Traditionally, distribution networks only have a single source upstream with loads connected downstream so the network parameters are well known and the network can be protected using relatively inexpensive devices such as fuses. With the advent of distribution generation (DG), storage, microgrids and scenarios such as islanding in distribution networks new protection schemes will be required. The advent of smart grids also creates opportunities for improved protection schemes.

Currently digital relays used in distribution networks predominately use phasor estimation techniques based on the Discrete Fourier Transform (DFT). These filtering algorithms work well in conditions when the input waveforms are purely sinusoidal and do not have a high rate of change, however the current and voltage signals during the fault interval often contain large harmonics and an exponentially decaying DC offset which can cause large inaccuracies in calculating the fundamental components. Other phasor estimation techniques such as LES [1, 2] have also been proposed.

One of the challenges with phasor estimation is filtering out the decaying DC offset present in fault signals. Decaying DC offset affects the accuracy of the phasor estimation algorithms. Many solutions have been proposed [3–7] but this is still an area of ongoing
research as there is always demand for algorithms to be faster and more accurate in estimating the phasors.

Current algorithms used in digital relays are the Discrete Fourier Transform for phasor estimation, with digital mimic filtering being employed to remove the decaying DC offset before the signal is processed by the Discrete Fourier Transform. Digital mimic filtering relies on the fact that the network characteristics that affect the decay rate such as the network impedance are constant and predictable, however in a distribution network this may not always be the case.

The Discrete Wavelet Transform (DWT) has also been proposed as an alternative to the Discrete Fourier Transform in recent literature [8–10]. Osman and Malik [9] suggest that the Discrete Wavelet Transform converges significantly faster than the Discrete Fourier Transform. Feng and Jeyasurya [10] conclude through simulation that the Discrete Wavelet Transform converges faster than the Discrete Fourier Transform but mentioned that it has poorer performance when a DC offset is present.

Brahma and Kavasseri [11] also compare the performance of the Discrete Wavelet Transform with the Discrete Fourier Transform for phasor estimation but this is based on simulations. Silva, Neves and Souza [12], Chi-kong, Ieng-tak, Chu-san, Jing-tao and Ying-duo [8] also compare these but no practical implementations are assessed.

### 1.2 Research Motivation

The motivation behind this thesis is to improve protection for future distribution networks by first investigating distribution network faults, then by evaluating the potential for using and implementing the Discrete Wavelet Transform algorithm for phasor estimation, specifically for future smart grids.

### 1.3 Aims and Objectives

The main goal of this research was to investigate future smart grids with regards to the challenges they will face with protection. This will advance the knowledge of protection
for smart grids and assist in integrating distributed generation, managing microgrids and islanding and other aspects of future smart grids.

The first objective of this research is in two parts. The first part is to investigate the current distribution network in terms of its topology and the protection devices and protection schemes which are implemented. The second part is to investigate new advances that are being implemented such as smart grids, distributed generation and the challenges and opportunities this will create in the distribution network.

The second objective was to simulate a current distribution network using software such as PSCAD and investigate the types of faults that may occur, the expected fault waveforms that a protection device is likely to encounter and then investigate how this may change with the advent of new technology such as smart grids and distributed generation.

The third objective was to implement a test platform for use in analysing algorithms for use in smart grid protection. Commercial relays are protected by IP and therefore their internal software algorithms cannot be assessed, nor can new algorithms be tested on an existing commercial relay platform. Implementation of an open platform will allow evaluation of both current protection algorithms and proposed algorithms and accurate comparisons to be made. Many algorithms have been proposed but not all have been tested in an actual implementation. This objective will focus on the Discrete Wavelet Transform and will research any barriers with regards to implementation of this algorithm in a relay, look at the optimal way of doing this and what hardware resources will be required. It will then critically assess and compare current standard phasor estimation using the Discrete Fourier Transform algorithm with the proposed phasor estimation using the Discrete Wavelet Transform algorithm and determine any benefits it may have with regards to faults that would occur in future smart grids.

1.4 Scope of the Thesis

Chapter 1

This chapter introduces the topic and explains the motivations behind the thesis. It gives an overview of the contents of the thesis and contains the literature review of
the topics covered. It also details what was achieved, the contributions made and the peer-reviewed publications that were produced as part of the research.

Chapter 2

This chapter is in three parts. Firstly, existing protection schemes and devices for distribution networks are investigated. Next future developments to distribution networks such as distribution generation, smart grids and communication are investigated. Thirdly an existing distribution feeder based on a standard IEEE feeder is simulated and analysed. The distribution feeder is then modified to include distributed generation and the effects during faults are investigated. The fault waveforms are captured and stored to be used later in Chapter 4 to evaluate the protection algorithms in the implemented test platform.

Chapter 3

This chapter details the design and implementation of a digital relay, from the hardware design through to the algorithm development and then the incorporation of phasor estimation algorithms in the relay.

Chapter 4

This chapter compares the two algorithms used for phasor estimation (the Discrete Fourier Transform and the Discrete Wavelet Transform) using the hardware and software platform developed in Chapter 3. The computational efficiency and requirements of each of the algorithms was assessed and the algorithms compared by testing with both mathematically generated waveforms and simulated distribution network fault waveforms produced in Chapter 2. The tests include fault signals containing harmonics, decaying DC offset and variations in the fundamental frequency. The rates of convergence of the algorithms were also compared.

Chapter 5

This chapter summarises and concludes the thesis.

Chapter 6

This chapter suggests some possible directions for future research.
1.5 Publications

The main contribution of this Masters research has been the evaluation of an implementation of the Discrete Wavelet Transform algorithm for use in phasor estimation in digital relays as evidenced by the two papers published by the author [13, 14]. The contents of these papers are expanded on in Chapter 3 and Chapter 4. The other contribution is the investigation of the emerging distribution network and analysis of the effects on protection of adding distributed generation to distribution networks detailed in Chapter 2, of which the evaluated Discrete Wavelet Transform algorithm is intended to be applied to.

During the course of this research the following peer-reviewed contributions were published or are under preparation. The research for these publications was all carried out by the author.


4. C. M. Smith, N. C Nair, Investigation of Decaying DC Offset in Fault Waveforms with Distributed Generation, (Manuscript under preparation)
Chapter 2

The Emerging Distribution Network

2.1 Introduction

This chapter is in two parts. The first part investigates the distribution network as it is today in terms of its topology and protection devices. It then investigates future developments such as smart grids and the effect they will have on protection as well as the new opportunities they offer for more advanced protection schemes.

The second part models a distribution feeder with integrated distributed generation (DG) to investigate the types of faults that may occur in future distribution networks. In order to determine the source of some of the features of the fault waveforms, certain network parameters are varied and the results analysed. The results are then compared with a verified model of another distribution feeder.

2.2 Current Distribution Network

Traditionally distribution networks are radial in design, with a single upstream source from the transmission network connected via a substation. The substation typically steps down the voltage from the transmission network at 100kV or higher down to something in the range of 11kV using a transformer. This is in contrast to the transmission network
which consists of multiple sources and loads, and often multiple sets of transmission lines connecting them so if a fault occurs on any one of these items power can often be rerouted and the transmission network can continue to function in partial capacity until the fault is fixed.

Since there is a single source in a distribution network the direction of power flow is only one way, from the substation spreading out radially through the feeder to the loads. The number of customers it serves is typically a lot less than a transmission network, where a transmission network may serve one or more cities, a distribution feeder may only serve a single suburb. This means that in a distribution network, cost and simplicity is a more critical factor than reliability, as if there is a fault the distribution network can shut down while only affecting a small number of customers. When customers need higher reliability they can be supplied with a secondary backup power source, or connected directly to a substation.

2.3 Protection Devices in a Distribution Network

2.3.1 Fuses

Fuses are the most common type of protective device used in a distribution network currently. Fuses are comparatively simple and cheap devices that are only used once and become open circuit once a specific current threshold is reached. [15] The two key protection settings for fuses are their minimum melting and total clearing times and the corresponding current levels. The minimum melting time is the time it takes for the fuse to become open circuit once the specified threshold current has been reached. The total clearing time is the minimum melt time plus the time it takes for the resulting arc to be extinguished.

Fuses have the advantage that as they operate based on the heating effect on a resistive element they are not susceptible to phenomena such as harmonics, frequency drift or DC offset which may be present in a fault signal. A disadvantage of fuses is that they are not adaptive to changes in the system so, once blown, require replacement. They also have no communication ability, so the only way to determine if they require replacement is to monitor the network downstream.
2.3.2 Automatic Circuit Recloser

The majority of faults in a power system (over 80%) are temporary and using reclosers allows the protection system to react and isolate the fault and then, after a preset time to allow the fault to clear, they can ‘reclose’ and reconnect the faulted area to allow the least disruption for customers. They can act either instantaneously or with a time delay and will attempt to ‘reclose’ the circuit a predetermined number of times before remaining open permanently.

2.3.3 Sectionalizers

Sectionalizers work in conjunction with a recloser located upstream and monitor the fault current when the recloser operates. If the fault is still not cleared when the recloser attempts to re-energize the circuit the sectionalizer will operate when the recloser is open circuit, isolating a portion of the network so when the recloser attempts to re-energize the circuit again the fault will have been isolated by the sectionalizer.

A sectionalizer is self contained and consists of a breaker (that is not rated to interrupt a fault current, as it only operates when the recloser upstream has already disconnected the circuit) and a control interface that monitors the current flow.

2.3.4 Overcurrent Relays

Overcurrent relays are microprocessor based and are the most expensive option for protection in a distribution network. They operate by digitally sampling the current waveforms from a current transformer and then filtering the signal to extract the fundamental phasors. The positive, negative and zero sequence phasors are then calculated and then a decision is made by the relay whether a fault has occurred according to preset values, and what to do about it. Overcurrent relays are connected to a circuit breaker which can be tripped when a fault occurs. There are two basic types of overcurrent relay, instantaneous current and IDMT (Inverse Definite Mean Time Current). Instantaneous overcurrent relays will operate immediately should the current exceed the preset threshold, where as IDMT Current relays require the current to exceed a minimum value for a certain period of time before operating.
Overcurrent relays are currently used predominantly in transmission networks but in the future with the advent of smart grids they are expected to become more prevalent in distribution networks. Their potential for adaptive protection, communication with other protection devices and flexibility allows much more advanced protection schemes and they are the focus of this thesis.

The current state of research on overcurrent relay algorithms is detailed in Section 1.1.

2.3.5 Coordination of Protection

Currently to coordinate protection such as fuses, reclosers, sectionalizers and overcurrent relays in a distribution network one assumption is made, the system is radial [16]. This means that the power flows in only one direction and there is just a single upstream source feeding the distribution network.

To coordinate fuses the minimum melting time of the backup fuse must be greater than the total clearing time of the main fuse separated by the Coordination Time Interval (CTI). The CTI is the time delay between the operation of protection in the current zone and backup zone. This means the backup zone protection will wait for this length of time to allow the current zone protection to operate, if this does now occur the backup zone protection will operate instead. The CTI is the sum of the relay detection time, the relay pick up time, breaker operating time and the margin of error. It is typically in the range of 0.3 seconds. [17]

Reclosers normally coordinate with fuses in a distribution network and will act first to isolate the fault and then try to reconnect it, with the fuses themselves only blowing for permanent faults so the least disruption for the customer occurs.

In a distribution network, protection is coordinated in the following way. When a fault occurs, the recloser operates first, opening a breaker for a short period of time, then reclosing it to clear any temporary faults. This can happen multiple times depending on the configuration. If the recloser fails to clear the fault, an optional sectionalizer will have been monitoring the fault current and the recloser operation, and will operate further downstream when the recloser has opened a breaker, isolating the portion of the network that has the fault. The recloser will then close again, restoring power to
unaffected portions of the network. If the recloser/sectionalizer combination has failed to clear the fault, fuses will then operate according to their coordination settings.

2.4 Future Developments

2.4.1 Smart Grids

Smart grids [18] are a new initiative to modernise electricity networks. They seek to apply technology, tools and techniques to enable the grid to work more efficiently. Future smart grids incorporate features such as automation, communication, distributed generation, distributed storage and advanced metering.

A key part of the smart grid is communication. Smart grids will use communication schemes such as IEC61850 [19] extensively to allow communication between all devices on the network, not just between two protection devices within a substation. IEC61850 is an open communications standard based on the ethernet standard, and can operate over common twisted pair CAT5 cable or optical fibre. The ability to operate over optical fibre is an advantage in locations such as substations where electromagnetic interference and electrical isolation can be issues.

Currently, due to lack of communications in distribution networks, often the only way a utility knows if there is a fault is if a customer calls to report it. Smart grid seeks to change this and will automatically detect and identify faults on the network.

Communication schemes will also assist in allowing new features such as self healing of the network, where protection not only detects the fault and isolates it, but can then re-route power from another part of the network by communicating with other devices. The integration of Distributed Generation into the distribution network in conjunction with the new communication schemes will also give more options for sourcing power should a fault occur, as it is expected that the distributed generation will also be connected to the communication network and will allow control of its output to a certain extent. It will also enable planned islanding which will operate seamlessly with the rest of the grid. Storage devices will also be distributed around the network and improve power quality and reduce peak loading and will also be connected to the communication network [20].
Smart metering is another part of the smart grid initiative, and a more visible part for consumers. It will allow consumers to monitor their power usage in real time, and adjust their power consumption to take advantage of cheaper power at times of low demand, and reduce their power usage at times of peak demand. This could be done automatically or manually. This could also integrate with existing load shedding schemes in use today such as the ripple control by the distribution company of hot water cylinders [21]. This smart metering could also be integrated with the customers distributed generation so as well as reducing their power consumption, they would also supply power to the network at times of peak demand.

From this it is clear that future smart grids offer a lot of potential to create a more robust, smarter distribution network.

2.4.2 Islanding

One of the new scenarios that introducing distributed generation (DG) into the distribution network brings is islanding. Islanding can be either be desired or undesired in a distribution network, but either way it creates new challenges for protection.

Islanding occurs when a distribution network has incorporated DG and a fault upstream causes the source from the transmission network via the substation to be disconnected while the DG remains connected [22, 23]. The advantage of this is that the DG is still connected and supplying power, so could continue to maintain the power supply to at least a portion of the isolated distribution network. This would be an advantage where good security of supply is desired at critical locations such as hospital and airports. In the future it is expected there will be more demand for islanding, for example where a community operated a local renewable power plant (such as solar, wind or hydro) that could supply its energy requirements, but still desired the backup of the main grid for when the sun was not shining, or there was a drought. In this case if there were to be a failure upstream the community could continue to use power supplied by its local plant until the upstream source was restored. When islanding is desired and designed for, the resulting ‘island’ can also be known as a micro-grid.

The disadvantages of allowing the DG to remain in the system include maintaining power quality, protection and resynchronisation. The DG source may not be capable of
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supplying the load or maintaining the voltage and frequency by itself to this new ‘weak’ network. Also the dynamics of the network change with regards to power flow and fault current so the protection must adapt to compensate for this. This means there must be communication in place between the protection devices and the substation and other parts of the network so the protection devices can adapt and adjust their settings in the event of a fault upstream.

When the fault is cleared upstream resynchronisation is also an issue, the phase of the DG must be resynchronised with the transmission network before reconnecting otherwise serious damage could result. Communication and coordination between protection could solve this problem, once again an adaptive protection scheme would be required when the reconnection is complete.

At the present time islanding is not permitted by distribution networks in most cases due to the above disadvantages. When a fault occurs upstream the DG is required to disconnect and shut down until the fault is cleared, then the DG is resynchronised and reconnected to the grid.

2.4.3 Distributed Generation

Distribution generation (DG) sources are generally defined as typically small sources (<10MW) that are connected to the distribution network. Traditionally the electricity network is supplied by large sources (for example hydro dams, thermal plants) located far from loads that are connected to the high voltage transmission network. In contrast a DG source is usually located close to its load and only supplies a small area.

Integration of DG is a new challenge facing the protection of the traditional, radial design of distribution networks [24–26]. Traditionally distribution networks have been protected using time delay fuses (I^2t tripping time), where the ends of the nodes have a minimal time delay, which then increases as the closer the device is to the substation supplying the feeder to ensure only the fuse directly upstream of the fault trips. This means that a fault close the substation would have the largest delay before the protection is activated. However if a fault occurs at the end of the node, the protection there should activate, and other protection which also sees the fault should not as by the time its
time delay has expired, the fault has been isolated from the system, thereby limiting the outage to the affected area only.

The addition of DG will have a large effect on the protection of distribution networks. This is expected to occur because distribution networks rely on the fact that power only ever flows in one direction, and predominantly use fuses for protection coordinated by time delays. For DG protection also needs to be adaptive, as the power flow direction can vary depending on how much power the DG source is producing so overcurrent relays will be required instead of fuses.

2.4.4 Adaptive Protection

Adaptive protection is defined as protection in which the protection scheme is not in a fixed state, but can adapt and adjust its settings to suit a more dynamic network where generators, lines and loads can vary dramatically, changing the network characteristics.

With the advent of future smart grids, the fact that communications will not only exist within substations, but will span the entire network will allow adaptive protection to become more prevalent. A opportunity for adaptive protection is expected to occur where the network is dynamic, where not just the loads are changing, but the sources also. This is likely to occur on future distribution networks where there may be many DG sources connected with unpredictable outputs (for example wind turbines), so the direction of power flow could change often throughout the network depending on their output. When this occurs the protection settings will be required to adapt to the change in the network characteristics, and communications (based on schemes such as IEC61850) between the sources and the protection devices will allow this. It is likely that some of these distribution networks will also be able to exist in ‘islanded’ mode in the case of a fault so the protection devices will also need to adapt to this.
2.5 Simulations

2.5.1 Modelling of Feeder

To research the effects on protection schemes when introducing DG into an existing
distribution network a feeder based on the standard IEEE 13 Bus Feeder [16] was mod-
elled in PSCAD. PSCAD was chosen for this task as it is a time domain simulation tool
that is ideal for simulating transients in networks so will show fault waveforms that are
representative of those expected in reality. [27]

The parameters of the IEEE 13 Bus Feeder are supplied in Appendix A. A network
diagram of the IEEE 13 Bus Feeder is shown in Figure 2.1. It was decided to use
the IEEE 13 Bus feeder as it is smaller than the other models so can better determine
which parameters are having an effect on the fault characteristics but yet is large enough
to contain the common elements present in a distribution network. Its characteristics
include [16]

- Short and relatively highly loaded for a 4.16 kV feeder
- One substation voltage regulator consisting of three single-phase units connected
  in wye (auto tap transformer)
- Lines with variety of phasing
- Shunt capacitor banks
- In-line transformer
- Unbalanced spot and distributed loads

The IEEE 13 Bus test feeder specifications do not include overcurrent protective device
settings so those were calculated based on standard procedures. Given it is a relatively
small feeder it is assumed that it is protected by a single recloser located at the sub-
station labelled 632 in Figure 2.1 and fuses located at junctions throughout the feeder.
Coordination was set so in the event of a fault the recloser would operate first, and, if
it failed to clear the fault after opening twice the appropriate fuse will blow. The fuses
were set so the fuses at the tip off the feeder closest the end loads had a minimal time
delay, just enough to allow the upstream recloser to operate. The next fuse upstream of
the first fuse had a time delay set 0.3 seconds (18 cycles) after the first fuse, to provide
backup protection. This delay was based on a normal delay time. [17]

2.5.1.1 Modelling

As the source located at 650 in Figure 2.1 and corresponding regulator are the connection
to the transmission network via the substation they were modelled as an infinite voltage
source with output voltage set to 115V and a Delta-Y transformer stepping down 115kV
to 4.16kV as per the parameters listed in Table A.5 in Appendix A. The base MVA was
set to 100MVA.

A transformer is used in the feeder between nodes 633 and 634 as shown in Figure 2.1.
This was modelled as a Y-Y transformer stepping down 4.16kV to 0.48kV with a 500kVA
rating.

The distribution lines were modelled by directly specifying the x and y position relative
to the tower of each phase for each spacing configuration from Table A.1. The length of
each distribution line was then set individually using the data in Table A.2.
The loads were modelled as single phase fixed loads with the corresponding rated real and reactive power set from the specified data in Tables A.6 and A.7.

Reactive compensation were modelled as a three phase capacitive loads using the data supplied in Table A.4.

To simulate the addition of DG to the network a second 1MVA source was added and directly connected to the network via a short distribution line to point marked 632 on Figure 2.1. The resulting PSCAD model is shown in Figure 2.2. To simulate a fault on the network a timed breaker was connected at the point which was determined to cause the worst case for fault currents, the point directly between the two sources at 632. The breaker was configured to cause, line to ground, line to line and, with the addition of a second breaker, double line to ground faults via a configurable fault impedance.

Figure 2.2: Simulated 13 Bus Feeder with DG shown in PSCAD
2.5.2 Results of Simulations

After simulating the distribution network it was observed that the fault waveforms contained a significant amount of decaying DC Offset. With the advent of Smart Grids and the expected increased use of overcurrent relays in future distribution networks as detailed in the previous section, this is a potential issue. Overcurrent relay algorithms for phasor estimation can be susceptible to decaying DC offsets and this is an active area of research [3–7], as was detailed in Section 1.1. It was also observed that with DG connected, the level of decaying DC offset present increased and it was more widespread on the network so the factors which affect this portion of the fault current waveform were investigated further.

2.5.2.1 Effect of fault type and load imbalance

As the IEEE 13 bus feeder is quite unbalanced in terms of the load on each phase, various fault types were simulated. Line to line, single line to ground, double line to ground and three line to ground faults were all compared. Single line to ground faults were also compared for all three phases.

The results are shown in Figure 2.3 for the single and double line to ground faults, and Figure 2.4 for the line to line faults. From these it was determined that a single line to ground fault occurring on phase B presented the worst case scenario so it was decided to simulate just this type of fault for the further simulations.
Figure 2.3: Effect of Single and Double Line to Ground Faults

Figure 2.4: Effect of Line to Line and Single Line to Ground Faults
To determine the effect on the fault current a portion of the load was disconnected from the feeder. The load was disconnected by removing the distribution line between 632 and 671, in simulation of a fault where a fuse located next to the distribution line would blow in response to a fault. This meant that the loads on each phase were reduced considerably to those shown in Table 2.1. A fault was then simulated by activating the breaker connected to the point of 632 in Figure 2.1 for a single line to ground fault on phase B. Another simulation was also performed, for the case of no load connected. The effect on the fault current is shown in Figure 2.5 for phase B. It shows that as the load is reduced there is only a small effect on the fault current, and the peak is reduced as the loading on the network is reduced.

<table>
<thead>
<tr>
<th>Phase</th>
<th>Real Power</th>
<th>Reduction</th>
<th>Reactive Power</th>
<th>Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>One</td>
<td>160kW</td>
<td>(14%)</td>
<td>110kVAR</td>
<td>(18%)</td>
</tr>
<tr>
<td>Two</td>
<td>520kW</td>
<td>(53%)</td>
<td>347kVAR</td>
<td>(55%)</td>
</tr>
<tr>
<td>Three</td>
<td>120kW</td>
<td>(11%)</td>
<td>90kVAR</td>
<td>(12%)</td>
</tr>
</tbody>
</table>
2.5.2.3 Impact of instant of fault initiation

The purpose of this test is to find the phase offset which gives the worst case of decaying DC offset. The effect is shown in Figure 2.6 and shows that while the phase instant when the fault occurs is not something that is able to be controlled in practise, it has a large effect on the output so when performing simulations to generate accurate realistic results the value of this needs to be taken into account.

The simulations show that the level of decaying DC offset is significantly affected by the phase offset at the time of the fault. The worst case occurs when the fault occurs at the moment where the sinusoidal waveform of the affected phase is at either $\frac{3\pi}{4}$ for the largest positive peak of the decaying DC offset and $\frac{3\pi}{2}$ for the largest negative peak.

![Figure 2.6: Effect of phase offset value when fault occurs](image)

2.5.2.4 Change in Fault Impedance

Varying the level of fault impedance was simulated by inserting a resistor in series with the fault to ground. This effect is shown in Figure 2.7 where, as the resistance is increased, it reduces the peak of the DC offset considerably to a point where, with a phase to ground fault resistance of 10Ω, there is negligible DC Offset present in the fault signal.
2.5.2.5 Series Impedance between sources

In order to determine what effect the length of distribution line has on the decaying DC offset, the distribution line length connecting the substation to the network was varied, in order to simulate the DG being closer to the loads than the substation.

As a variant on this, the location of the fault was also altered to see the effect on the decaying DC offset. It can be seen that the further from the source and the more series impedance between the source and the fault the less the decaying DC offset. This has significance for distribution networks integrating DG, as it can be expected that...
should a fault occur close to a DG source, even though there is a high series impedance between the main source from the transmission network, the level of decaying DC offset is expected to be significant.

2.5.3 The IEEE 34 Bus Feeder

In order to verify the results from simulating the IEEE 13 Bus Feeder a pre-existing, tested model of the standard IEEE 34 Bus Feeder was obtained that had been verified against the published load-flow study for the feeder [28]. The model comes with two versions, one matching the standard IEEE 34 bus feeder, the other has been modified and two DG sources have been attached. The DG sources are 660kVA wind turbines modelled as wound rotor induction machines. The DG sources are attached at nodes 848 and 890 shown in the model in Figure 2.10.

The IEEE 34 Bus Feeder differs from the 13 Bus Feeder in the following ways,

- lightly loaded
- larger network
- multiple voltage regulators
- two DG sources located at the ends of nodes modelled as wind induction generators.
This feeder was then used to verify the tested results from the 13 bus feeder. A line to ground fault was simulated at node 834 starting at time 4.1 seconds and the current waveform as would be seen by a protection device connected between nodes 842 and 834 was obtained. The resulting waveform is shown in Figure 2.11 along with the waveform from the same fault on the original IEEE 34 bus feeder. It shows that with DG present, the fault waveforms changed dramatically with higher levels of decaying DC offset present during faults on portions of the network where there was no significant levels before. It was also observed that, depending on the fault location, changes in direction of current flow occurred during the fault as the fault is supplied by the DG sources from the other direction.

This means that existing protection schemes depending on single direction current flow to determine protection zones would need to be redesigned. Any protection scheme would need to adapt, possibly in realtime depending on the participation of the DG in the network and whether intentional islanding would be permitted. [29]
2.6 Discussion

The distribution network was investigated in terms of its topology, protection devices and protection schemes which are currently implemented and new advances such as smart grids, distributed generation and the challenges and opportunities this will create in the distribution network were investigated. It was shown that future distribution networks are likely to include significant DG sources and other aspects of the smart grid initiative such as more advanced communications using standards such as IEC61850. This will require changes to the traditional method of protecting distribution networks and fuses are likely to be required to be replaced by overcurrent relays in many areas but this will also create new opportunities for more effective protection schemes.

From simulations of a distribution feeder it was determined that the decaying DC offset is a significant component in the fault waveforms when DG was added to a distribution network. From the results of varying the fault impedance and the distribution line impedance it is clear that the level of the decaying DC offset is affected by the series impedance between the source and fault to ground. The relationship is defined by (2.1). The series impedance $Z_s$ consists of the sum of the impedance of the source, the total impedance of the distribution line and the fault impedance as shown in (2.2).
Chapter 2. The Distribution Network

\[ DC_{\text{peak}} \propto \frac{1}{Z_s} \] (2.1)

where

\[ Z_s = Z_{\text{source}} + Z_{\text{line}} + Z_{\text{fault}} \] (2.2)

The instant in which the fault occurs also has a large effect on the peak level of the decaying DC offset in the fault current waveform with the highest peaks occurring at a phase offset of \( \frac{3\pi}{4} \) and \( \frac{3\pi}{2} \). Changes in the loads connected to the feeder were shown to have little effect on the level of decaying DC offset in the fault current.

In current distribution networks the protection is not required to act quickly, with coordination delays of approximately 0.3 seconds (15-18 cycles) common between fuses [17]. This means that extensive filtering such as bandpass filtering and mimic filters can be implemented to remove the decaying DC offset as the additional time delay it causes will not be a problem.

With increased penetration of DG being connected to the grid (and more forecast to be connected in the future) there is expected to be a requirement for faster acting protection. This is because the DG is likely to become a larger portion of the electricity supply for some networks so may be expected to stay connected and ‘ride-through’ minor faults in the same way large generators do today. Protection will need to be fast enough to act quickly in this scenario to protect the DG sources.

The next step is to develop a test platform which can develop, assess and compare protection algorithms against these fault waveforms and determine their suitability for future distribution networks.


Chapter 3

Implementation of Digital Relay

3.1 Introduction

A key part of this Masters research was the development of a testing platform to critically assess and test phasor estimation algorithms in digital relays. This chapter details the design, the hardware implementation and the software implementation of this.

3.2 Phasor Estimation

Digital relays are a critical component in modern protection schemes, they detect faults when they occur and decide what action to take. As protection schemes become more complex older protection devices such fuses and electromechanical relays are being replaced with digital relays.

The main processing task of the relay is *Phasor Estimation*. Once the voltage or current phasors have been calculated the relay can then calculate the positive, negative and zero sequence symmetrical components on which most protection scheme settings are based.

The symmetrical components are the positive, negative and zero sequence components represented by $I_1$, $I_2$ and $I_0$ respectively. They are defined in terms of the phasor currents $I_a$, $I_b$ and $I_c$ in (3.1) using (3.2)
\[
\begin{bmatrix}
  I_a \\
  I_b \\
  I_c
\end{bmatrix} = A 
\begin{bmatrix}
  I_0 \\
  I_1 \\
  I_2
\end{bmatrix}
\]  \quad (3.1)

where \( A \) is defined as

\[
A = \begin{bmatrix}
  1 & 1 & 1 \\
  1 & \alpha^2 & \alpha \\
  1 & \alpha & \alpha^2
\end{bmatrix}
\]  \quad (3.2)

where \( \alpha = 120^\circ \) or \( \frac{2\pi}{3} \) radians

however to generate the sequence components from the phasors we need to use 3.3 with the inverse of \( A \) (3.4)

\[
\begin{bmatrix}
  I_0 \\
  I_1 \\
  I_2
\end{bmatrix} = A^{-1} 
\begin{bmatrix}
  I_a \\
  I_b \\
  I_c
\end{bmatrix}
\]  \quad (3.3)

\[
A^{-1} = \begin{bmatrix}
  1 & 1 & 1 \\
  1 & \alpha & \alpha^2 \\
  1 & \alpha^2 & \alpha
\end{bmatrix}
\]  \quad (3.4)

where \( \alpha = 120^\circ \) or \( \frac{2\pi}{3} \) radians

3.3 Hardware

3.3.1 The Digital Relay Components

The components of a digital relay normally consist of a current/voltage transformer (CT/VT), analogue circuitry to protect and scale the input to a suitable level, an analogue to digital converter, a processor, one or more circuit breaker outputs and a communications interface for configuration and optionally for coordination. The layout of these is shown in the block diagram in Figure 3.1.
3.3.2 Processor

In digital relays the main processor needs to provide the following functions:

- downsampling and filtering of input signals
- phasor estimation
- protection scheme implementation
- communications interface for configuration
- (optional) communications interface for coordination with other relays

As the intended use of a digital relay is in the electricity industry, speed, reliability and accuracy of the processor are a higher priority than cost. Therefore the processor selected should be more than capable of providing the above functions with high accuracy.

A floating point Digital Signal Processor (DSP) was chosen for this application for increased accuracy when comparing the performance of the algorithms and flexibility with testing different wavelets with different decomposition levels using the Discrete Wavelet Transform. The algorithm is also designed to be implemented on a fixed point Digital Signal Processor which would speed up execution time. For this the core of the algorithm would remain the same, the only change required would be the addition
of scaling factors to ensure that the result did not suffer from additional error due to quantization.

The Digital Signal Processor chosen was the ADSP-21369 SHARC Processor [30] incorporated within the Analog Devices ADSP-21369 SHARC EZ-KIT Lite Evaluation Kit shown in Figure 3.2. The ADSP-21369 core clock speed is set to 331.776 MHz. The DSP is connected via the SPI (Serial Peripheral Interface) bus to the Analog Devices AD-1835A Codec which contains the analogue to digital converters (ADCs) for sampling the waveforms.

![Figure 3.2: Circuit board containing ADSP-21369 Digital Signal Processor with AD1835 Analogue Front End](image)

**3.3.3 Analogue to Digital Converter**

As the Digital Signal Processor is digital, it requires a digital representation of the signal before it can perform the estimation of the phasors. This is provided by the analogue to digital converters (ADCs). The analogue to digital converters should be capable of sampling higher than the Nyquist rate of the frequencies we are interested in, in this case the fundamental 50/60Hz and its harmonics. The Analog Devices AD1835 codec was selected which is capable of sampling at a rate of 48kHz with an input voltage range of 5.0 Volts. As the sampling rate of 48kHz is much higher than required digital FIR
filters were implemented and the signal was then decimated to provide a lower sampling rate for the phasor estimation algorithms.

The DSP is connected via the I²S (Integrated Interchip Sound) and the SPI (Serial Peripheral Interface) bus to the Analog Devices AD-1835A Codec. The I²S bus carries the audio stream and the SPI bus is used for configuration of the codec.

### 3.3.4 Analogue Electronics

As most analogue to digital converters are limited in terms of the input voltage and frequency, they require external components to protect them, to scale the voltage to a usable level and provide anti-aliasing filtering. For use in the lab the voltage scaling was provided by external means as detailed in Section 4.3 so a simple circuit consisting of a single pole low pass filter and Schottky diodes to limit the input voltage to the ADC to between -0.3 Volts and 5.3 Volts was implemented as shown in Figure 3.3. As the ADC used was differential input but the analogue circuitry is single ended, the resolution of the codec was limited to 23 bit instead of 24 bit, but as the signal is being oversampled by a large amount and is expected to be decimated this is not a problem.

![Figure 3.3: ADC analogue electronics](image)

**Figure 3.3: ADC analogue electronics**
3.3.5 Communications Interface

Digital relays normally contain a communication interface, both to provide a means of configuring the protection scheme in the relay and optionally a means of coordinating with other protection devices. The communication interface for configuration is often based on the RS-485 serial interface although more in more recent relays this can also be provided by an ethernet and TCP/IP based interface.

Coordination between relays can be implemented using a variety of interfaces such as twisted pair, microwave or fibre optic. In the future this is expected to be implemented using more open protocols such as IEC61850.

In this case communication was provided by a USB connection built into the development board based on the JTAG interface. A possible direction for future research is to expand this to include an Ethernet interface based on the IEC61850 [19] communications standard.
3.4 Software

The design of the software inside the Digital Signal Processor is shown in the block diagram in Figure 3.4. The analogue waveform from the CT or VT is sampled using the analogue to digital converter (ADC) and then passed through a multistage down-sampling filter to decimate the signal. This decimation reduces the computing resources required while still providing an accurate representation of the parts of the signal we are interested in for the phasor estimation algorithms. After the decimation the same signal is processed independently by both the phasor estimation using the Discrete Fourier Transform and the phasor estimation using the Discrete Wavelet Transform algorithms, each estimating a different value of the phasor which can be compared to compare the performance of the algorithms. The sections below explain in detail the algorithms contained within each block.

Figure 3.4: Software Block Diagram
3.4.1 Downsampling using Digital Filter and Decimation

As an audio codec (ADC) was used, the sampling rate was set relatively high for this application at 48kHz with 24 bit resolution. A limitation of the analogue circuitry used reduces this to 48kHz at 23 bit resolution. As the signals we are interested in are the 50Hz fundamental and its harmonics and the DFT and DWT algorithms are processor intensive at high sampling rates downsampling was implemented. In this process we also increase the resolution from 24 bit to 32 bit.

The choice of the new sampling frequency is not arbitrary, certain conditions must be meet in order for both the DFT and the DWT to work effectively.

The first requirement is computational efficiency, the new rate must be low enough that excess computation is not required but still high enough that it contains all the frequencies that we are interested in. It was decided that 400Hz (the 8th harmonic of the fundamental frequency of 50Hz) would be the highest frequency, so a sampling rate of at least 800Hz would be required in order to meet the Nyquist criteria. This defines the passband frequency of the downsampling filter.

The second requirement is from the characteristics of DFT algorithm. The DFT divides the frequency spectrum up into ‘bins’ and in order to obtain an accurate phasor it is desired that the fundamental frequency falls in the centre of one of these ‘bins’. The number of these ‘bins’ is determined by the number of ‘points’ of the DFT. In this case we use a 512 point FFT, so the 50Hz fundamental must fall into a multiple of this as shown in Equation 3.5 where $f_1$ is the fundamental frequency, in this case 50Hz, $F_s$ is the sampling frequency and $N$ is the number of points of the FFT.

$$\text{Bin Number} = \frac{f_1 \times N}{F_s} \quad (3.5)$$

A third requirement was that the downsampling decimation rate should be an integer multiple of the original sampling frequency for ease of implementation.

From these requirements we have two possible sampling rates, 1.6kHz and 3.2kHz. Out of those, 1.6kHz would require downsampling by 30, whereas as 3.2kHz only by 15, a lot simpler in terms of the filter length and computations required. The equiripple
filter design technique was used with MATLAB filter design tool (fdatool) [31] using the parameters shown in Table 3.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Passband Attenuation</td>
<td>1dB</td>
</tr>
<tr>
<td>Stopband Attenuation</td>
<td>80dB</td>
</tr>
<tr>
<td>Passband Frequency</td>
<td>800Hz</td>
</tr>
<tr>
<td>Stopband Frequency</td>
<td>$\frac{F_s}{2}$</td>
</tr>
</tbody>
</table>

Downsampling consists of both filtering (with a low pass filter with cutoff frequency less than the Nyquist frequency of the new sampling rate) and decimation. Downsampling from 48kHz to 3.2kHz could be completed in a single pass, however to achieve the filtering requirements a filter of size 151 would be required. So instead multistage downsampling options were investigated to determine the optimal solution. Using multistage downsampling means that the filter requirements for each stage are relaxed, specifically the stopband frequency only needs to be at the Nyquist frequency for that sampling rate for the first stage which reduces the filter size, and for subsequent stages the input sampling rate is reduced so the number of computations required is much less. The characteristics of each of these options and the filter size required for each is shown in Table 3.2.

<table>
<thead>
<tr>
<th>Option</th>
<th>Original Rate</th>
<th>New Rate</th>
<th>Decimation Factor</th>
<th>Filter Order</th>
</tr>
</thead>
<tbody>
<tr>
<td>One</td>
<td>48kHz</td>
<td>3.2kHz</td>
<td>15</td>
<td>151</td>
</tr>
<tr>
<td></td>
<td>48kHz</td>
<td>9.6kHz</td>
<td>5</td>
<td>29</td>
</tr>
<tr>
<td>Two</td>
<td>48kHz</td>
<td>3.2kHz</td>
<td>3</td>
<td>29</td>
</tr>
<tr>
<td>Three</td>
<td>48kHz</td>
<td>16kHz</td>
<td>3</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>16kHz</td>
<td>3.2kHz</td>
<td>5</td>
<td>49</td>
</tr>
</tbody>
</table>

The following equations (3.6)(3.7) [32] detail a method of quantifying the computational effort of each option for downsampling so the optimal method can be selected.

$$\text{Multiplications Per Second} = \sum_{i=1}^{I} N_i F_i$$ (3.6)
Total Storage Requirements = \sum_{i=1}^{I} N_i \tag{3.7}

where \(N_i\) is the number of filter coefficients in stage \(i\) and \(F_i\) is the resultant sampling frequency of the filter stage \(i\).

Table 3.3 shows the cost of each of the options in both computations and storage space. It shows that using the two stage Option One requires 79% of the computations and 39% of the storage space of Option Three with a single downsampling stage. Option Two also requires less computations than Option Three but Option One has a clear advantage in terms of computations with only 7% more storage space required and therefore was selected as the optimal solution to implement.

**Table 3.3: Downsampling Options Requirements**

<table>
<thead>
<tr>
<th>Option</th>
<th>Multiplications Per Second</th>
<th>Total Storage Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>One</td>
<td>384000</td>
<td>60</td>
</tr>
<tr>
<td>Two</td>
<td>416000</td>
<td>56</td>
</tr>
<tr>
<td>Three</td>
<td>486400</td>
<td>152</td>
</tr>
</tbody>
</table>

The magnitude responses of the first stage and second stage downsampling filters are shown in Figure 3.5 and Figure 3.6. It can be seen that the cutoff frequency of the first stage is 4.8kHz, and the second stage cutoff is 1.6kHz.

![First stage downsampling filter frequency response](image)
3.4.2 Phasor Estimation using the Discrete Fourier Transform

The Discrete Fourier Transform (DFT) is widely used in digital relays at present and is based on the standard equation of the Fourier Transform shown in (3.8). [33] The Fourier Transform represents a waveform as an infinite series of sine waves of varying amplitude at frequencies from DC up to the Nyquist limit set by the sampling rate. In practice however the number of sine waves is set by the size of the Discrete Fourier Transform performed. The Discrete Fourier Transform effectively transforms data between the time and frequency domains.

For phasor estimation, where the fundamental frequency of waveform is represented as a phasor with a magnitude component and a phase component, the Fourier Transform can be used to directly calculate the phasor components and filter out the DC component, harmonics and other unwanted noise.

\[
S(n) = \frac{2}{N} \sum_{n=0}^{N-1} s(n)e^{-j\omega t_n} \tag{3.8}
\]

where \( s \) is the sampled signal and \( N \) is the size of the DFT.

3.4.2.1 Implementation

To implement the Discrete Fourier Transform (DFT) a more efficient algorithm designed for embedded applications known as the Fast Fourier Transform (FFT) was used. Digital
Signal Processors are normally supplied with signal processing libraries which contain an optimized implementation of the FFT and this was used to implement the DFT in this case.

A Discrete Fourier Transform (DFT) of the array $s$ containing a window of the latest samples from the ADC is performed as shown in (3.9)

$$S = FFT(s)$$  \hspace{1cm} (3.9)

The frequency bin $M$ is then selected based on the sampling frequency, reference frequency and the size of the FFT as shown in (3.10)

$$M = \frac{f_r \cdot \text{sizeFFT}}{f_s}$$  \hspace{1cm} (3.10)

The magnitude and phase are then calculated by (3.11) and (3.12)

$$\text{Magnitude} = \sqrt{S_r^2(M) + S_i^2(M)}$$  \hspace{1cm} (3.11)

$$\text{Phase} = \arctan \left( \frac{S_i(M)}{S_r(M)} \right)$$  \hspace{1cm} (3.12)

This gives the magnitude and phase angle of one phase at one point in time, the process is then repeated for all other current and voltage phases.

### 3.4.3 Phasor Estimation using the Discrete Wavelet Transform

Unlike the Discrete Fourier Transform, phasor estimation with the Discrete Wavelet Transform (DWT) does not generate the magnitude and phase values directly as the DWT does not transform directly between the Time and Frequency domains. The DWT does however have the advantage of time resolution as well as frequency resolution as it represents the signal as a series of wavelets.
The ‘Wavelet’ domain is orthogonal however so the DWT of the sampled waveform can be compared with the DWT of a known reference waveform to find the magnitude and phase.

The Discrete Wavelet Transform (DWT) \[34, 35\] is based on the equation (3.13)

\[
DWT(m,k) = \frac{1}{\sqrt{a_0^m}} \sum_{n=0}^{N-1} s(n) \Psi \left( \frac{k - na_0^n}{a_m} \right)
\]  

(3.13)

where \( \Psi(n) \) is the ‘mother wavelet’ of which there is an infinite number of possible wavelets that can be used, for example the Daubechies wavelets as mentioned by Osman and Malik. \[9\]

The mother wavelet \( \Psi(n) \) must have the two properties listed in equations (3.14) and (3.15)

The first property (3.14) states that the wavelet must have an average value of zero, the second property (3.15) states that the square norm must be one.

\[
\int_{-\infty}^{\infty} \Psi(t) dt = 0
\]  

(3.14)

\[
\int_{-\infty}^{\infty} \Psi^2(t) dt = 1
\]  

(3.15)

It was decided to evaluate the Discrete Wavelet Transform with the Haar and Daubechies series of wavelets as they are recommended \[10\] and are the most commonly used wavelets. There is potential for future research to evaluate other mother wavelets for their potential for phasor estimation.

3.4.3.1 Implementation

The algorithm to perform phasor estimation using the Discrete Wavelet Transform is detailed as follows.
The Discrete Wavelet Transform (DWT) of the array $s$ containing a window of the latest samples from the ADC is performed as shown in (3.16). The algorithm for the Discrete Wavelet Transform itself is detailed in Section 3.4.4.

$$S = DWT(s) \tag{3.16}$$

To calculate the phase a reference signal $r_1$ is generated to be compared with the sampled signal as in (3.17)

$$r_1 = \sum_{n=0}^{N} \sin \left(2\pi \frac{f_r}{f_s} n \right) \tag{3.17}$$

where $f_r = \text{reference frequency (eg 50Hz)}$

and $f_s = \text{sampling rate (eg. 3.2kHz)}$

and $N = \text{number of samples}$

The Discrete Wavelet Transform of $r_1$ is then calculated in (3.18) and the phase angle between $r_1$ and $s$ is then calculated in (3.19) using the *inner (dot) product*.

$$R_1 = DWT(r_1) \tag{3.18}$$

$$\theta_1 = \arccos \left(\frac{R_1 \cdot S_1}{|R_1||S_1|}\right) \tag{3.19}$$

Due to the properties of the dot product, (3.19) only gives a value of $\theta_1$ between $0$ and $\pi$. This means that if $\theta > \pi$ the result from (3.19) will give a value of $\theta_1$ which will be indistinguishable from a value of $\theta_1$ if $\theta < \pi$. This is shown in Figure 3.7.

To solve this problem another reference waveform $r_2$ is calculated in (3.20) to determine the correction to apply to $\theta_1$ to get the true value of $\theta$. The waveform has an offset of $\frac{\pi}{2}$.

$$r_2 = \sum_{n=0}^{N} \sin \left(2\pi \frac{f_r}{f_s} n + \frac{\pi}{2} \right) \tag{3.20}$$
\[ R_2 = DWT(r_2) \] (3.21)

\[ \theta_2 = \arccos \left( \frac{R_2 S_1}{|R_2||S_1|} \right) \] (3.22)

Using the result \( \theta_2 \) from (3.22), Figure 3.8 shows that a simple logic test (3.23) can then be performed to calculate the absolute value of the phase \( \theta \).

\[ \text{If } \theta_2 > \frac{\pi}{2} \text{ then } \theta = 2\pi - \theta_1, \text{ Else } \theta = \theta_1 \] (3.23)

Now that the phase \( \theta \) is calculated, the magnitude is calculated by generating a third reference waveform (3.24) with phase equal to the sampled waveform and performing the DWT on it (3.25). The magnitude is then determined using the ratio of the norms of \( S \) and \( R_3 \) as shown in (3.26).

\[ r_3 = \sum_{n=0}^{N} \sin \left( 2\pi \frac{f_r}{f_s} n + \theta \right) \] (3.24)
\[ R_3 = DWT(r_3) \] (3.25)

\[ \text{Magnitude} = \frac{|S|}{R_3} \] (3.26)

This gives the magnitude and phase angle of one phase at one point in time, the process is then repeated for all other current and voltage phases.

### 3.4.4 Implementation of the Discrete Wavelet Transform (DWT) Algorithm

This section describes the implementation of the Discrete Wavelet Transform (DWT) Algorithm itself which is used in the previous section for Phasor Estimation.

To give maximum flexibility the Discrete Wavelet Transform was implemented using the filter method [36] which uses a pair of quadrature mirror filters. This allows for testing of different wavelet sizes and types and use of the optimized FIR filter library functions supplied with the DSP.

A table of the orthogonal Daubechies filter coefficients contained in Appendix B was used for the filters obtained from [36]. The values in the table are the approximation coefficients, to get the detail coefficients the order is reversed and the sign of every second coefficient is inverted. The wavelets tested were Haar (a special case of the Daubechies Wavelet), Daubechies 4, Daubechies 8 and Daubechies 10.

Wraparound was added before and after the signal to be transformed to ensure the end values would be accurate. This is shown in (3.27) in MATLAB notation of the 64 sample input signal \( s \) using the Daubechies 4 wavelet. The wraparound is set to the same size as the number of filter coefficients so the total size of the data to be transformed is 72 values.

\[ [s(60:63)][s][s(0:3)] \] (3.27)
The FIR filter (Convolution) and Decimation function (3.28) from the DSP library was then used to convolve the array of filter coefficients with the signal array \( s \) with added wraparound (3.27) and decimate by two (as the frequency band contained in the signal has been halved) in one step. The wraparound (now 2 samples on each end of the data array) was then removed to get the result.

\[
y(i) = \sum_{j=0}^{k-1} x(i \cdot l - j) \cdot h(k - l - j) \quad (3.28)
\]

where \( i = 0...\text{numOutputSamples}-1 \)
and \( h \) = array of filter coefficients
and \( k \) = number of filter coefficients
and \( l \) = decimation level

The DWT can be performed also more than once (recursively) on the same input values, each time halving the size of the output and of the frequency band it filters. This effect is shown in Figure 3.9 with three levels of recursion. This number of times it is performed is known as the decomposition level. For example, with a sampling rate of 3.2kHz a single level DWT will produce two outputs, the approximation coefficients and the detail coefficients, each covering half the input frequency spectrum. The output after filtering by the detail coefficients cover from 800Hz to 1.6kHz, and output from filtering by the approximation coefficients covers from 0Hz to 800Hz. For a second level DWT the approximation coefficients output from the first level are used as the input and the DWT is performed again, again splitting the input frequency spectrum in two. The frequency bands that result from this are 0 to 400Hz, and 400Hz to 800Hz.

Multiple levels of DWT can provide more filtering of unwanted harmonics and noise before the phase and magnitude are calculated. Wavelets with higher numbers of filter coefficients are required when using multiple level DWT otherwise too much information required for accurate phase and magnitude calculation can be lost. This is one of the reasons Feng and Jeyasurya [10] recommend use of Daubechies 8.
3.4.5 Variation of the Fundamental Frequency

With the Discrete Fourier Transform, care must be taken to select the sampling rate and size of the FFT so that the frequency we are interested in falls exactly into the centre of one of these ‘bins’. If the frequency is off by even a small amount (the frequency of the grid is normally kept within 0.1pu) this will affect the accuracy of the estimated phasor. Depending on the frequency of the grid (50Hz or 60Hz), a different sampling rate may also be required (although this can be modified in software by oversampling with the analogue to digital converter and modifying the decimation rate to obtain the new required sampling rate).

With the Discrete Wavelet Transform, the frequency of the phasor we are estimating is calculated on the fly by generating a sine wave with the matching frequency. This creates an opportunity for use of a Phase Locked Loop (PLL) to calculate the exact frequency of the fundamental and generate a sine wave to match, hereby increasing the accuracy of the Phasor Estimation algorithm. The Discrete Wavelet Transform is not affected by the sampling frequency itself as long as the sampling rate is high enough so the frequencies we are interested in are lower than the Nyquist rate.
Chapter 4

Analysis of Digital Relay Implementation

4.1 Introduction

In the previous chapter a testing platform was designed and implemented in the form of a digital relay. This chapter will use that testing platform in conjunction with the results from Chapter 2 to critically assess and compare the performance of the phasor estimation algorithms in three parts.

The first part assesses the computational requirements and efficiency of the proposed algorithm for phasor estimation using the Discrete Wavelet Transform. The second part then compares the accuracy and performance of the proposed algorithm with the phasor estimation using the Discrete Fourier Transform algorithm using fault waveforms generated in simulations of the distribution feeder as detailed in Chapter 2. The third part compares the phasor estimation algorithms using specific, mathematically generated signals to assess their performance with specific signal components and characteristics that are expected to be present in the signal from a CT/VT during a fault.
4.2 Algorithm Analysis

4.2.1 Breakdown of DWT Phasor Estimation Algorithm

In analysing the parts of the DWT phasor estimation algorithm it was determined that the largest single portion is spent calculating values for the synchronized reference waveform (3.24), a huge 36% as shown in Figure 4.1. This could be reduced considerably by generating a lookup table of the waveform and then ‘shifting’ the wave so its phase matches the sampled waveform phase. This disadvantage of this would be reduced accuracy when calculating the magnitude as the shifted waveform may not be a close enough match to the phase and also there would be increased program memory use. However if this was implemented, the only computational time required for this portion would be to move values from one location in memory to another, so the computational time required for the DWT phasor estimation would be 64% of the current time, so in the case of the Daubechies 8, 1 level, full cycle algorithm in Figure 4.3, this would be 17.5\(\mu s\), instead of the current 27.4\(\mu s\), putting it in the same category as performing a 256 point FFT. The next largest parts are the two DWT’s with 17% each, these are currently implemented using the filter method as described in (3.28). They may be able to be optimized further by using the lifting method as described in [36], but this would remove the flexibility of being able to implement different wavelets. Since this and most other DSPs have optimized instructions for filter coefficient calculation it was not implemented in this case.

![Figure 4.1: Breakdown of DWT Phasor Estimation Algorithm](image-url)
4.2.2 Comparing the DWT with the FFT computation time

Figure 4.2 compares the computation time required for phasor estimation using the Discrete Wavelet Transform with the computation time required for phasor estimation with the Discrete Fourier Transform (implemented using the Fast Fourier Transform algorithm). The wavelets Haar, Daubechies 4, Daubechies 8 and Daubechies 10 are tested with varying sizes of the Fast Fourier Transform. In terms of computational time phasor estimation using the Discrete Wavelet Transform does not require much more processing power, and depending on which size FFT is used may even require less such as in the case of the 512 point (or larger) FFT.

![Figure 4.2: Comparing computation time of the DWT and the FFT - Half cycle](image-url)
4.2.3 Comparing execution time of wavelets

Four different wavelets were tested and implemented using the DWT phasor estimation algorithm, their execution time is compared in Figure 4.3. The difference in execution time is small, with full cycle analysis the variation between Haar (special case of Daubechies 2) and Daubechies 10 is only 17%, and with with half cycle analysis this becomes 28%. This may become more of an issue if the total computation time can be reduced by the method suggested in the DWT phasor estimation algorithm breakdown. As the computation time is under 30µs real time processing can be performed at sampling rates of up to 11kHz when using this processor to calculate all three phases.

Figure 4.3: Comparison of execution time of Wavelets
4.2.4 Comparing execution time of different levels of decomposition of DWT

Recursion was also implemented to add extra levels of decomposition of the DWT to add further filtering as detailed in Section 3.4.4. As shown in Figure 4.4 recursion does not add a significant amount of extra processing time when using the DWT algorithm. This is because the only extra processing required is of the DWT itself, which is shown from the analysis of the algorithm in Section 4.2.1 to only contribute to 11% of the total processing time.

![Figure 4.4: Comparison of execution time of different levels of decomposition - Full cycle](image)

Figure 4.4: Comparison of execution time of different levels of decomposition - Full cycle
4.3 Relay Test Bench Setup

For realtime testing of the phasor estimation algorithms in the implemented digital relay a lab test bench was assembled as shown in Figure 4.5. A block diagram of this system is shown in Figure 4.6 and is described below.

1. A standard IEEE 13 bus distribution feeder is simulated in PSCAD (as described in Chapter 2) and the current waveforms as would be seen by a CT and overcurrent relay located as they would be in an actual feeder are generated. They are captured and stored in the industry standard IEEE COMTRADE [37] file format.

   The COMTRADE file format was chosen as it is the file format used by fault recorders and other protection devices to capture fault waveforms on electricity networks and was designed specifically for this purpose. This will also allow an opportunity for future research to test the performance of relay algorithms using fault signals captured directly during faults on electricity networks.

2. LabView [38] based software developed for numerical testing of digital relays as a 2009 Honours project [39] is used to load the COMTRADE files, then generate the analogue waveforms using a National Instruments NI 9263 Analog Output Module [40]. The testing hardware is shown in Figure 4.5.

3. The implemented Digital Relay samples the waveform using its analogue to digital converter. The sampled waveform is then processed by the algorithms under test to estimate the current phasors.

4. The estimated current phasors are then communicated back from the DSP to the PC for analysis using the JTAG interface.
Figure 4.5: Relay Test Bench Hardware

Figure 4.6: Realtime Testing Setup Block Diagram
4.3.1 Results of testing with simulated waveforms

The first test performed was the case of the double line to ground fault (phases A and B) from Figure 2.3 in Section 2.5.2.1. This was chosen as it presented the worst case of likely faults with the highest level of decaying DC offset in the IEEE 13 bus feeder. The result of this using the full cycle implementation is shown in Figure 4.7 and from this we can see that Discrete Fourier Transform is able to estimate the phasor accurately, with the phasor estimation using the Discrete Wavelet Transform overshooting by a factor of 12% due to the decaying DC offset present at the moment of the fault. As this is a full cycle implementation the DFT is able to remove the majority of the decaying DC. It was also observed from this test that some high frequency noise remains in the signal with a small oscillation occurring throughout the time period showing that more filtering may be required.

The result of this using the half cycle implementation is shown in Figure 4.8 and shows that with the harmonics and decaying DC offset present in the waveform neither the DFT nor the DWT can estimate the phasor accurately from the raw waveform, both oscillate significantly around the value.

To attempt to remove the high frequency oscillations present in the estimated phasors a higher decomposition level was used for the DWT, the result of which is shown in Figure 4.9. It shows that the higher level of decomposition had no significant effect on the oscillations, but it did introduce a larger error in the phasor estimation.

When calibrating the test setup, specifically the 0.0 Volt point it was also noted that any DC offset at all caused significant errors in the phasor estimation when using the DWT, whereas the DFT was able to filtering out any constant DC offset. This meant the DFT effectively required no calibration for the 0.0 Volts point, whereas the DWT would need to be carefully calibrated and the calibration would need to be maintained, or the signal would need to be pre-filtered to remove any DC offset.
Figure 4.7: Comparison of DFT and DWT during Double Line to Ground Fault - Full cycle

Figure 4.8: Comparison of DFT and DWT during Double Line to Ground Fault - Half cycle
A test was also performed to determine the performance of the phasor estimation algorithms with a signal not containing any significant decaying DC offset, in this case the waveform was from a simulated fault with a higher fault impedance of 1Ω from Section 2.5.2.4. With the full cycle implementation both the DFT and the DWT algorithms were able to estimate the phasors accurately during the fault as shown in Figure 4.10. With the half cycle implementation as shown in Figure 4.11 it is again shown that with raw waveform neither the DFT nor the DWT algorithms are able to estimate the phasor accurately and oscillate significantly around the value. There is however a reduction in the oscillation compared to the previous test showing that the decaying DC offset has a significant effect on the algorithms.
Chapter 4. *Analysis of Digital Relay Implementation*

Figure 4.10: Comparison of DFT and DWT during fault with high fault impedance
- Full cycle

Figure 4.11: Comparison of DFT and DWT during fault with high fault impedance
- Half cycle
4.4 Comparison of the DWT and DFT in the Implemented Digital Relay

While the ADC was implemented for sampling and was used in Section 4.3, for the following comparisons the waveforms were generated directly in MATLAB and the ADC and downsampling filters were bypassed in the DSP for reproducible results and so multiple comparative tests could be run with accurate timing. This would also allow waveforms with specific characteristics to be generated that would allow accurate assessment of the algorithms performance and also allow replication of tests documented in the literature [10, 34].

4.4.1 Harmonic Comparison

The following equation (4.1) was used to test and compare the performance of phasor estimation using the DWT and the DFT when harmonics exist in the input signal. Both full cycle (moving sampling window set to the number of samples in 1 period) and half cycle (moving sampling window set to the number of samples in 1 period) were implementations were compared. The fundamental frequency used was 50Hz and sampling rate was set to 3.2kHz.

\[
s = 100 \cos(\omega t) + 5 \cos(2\omega t + \frac{\pi}{3}) + 1.5 \cos(3\omega t + \frac{\pi}{3}) \\
+ 0.5 \cos(4\omega t + \frac{\pi}{1}) + 0.15 \cos(5\omega t + \frac{\pi}{9})
\]  

(4.1)

4.4.1.1 Full cycle

The full cycle analysis in Figure 4.12 shows that phasor estimation using either the DWT or the DFT can filter out the harmonics effectively and estimate the magnitude of the fundamental accurately. The DWT has a small steady state error of 0.14% which is most likely due to rounding errors.
4.4.1.2 Half cycle

While using a full cycle of data to estimate the phasors is more accurate, it is slower to converge so takes longer to detect a fault so the performance of phasor estimation using just a half cycle of data was also assessed.

In Figure 4.13 the DFT and the DWT (using Daubechies 8 wavelets) were compared show that the performance of both is very similar, both are considerably affected by the presence of harmonics (especially the 2nd harmonic) and have difficulty filtering them out. The DFT has a very slight advantage and does not overshoot to the same extent as the DWT, but both have a maximum error of $\pm 5\%$.

Figure 4.14 compares two wavelets, the most simple (Haar) and the most complex tested (Daubechies 10) to test whether using different wavelets affected the accuracy of phasor estimation. There was little difference observed between the two wavelets, Daubechies 10 has a very slight advantage and does not overshoot to the same extent but this would have negligible effect.

Figure 4.15 compares the performance of using different levels of recursion of the DWT to attempt to filter out the unwanted components of the input signal more effectively. It shows also that there is little difference between them, in fact using a higher levels of recursion introduces more error, most likely rounding error.
Figure 4.13: Comparison of Harmonic Performance of DWT and DFT over two cycles (40ms)

Figure 4.14: Comparison of Harmonic Performance of Haar and Daubechies 10 Wavelets
4.4.2 Convergence Performance

One of the key documented advantages of using the DWT for phasor estimation is its faster response time to changes in the input. [9, 10] So to compare the speed of the convergence of phasor estimation using the DFT and the DWT the signal (4.2) was used from [10] with the step occurring after 50ms.

\[ s = \begin{cases} 
50 \sin(\omega t), & t \leq 0.05 \\
100 \sin(\omega t), & t > 0.05 
\end{cases} \quad (4.2) \]

where \( \omega = 2\pi f \), with \( f = 50\text{Hz} \)

The waveform was sampled at 3.2kHz.

4.4.2.1 Full cycle

As seen in Figure 4.16, the full cycle DFT is slower to respond to changes that the DWT at first, but as the DWT estimated phasor gets closer to the actual value its response slows, and the DFT response increases so the DFT and DWT estimated phasors have the same total convergence time. However the DWT reaches 50% of the new value.
2.96ms faster than the DFT. Changing the level of recursion had no significant effect on the convergence in this case.

![Graph showing convergence testing using full cycle analysis](image)

**Figure 4.16:** Convergence testing using full cycle analysis

### 4.4.2.2 Half cycle

As seen in Figure 4.17 the DWT has a slight advantage initially but the total time to converge for both is the same as both reach the new set point at the same time. In Figure 4.18 however, the Daubechies 8 wavelet with extra levels of recursion was used which reduced the convergence time and reached the new set point 1.72ms faster, 82% of the time required for the standard DFT.

As seen in Figure 4.19 which compares the convergence performance of the Daubechies 8 wavelet with different levels of recursion of the DWT, increasing the level of recursion reduces the total time needed to converge, but adds a slight initial delay. Looking at the time scales compared to those in Figure 4.16, the half cycle has a definite advantage in the speed it takes to detect the change, in the case of the signal of (4.2), a 10ms advantage which corresponds to half a cycle.

As seen in Figure 4.20 which compares the Haar and Daubechies 10 wavelets, it was observed that changing the type of wavelet had little effect on the convergence performance of the DWT.
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**Figure 4.17:** Convergence Comparison of the DFT and DWT

**Figure 4.18:** Convergence Comparison of the DFT and DWT with recursion
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Figure 4.19: Convergence Performance of Different Levels of Recursion

Figure 4.20: Wavelet Convergence Comparison between Haar and Daubechies 10
4.4.3 Decaying DC Offset Performance

To assess the ability of the DWT to handle a fault waveform with a decaying DC offset the signal (4.3) was used from [34]. The signal is a constant amplitude sinusoid at the fundamental frequency with a decaying DC offset added and is shown in Figure 4.21. Various values of the time constant decay factor $t$ were tested and the value 0.2 was chosen to be a worst case value based on the values presented in [34]. Being able to filter out decaying DC offset is a critical requirement of phasor estimation algorithms as it was shown to be present in fault waveforms in future distribution networks in Section 2.5.

$$s = I_0 e^{-\frac{t}{\tau}} + I_1 \sin(\omega t + \phi)$$

(4.3)

where $\tau = 0.2$, $I_0 = 1$, $I_1 = 1$

and $\omega = 2\pi f$, where $f = 50$Hz

The waveform was sampled for 8 periods (0.16 seconds) at 3.2kHz.

![Decaying DC Offset Fault Waveform](image)

**Figure 4.21:** Decaying DC Offset Fault Waveform
4.4.3.1 Full cycle

As seen in Figure 4.22, the full cycle DFT can filter out the majority of the decaying DC offset and estimate the magnitude of the phasor within ±3%. The DWT however is significantly affected and estimates the phasor magnitude to be too high at 70% of the actual value, this is then observed to be decaying as the DC offset in the original waveform decays. The accuracy of the phase estimating portion of the algorithms was also assessed, if it is estimated correctly it should appear as a series of linear curves, starting at zero and peaking at 6.28 (2π radians). As seen in Figure 4.23 the DFT is able to estimate the phase correctly, however with the higher levels of DC offset the DWT has large errors when the phase approaches the values of 0, π and 2π.

As the DWT algorithm works by first calculating the phase and then using the result to calculate the magnitude of the phasor this may be contributing to the large error of the magnitude calculation. To determine whether this was the case, a simple test was performed, the DFT was first used to calculate the phase (which it had proven to be able to do accurately for this waveform), then the DWT used to calculate the magnitude. The result in Figure 4.24 shows that while there is an error in the DWT phase calculation, this has no significant effect on the error in the magnitude of the phasor calculated by the DWT.

![Figure 4.22: Decaying DC Offset Comparison using full cycle analysis](image)
Figure 4.23: Decaying DC Offset Comparison of Phase using full cycle analysis

Figure 4.24: Decaying DC Offset Comparison of DWT using the phase from FFT
4.4.3.2 Half cycle

As seen in Figure 4.25, the estimated phasor magnitudes from both the DFT and DWT are affected by the decaying DC offset to a large extent. The DFT overshoots to 224% of the actual value and then undershoots to 18%. The DWT does slightly better with an overshoot of 232% and an undershoot of 60% of the value. Figure 4.26 is a zoomed in view over a shorter time scale of Figure 4.25 and shows this more clearly. Changing the level of recursion or the wavelet type had no significant effect.

![Graph showing decaying DC offset comparison with DFT and DWT](image)

**Figure 4.25:** Decaying DC Offset Comparison using half cycle analysis
4.4.4 Grid Frequency Variation

To compare the ability of the DWT and the DFT to perform phasor estimation where the grid frequency is not exactly at 1.0pu (standard error margin is 2.5%) the fundamental frequency was varied to see the effect. As a 50Hz base frequency was being tested, the frequency was started at 48.75Hz, and increased to 51.25Hz during the course of the test. The signal that was generated is defined by Equation 4.4.

\[ s = 100 \sin(\omega t + \phi) \]  \hspace{1cm} (4.4)

where \( \omega = 2\pi f \), \( 48.75Hz < f < 51.25Hz \)

Both phasor estimation using the DFT and phasor estimation using the DWT are heavily affected by variations in the fundamental frequency variation, both to the same extent in both the full cycle implementation as shown in Figure 4.27 and the half cycle implementation as shown in Figure 4.28. The error is also greater with higher levels of recursion of the DWT and the half cycle implementation.

If the phase locked loop (PLL) were to be implemented as detailed in Section 3.4.5 to track the fundamental frequency, the flexibility of the DWT algorithm is expected to
enable the magnitude to be estimated much more accurately in the case of fundamental frequency variation. Implementing this was outside the scope of the thesis but is a possibility for future research.

![Figure 4.27: Grid Frequency Variation Comparison - Full cycle](image)

![Figure 4.28: Grid Frequency Variation Comparison - Half cycle](image)
Chapter 5

Conclusion

In this thesis the emerging distribution network was investigated. It was shown that with the advent of new technologies such as smart grids new protection schemes will be required. The continued introduction of DG sources presents new challenges to existing top down based protection of a distribution feeder. Fuses coordinated by time delays may need to be replaced by overcurrent relays as there is expected to be a requirement for protection to be adaptive to respond to realtime changes of network characteristics and topology such as islanding and to incorporate communications such as IEC61850. Communications will enable more coordination between protective devices and the ability to monitor the network to more efficiently repair faults.

To evaluate the effects of these changes a distribution feeder was simulated with a DG source added. It was observed that significant levels of decaying DC offset were present in the current waveforms during faults in a distribution network when DG is present. The level of the decaying DC offset was shown to be inversely proportional to the series impedance between the source and ground, with a higher series impedance increasing the peak level of the decaying DC offset. The series impedance is made up of the sum of the source impedance, total distribution line impedance and the fault impedance. Line to ground faults were shown to have the highest levels of decaying DC offset. Changes in the loads connected to the feeder were shown to have little effect on the level of decaying DC offset in the fault current. The instant in which the fault occurs also has a large effect on the peak level of the decaying DC offset in the fault current waveform with the highest peaks occurring at a phase offset of $\frac{3\pi}{4}$ and $\frac{3\pi}{2}$. As the fault could occur at any time this
would need to be taken into account to ensure the worst case level is calculated to be used when designing protection schemes and setting limits in overcurrent relays. From simulating the IEEE 34 bus feeder it was determined that introducing DG into larger, more complex feeders will have significant effect on the protection schemes. Depending on the location of the fault the current direction could be reversed and significant levels of decaying DC offset may be present. The presence of decaying DC offset in the fault waveform has implications for protection devices such as overcurrent relays as the algorithms they use can be susceptible to errors in estimating phasors when decaying DC offset is present in the fault waveform. In current distribution networks the protection is not required to act quickly which means that extensive filtering can be implemented to remove the decaying DC offset as the additional time delay it causes will not be a problem. However with increased amounts of DG being connected to the grid there is expected to be a requirement for faster acting protection. This is because the DG is likely to become a larger portion of the electricity supply for some networks so may be expected to stay connected and ‘ride-through’ minor faults in the same way large generators do today. Protection will need to be fast enough to act quickly in this scenario to protect the DG sources so there is a requirement for faster, more accurate phasor estimation algorithms for digital relays that can filter out DC offset.

In this thesis a test platform was designed and implemented to assess protection algorithms. Phasor estimation using the Discrete Fourier Transform and Discrete Wavelet Transform algorithms were implemented to run concurrently in the digital relay. It was determined that within the digital relay, the sampling rate of the digital waveform sampled by the ADC that is provided to the DFT is critical as the fundamental frequency must fall into the centre of a frequency ‘bin’. The DWT has no such requirement and can operate at any sampling rate within the computational limits of the processor. On reviewing the literature it was determined that the algorithm proposed to be used for phasor estimation using the DWT had a disadvantage due to a limitation of the dot product. A method for overcoming this by using a second reference waveform with a phase offset was found and implemented. It was determined that the computation power required to implement phasor estimation using the DWT is similar to the current DFT algorithm and in some cases is likely to be even less so can be implemented on current hardware.
The phasor estimation algorithms were critically assessed using fault waveforms simulated from a distribution feeder with DG. With the full cycle implementation the DFT was able to filter out the majority of the decaying DC offset however the overshoot of the phasor estimation using the DWT was 12% higher than the DFT. With the half cycle implementation the phasor estimation algorithm using either the DWT or the DFT was significantly affected by harmonics present in the fault signal as well as the decaying DC offset, with significant oscillations present around the value. Increasing the decomposition level of the DWT had no significant effect. With a fault waveform that had no decaying DC offset present phasor estimation using either the DFT or the DWT had similar performance.

Phasor estimation using the DWT was also critically assessed and compared to the DFT using mathematically generated waveforms. Varying decomposition levels of the DWT and the Haar, Daubechies 4, 8 and 10 wavelets were assessed. When the waveform contains harmonic components there is no significant advantage of phasor estimation when using the DWT over the DFT. Changing the wavelet type or the recursion level of the DWT also had little effect. When a decaying DC offset is present in the fault waveform the DWT is heavily affected in both half cycle and full cycle implementations. In comparison the DFT is able to filter it out with a full cycle implementation. In regards to convergence, the DWT has an advantage over the DFT and reaches the new set point 82% faster with the half cycle implementation. It was found that higher levels of recursion of the DWT have a positive impact on the rate of convergence. When there is a variation in the fundamental frequency, significant errors were present in the estimated phasor when using either algorithm.

From this we can determine that phasor estimation using the DWT does not offer any significant advantage over the existing standard algorithm, the DFT. On a future distribution network that is expected to include Distributed Generation, the decaying DC offset present during faults would cause large inaccuracies in the phasor estimation when using the DWT. If phasor estimation were to be implemented, a method of removing the decaying DC offset would need to be applied before the signal was passed to the algorithm.
Chapter 6

Future Research

There are many opportunities for future research in this area. In this thesis a test platform was developed to analyse protection algorithms and the proposed phasor estimation using the Discrete Wavelet Transform and phasor estimation using the Discrete Fourier Transform were implemented at tested. There is scope here to develop, implement and test other protection algorithms for phasor estimation on the same platform. Their performance could then assessed against fault waveforms expected to encountered on future distribution networks. The platform is also able to test waveforms captured directly during faults on electricity networks using the industry standard COMTRADE format so the implemented algorithms could be tested with real faults that have occurred.

In the implemented test platform communication was provided by a USB connection on the development board based on the JTAG interface. A possible direction for future research is to expand this to include an Ethernet interface based on the IEC61850 communications standard or other standards proposed for smart grids. This would allow development and evaluation of protection schemes that involve multiple protection devices and communication.

One point noted during the development of the testing platform and the implementation of the phasor estimation using the Discrete Wavelet Transform was the flexibility of the DWT to calculate the phasor of any fundamental frequency contained in the signal, irrespective of sampling frequency with only a software change of frequency of the generated reference sine wave required. By implementing a PLL it is expected that the
phasor estimation using the DWT algorithm could track any changes in the fundamental frequency and give an accurate phasor estimation of the fundamental at any frequency.
Appendix A

IEEE 13 Bus Test Feeder

The standard IEEE 13 bus test feeder from [16].

Table A.1: Overhead Line Configuration Data

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<th>Neutral ACSR</th>
<th>Spacing ID</th>
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<td>4/0 6/1</td>
<td>500</td>
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<td>602</td>
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<tr>
<td>604</td>
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Table A.2: Line Segment Data

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<th>Config</th>
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<td>500</td>
<td>603</td>
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<tr>
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<td>671</td>
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<td>606</td>
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<th>kV-Low</th>
<th>R - %</th>
<th>X - %</th>
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### Table A.4: Capacitor Data

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<td>Phases</td>
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### Table A.6: Compensator Settings

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<td>Voltage Level</td>
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### Table A.6: Spot Load Data

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### Table A.7: Distributed Load Data

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<th>Ph-1 kVar</th>
<th>Ph-2 kW</th>
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<th>GMR (Feet)</th>
<th>Rating (Amps)</th>
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Appendix B

Discrete Wavelet Transform

Filter Coefficients

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<th>Haar (Daubechies 2)</th>
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Bibliography


[40] National, Instruments. (November 2009) Ni 9263 - 4-channel, 100 ks/s, 16-bit, 10
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