Novel Types of Cyclically-Coupled Quasi-Cyclic LDPC Block Codes

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***Abstract*— Cyclically-coupled quasi-cyclic LDPC (CC-QC-LDPC) block codes have been shown to achieve outstanding bit error performance with extremely low error floor. In this paper, we propose two new types of CC-QC-LDPC block codes which can achieve a larger girth. We present the error performance of the CC-QC-LDPC codes constructed by the new mechanism. We show that even with a shorter codelength, the new CC-QC-LDPC codes can outperform the traditional CC-QC-LDPC ones.**

I. Introduction

Low-density parity-check (LDPC) [1] codes have been shown to possess theoretical limits approaching the channel capacity. Moreover, extremely long codes (length larger than 10^6) can perform very close to their theoretical limits because the probability of having short cycles in their graph representations is very small [2]. However, such long codes are not practical in most applications because of the high hardware complexity and high latency [3], [4]. Codes of length ranging from 500 to $30,000$ are of more practical values because they can be applied to many communication systems.

It is also well-known that error performance of LDPC codes with finite lengths may degrade significantly from their theoretical limits if there exists many short cycles in their associated Tanner graphs. Such short cycles will also form structures such as stopping sets [5], [6], elementary/dominant/detrimental trapping sets [7]–[9] and absorbing sets [10]–[13] that give rise to the error floor in the high signal-to-noise-ratio (SNR) region. One effective way to maximize the girth (shortest cycle length) of an LDPC block code is to connect the variable nodes and the check nodes based on the progressive-edge-growth (PEG) method [14] or its modifications [15], [16]. Yet, the codes constructed using these algorithms may still possess error floors in the high signal-to-noise-ratio (SNR) region.

To lower the error floor by reducing the occurrences of stopping sets and/or elementary/detrimental trapping sets and/or absorbing sets, various construction methods that (i) avoid small-size stopping sets [17]; (ii) avoids short cycles with approximate cycle extrinsic message degree (ACE) below a given value [6]; (iii) combines PEG and ACE [15]; (iv) combines PEG and Approximate-minimum-Cycle-Set-Extrinsic-message-degree (ACSE) [9]; and (v) controls the absorbing set spectrum [18], [19]; have been proposed [6], [9], [15], [17]–[19]. These methods in general can be applied to the construction of random LDPC block codes as well as structured LDPC block codes such as quasi-cyclic LDPC (QC-LDPC) block codes. Another way to lower the error floor is to use LDPC convolutional codes (LDPCCCs) and QC-LDPC convolutional codes (QC-LDPCCCs) [20]–[22]. However, the complexity of an LDPCCC decoder is much higher.

Recently, a novel type of LDPC block code called "cyclically-coupled quasi-cyclic LDPC block codes" (CC-QC-LDPC code) has been proposed [23]. It is formed by spatially-coupling a number of identical QC-LDPC block codes partially in a cyclic manner. Furthermore, this property allows a simple design of a CC-QC-LDPC decoder. To verify the feasibility of the idea that coupling the QC-LDPC block codes partially can improve the overall error performance, the authors in [23] construct a CC-QC-LDPC code with a rate of $5/6$ and length 98000. The only criterion in the design is that the girth (minimum cycle length) equals 8. No other optimization technique such as minimum distance analysis has been applied. An experimental decoder has also been implemented on a field-programmable-gate-array (FPGA) device. Under the condition that 10 decoding iterations are performed for each codeword, the decoder achieves an amazing throughput of 3.0 Gb/s. Moreover, the CC-QC-LDPC decoder has a much lower complexity requirement and 50% higher throughput compared to an LDPCCC decoder that achieves similar BER performance [22].

For this rate-$5/6$ CC-QC-LDPC code, no error floor has been observed above a bit error rate (BER) of 10^{-14} and a BER below 10^{-15} is expected at a bit-energy-to-noise-power-spectral-density ratio (E_b/N_0) of 3.5 dB. A net coding gain of 11.5 dB is therefore achieved. Furthermore, having taken the difference in code rates into consideration, the CC-QC-LDPC code has still demonstrated substantially improvement over the un-coupled QC-LDPC block codes.

In this paper, we propose two new types of CC-QC-LDPC codes which possess better girth properties. We construct the codes and simulate their error performance. We organize this paper as follows. In Section II, we review the structure of CC-QC-LDPC codes and the decoding mechanism. In Section III, we describe the structures of the two new types of CC-QC-LDPC codes. Finally, in Section IV, we present the error performance of the new CC-QC-LDPC codes.

II. Cyclically-Coupled QC-LDPC Codes

The parity-check matrix of a CC-QC-LDPC code, denoted by $\mathbf{H}_{cc,k}$, is given by [22]

$$\mathbf{H}_{cc,k} = \begin{bmatrix} \mathbf{H}_l & \mathbf{H}_m & \mathbf{H}_r & & & & & & \\ & & \mathbf{H}_l & \mathbf{H}_m & \mathbf{H}_r & & & & \\ & & & & \mathbf{H}_l & \cdots & & & \\ & & & & & \ddots & & & \\ & & & & & \cdots & \mathbf{H}_r & & \\ \mathbf{H}_r & & & & & & \mathbf{H}_l & \mathbf{H}_m \end{bmatrix} k \text{ rows} \tag{1}$$

where the sub-matrices $\mathbf{H}_l$, $\mathbf{H}_r$ and $\mathbf{H}_m$ consist of circulant permutation matrices (CPMs); $\mathbf{H}_l$ and $\mathbf{H}_r$ are of the same size; and $\mathbf{H}_m$ has the same number of block rows but not necessarily the same number of block columns as the other two sub-matrices. The "coupling degree" W is defined as the number of coupled columns, i.e., the number of columns in $\mathbf{H}_l$ or $\mathbf{H}_r$. For example in [22], $\mathbf{H}_l$ and $\mathbf{H}_r$ consist of 4 block rows and 4 block columns, while $\mathbf{H}_m$ has 4 block rows and 20 block columns.

Defining a subcode $\mathbf{H_c}$ as

$$\mathbf{H_c} = \begin{bmatrix} \mathbf{H}_l & \mathbf{H}_m & \mathbf{H}_r \end{bmatrix}, \tag{2}$$

a CC-QC-LDPC code can be constructed with k subcodes and by shifting and coupling $\mathbf{H}_l$ and $\mathbf{H}_r$ from two consecutive subcodes $\mathbf{H_c}$ in a cyclic manner. However, $\mathbf{H}_m$ is not coupled. In general, we assume that the subcode $\mathbf{H_c}$ contains $J \times L$ CPMs each of size $z \times z$.

For every subcode $\mathbf{H_c}$, there will be a corresponding sub-decoder within the CC-QC-LDPC decoder. In the above example, there will be k sub-decoders connected in a cyclic way, i.e., the first sub-decoder connected to the second and k-th sub-decoders; the second sub-decoder connected to the first and third sub-decoders; etc. Each sub-decoder is responsible for (i) the decoding of the corresponding subcode and (ii) exchanging check-to-variable (C2V) and variable-to-check (V2C) messages with its adjacent sub-decoders. With such a decoder design, each sub-decoder can remain relatively simple and the overall throughput is approximately the sum of the throughputs of the sub-decoders.

III. Novel CC-QC-LDPC Codes with Larger Girth

Assuming $J = 4$ and $W = 4$, Fig. 1(a) illustrates a *full* CC-QC-LDPC code. Here all the sub-matrices are non-zero and mechanisms such as fast hill-climbing [24] can be applied to select the CPMs such that a desired girth can be achieved. In [22], a girth-8 CC-QC-LDPC code is found with $z = 1024$. When z is reduced to $512, 256$ and 128, however, we can only find CC-QC-LDPC codes with a girth of 6 due to substantially smaller search spaces.

With an aim to improving the girth, we propose two special types of CC-QC-LDPC codes which contain zero matrices. They are shown in Figs. 1(b) and 1(c), respectively. Type-I CC-QC-LDPC codes is characterized with $\mathbf{H}_l$ being upper triangular and $\mathbf{H}_r$ being *strictly* lower triangular; and Type-II CC-QC-LDPC codes is characterized with $\mathbf{H}_l$ being upper triangular and $\mathbf{H}_r$ being lower triangular. By converting some

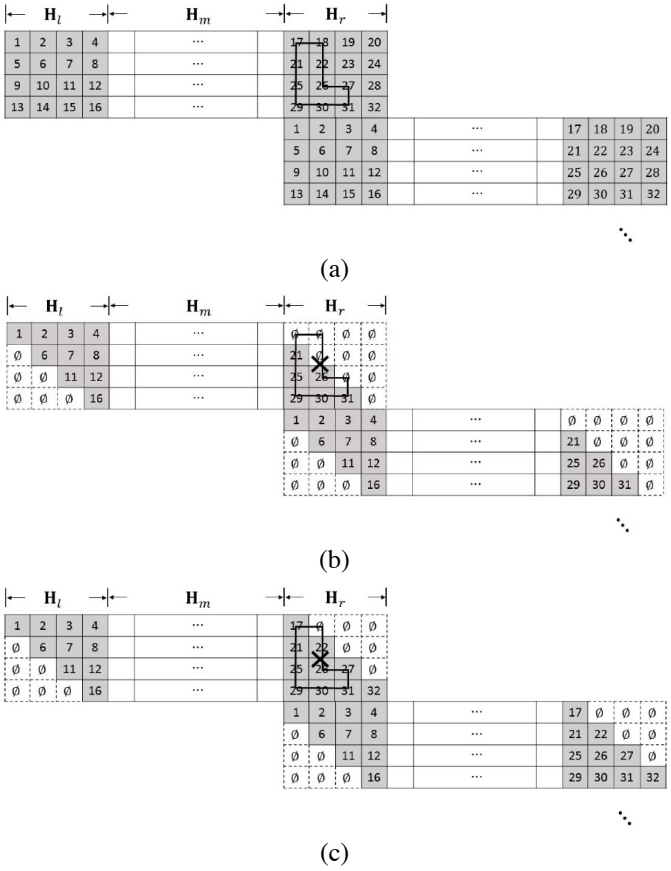

Fig. 1: CC-QC-LDPC codes. (a) Full, (b) Type-I and (c) Type-II.

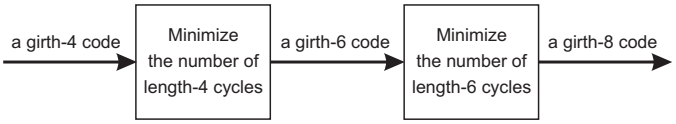

Fig. 2: Fast hill-climbing algorithm [24].

sub-matrices in Fig. 1(a) to zero submatrices, we form the Type-I and Types-II CC-QC-LDPC codes shown in Figs. 1(b) and (c). Because of the conversion, cycles passing through these removed submatrices can be eliminated. One such removal of cycle-6 has been demonstrated in Fig. 1. As a result, CC-QC-LDPC codes with girth 8 can be easily designed with a smaller value of z, i.e., shorter codelength. Note that by converting the submatrices in $\mathbf{H}_l$ and $\mathbf{H}_r$ instead of $\mathbf{H}_m$ to zero submatrices, we can maintain column weights of at least 4.

IV. Simulation Results

We compare CC-QC-LDPC codes with the following parameters: $J = 4, L = 28, W = 4, k = 4$ and a code rate of $5/6$. For all cases, we optimize the girth of the CC-QC-LDPC codes using the fast hill-climbing method [24], the block diagram of which is shown in Fig. 2. Note that in the

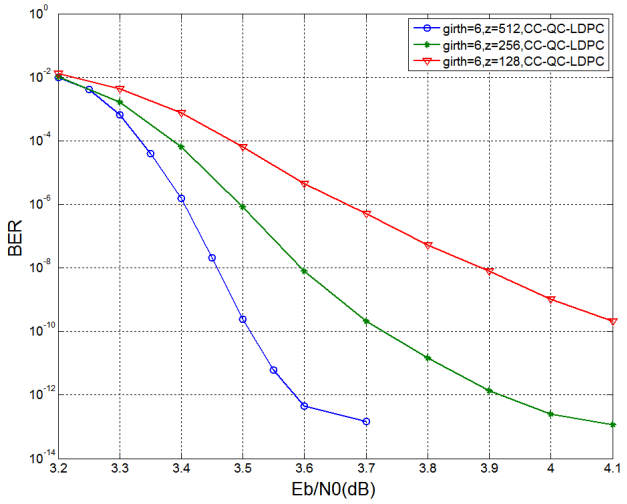

Fig. 3: Bit error rate of *full* CC-QC-LDPC codes with $z = 512, 256$ and 128.

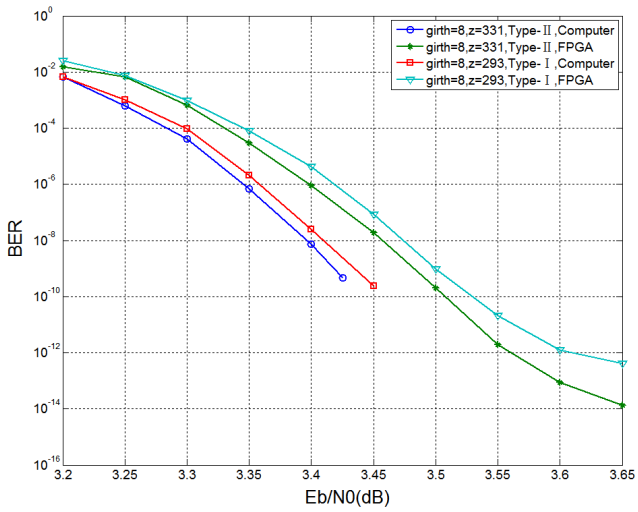

Fig. 4: Bit error rates of Type-I and Type-II CC-QC-LDPC codes. $z = 293$ and 331, respectively, for Type-I and Type-II codes.

optimizing process, it is adequate to consider cycles formed by two consecutive subcodes only, i.e., cycles found in Fig. 1.

First, we consider the *full* CC-QC-LDPC codes with $z = 512, 256$ and 128. The optimized codes all have the same girth of 6. In Fig. 3, we present the bit error rate (BER) results found by FPGA implementation. We can observe that as the code length increases, the BER performance improves. However, error floor exists in all cases.

Next, we attempt to construct Type-I and Type-II CC-QC-LDPC codes with girth-8. The minimum values of z that achieve girth-8 are 293 and 331, respectively, for Type-I and Type-II codes. In Fig. 4, we further present the BER results found by computer simulation and FPGA implementation. Comparing the computer simulation and the FPGA implementation results, we observe that the BER degrades by about 0.05 to 0.1 dB. Moreover, Type-II CC-QC-LDPC code slightly outperforms Type-I code in terms of BER and has a lower error floor. One possible explanation is that the column weights of Type-I code are all 4 but the column weights of Type-II code can be 4 or 5.

Finally, we compare the FPGA experimental BERs of all three different types of CC-QC-LDPC codes in Fig. 5. We find that Type-I and Type-II CC-QC-LDPC codes outperform full CC-QC-LDPC codes with $z = 128$ and 256, and have similar BER performances as full CC-QC-LDPC codes with $z = 512$. In particular, Type-I code (with $z = 293$) though having a shorter codelength can achieve very similar BER performance compared with the full CC-QC-LDPC code with $z = 512$. Type-II code (with $z = 331$) can even accomplish a lower error floor compared with the full CC-QC-LDPC code with $z = 512$.

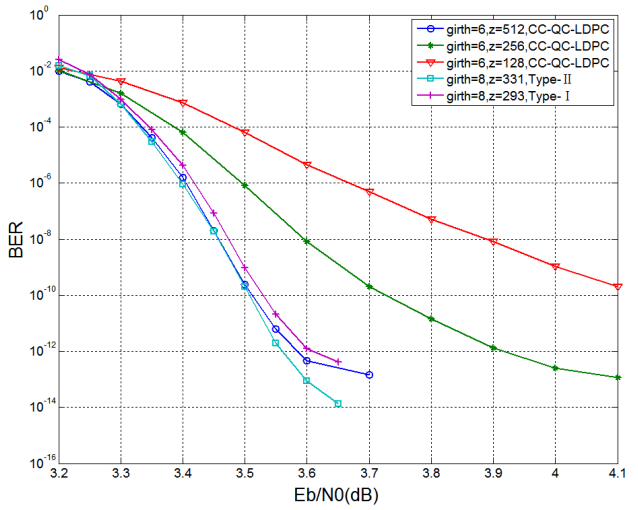

Fig. 5: Bit error rate of all three types of CC-QC-LDPC codes.

V. Conclusions

We have proposed two new types of CC-QC-LDPC codes and have demonstrated their superior BER performance and low error floors even with short codelengths. Our future tasks include comparing our BER results with traditional QC-LDPC codes with similar codelengths and designing ways to further lower the error floors.

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